Mater. Res. Soc. Symp. Proc. Vol. 1021 © 2007 Materials Research Society 1021-HH05-24

Nanomechanical Properties of strained Silicon-on-Insulator (SOI) Films epitaxially grown on $Si_{1-x}Ge_x$ and Layer Transferred by Wafer Bonding

Nathanael Miller[1,2], Kandabara Tapily[2,3], Helmut Baumgart[2,3], George K. Celler[4], Francois Brunier[4], and A. A. Elmustafa[1,2]

[1]Mechanical Engineering, Old Dominion University, 224 Kaufman Hall, Norfolk, VA, 23529

[2]The Applied Research Center-Jefferson Lab, Newport News, VA, 23606

[3]Electrical Engineering, Old Dominion University, 231 Kaufman Hall, Norfolk, VA, 23529

[4]SOITEC, Bernin, France

ABSTRACT:

Using nanoindentation, we report on the elasto-mechanical properties of multiple thin films of strained Silicon-on-Insulator (sSOI) and extreme strained Silicon-on-Insulator (xsSOI). We measured the hardness and elastic moduli of the films. Both the hardness and elastic moduli were determined for the surface layers of SOI, SiO_2, and the bulk silicon using the continuous stiffness method (CSM) XP Nano Instruments Nanoindentation tester. The measured hardness values for bi-axially tensile strained sSOI films and relaxed SOI films are found to be 9.23 GPa and 9.36 GPa respectively. The moduli are 101.2 GPa and 105.6 GPa respectively. Since these values are different from the bulk Si values of 12.5 GPa and 160.0 GPa for hardness and modulus, further investigation of the elastic properties of the nanolayers composite will be performed including simulation.

1. INTRODUCTION:

Manufacturing processes in the microelectronics industry have relied on continued miniaturization of devices in silicon planar technology to increase performance, functionality and bit density. Devices are geared toward faster, smaller, more densely packed structures and device dimensions are approaching quantum physics. This in turn dictates advanced chip engineering technology. The changes in device dimensions provoke development of new materials, device structures, processing technologies, and architectures. Semiconductor nanowires, silicon nanocrystals, and quantum dots are among the projected candidate nanomaterials to replace classical materials used in existing microelectronics fabrication. High performance faster devices are listed on the International Technology Roadmap for Semiconductors (ITRS) as a critical step in keeping up with Moore's law at the 45 nm technology node and beyond. One way of making faster high performance devices with enhanced carrier mobility is through strain engineering technology. Strained SOI wafer technology increases the device speed 30 to 40 %, and reduce parasitic effects, leakage current, and power consumption up to 50%. The samples used in this research are relaxed Silicon-on-Insulator (SOI) single crystal thin films, bi-axially tensile strained and extra-strained Silicon-on-Insulator (sSOI & xsSOI) thin films with a mean 1.3 GPa stress level [1, 2]. Because of the potential advantages of strained channel silicon devices, it is imperative to investigate the electrical and mechanical properties of those materials. Measured

electrical properties of bi-axially strained Si films have been disseminated in the literature [3, 4]. The objective of this paper is to thoroughly characterize the elasto-mechanical properties of strained Silicon-on-Insulator (sSOI) nano-sized single crystal films.

2. SAMPLE FABRICATION:

SOI technology offers CMOS performance enhancement with the use of an embedded oxide layer to isolate transistors from the substrate, which results in lower parasitic capacitance and reduced junction leakage. Combining SOI substrates with strained Si technology takes advantage of the performance enhancement by both SOI and the increased carrier mobility of strained Si. There are two main approaches in producing mobility enhancement: strain engineering and orientation effects. The method of choice for strain engineering is to epitaxially grow a $Si_{1-x}Ge_x$ layer on a Si substrate. By selectively choosing the Ge doping content of $Si_{1-x}Ge_x$, one can modulate the built-in strain level. Subsequently, a thin bi-axially tensile strained Si layer can be grown epitaxially on top of a strain relaxed $Si_{1-x}Ge_x$ buffer layer in order to obtain a Ge-free strained Si epitaxial device layer. The samples used in this experiment are fabricated through the SMART CUT ™ technology, which employs a combination of hydrogen ion implantation and wafer bonding technology. Bonding between two Si wafers typically takes place via an oxide layer. The desired thickness of the final SOI device layer is determined by the hydrogen implantation step. The projected hydrogen implant range at a given implant energy, establishes the device layer thickness following film exfoliation. The wafer is then bonded to another silicon wafer. In the final film exfoliation step, high temperature annealing causes the bulk of the device wafer to split by cleavage from the device layer. This results in an SOI device layer separated by buried oxide film from the Si substrate wafer. Figure 1 provides the schematic process flow of SMART CUT ™. In similar fashion the bi-axially tensile strained sSOI films were obtained with a fabrication sequence of epitaxially growing 150Å to 600Å strained Si films on a relaxed 20% Ge containing $Si_{1-x}Ge_x$ buffer layer on a donor wafer. During epitaxy the Si lattice stretches to match the larger $Si_{1-x}Ge_x$ lattice. The larger lattice constant of Ge produces a 4.1 % lattice mismatch with the Si crystal. Following successful bonding of both wafers, the donor wafer was split off with the SMART CUT ™ exfoliation technique. The surface is then finished with an etching process to completely remove all traces of the $Si_{1-x}Ge_x$ film, resulting in a Ge-free bi-axially strained Si film on amorphous SiO_2 insulator [1, 2]. The insulating buried oxide beneath the SOI film is on the order of 145 nm thick.

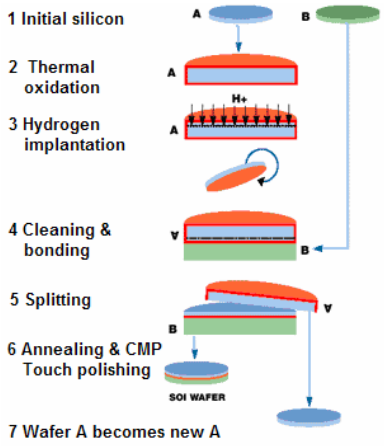

Figure 1. SMART CUT ™ process (source: SOITEC, Bernin, France) [1]

3. EXPERIMENT SET-UP:

Instrumented indentation, or nanoindentation, has been advanced over the last 20 years to measure the mechanical properties of small specimens including modified surface layers, tribological coatings, microelectronic interconnects, micro-electro-

mechanical-systems (MEMS). Nanoindentation can be used to characterize the mechanical properties of material structures, and this is particularly useful for examining properties of thin films and nanoscopic wires. The versatility and potential for precise and highly sensitive measurements, nanoindentation enables scientists to study mechanical properties of a variety of materials including the cell walls in plants and viscoelastic properties of cartilage bone materials. Most often instrumented indentation is used to measure hardness and elastic modulus, but it can also used for investigating rate-sensitive plasticity or creep. Advances in fabrication and processing of nanostructured materials, nano-electronics, and nanorods resulted in the rapid development of experimental methods for characterizing their properties.

Nanoindentation experiments were conducted using a Nano Indenter® XP in conjunction with a continuous stiffness measurement (CSM) unit made by MTS Nano Instruments. The CSM device adds capabilities not possible with conventional indentation testing methods. By the introduction of a small and well controlled oscillation into the normal loading sequence of the Nano Indenter®, the CSM can monitor the contact depth and the contact stiffness throughout loading of the indenter head, unlike conventional indentation testing methods, the use of the CSM makes possible the measurement of material hardness and elastic-modulus as a continuous function of depth for a single indent [5]. In this paper, we measure thin film material properties such as hardness of nanolayer composites, amorphous silicon oxide interface and single crystal bulk silicon substrates using the CSM nanoindentation technique. The Smart Cut Wafer Bonding technique produces a multi-layer nanocomposite sample illustrated schematically in Figure 2 with an active device layer of strained Si which is dielectrically insulated from the substrate. Nano Indentation experiments start at the surface of the top sSOI film and measure the strained Si film first. Probing proceeds from sample top towards sample bottom and depending on the penetration depth of the Berkovich tip we continuously measure data either from the crystalline strained sSOI top film or from the buried oxide layer (BOX) underneath or ultimately for very deep indents we obtain bulk Si properties from the Si substrate underneath the films.

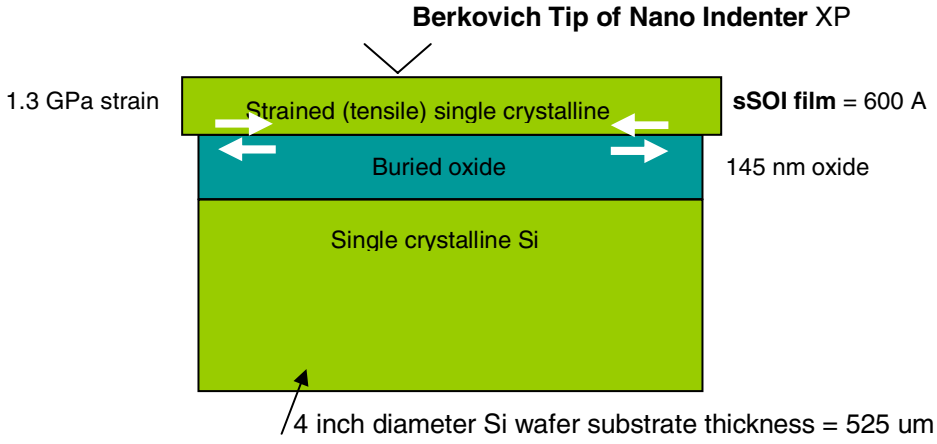

Figure 2. Schematic cross-section of composite sSOI sample being probed by the Berkovich tip of the Nano Indenter XP system.

EXPERIMENTAL DATA:

The surface quality and surface preparation of the samples enable us to obtain data at very shallow depths of indentation. From previous experience with the CSM Nano

Indenter®, there is a direct correlation between the mean surface-feature size and the quality of the shallow data. The manufacturers' CMP planarization process prepared the SOI samples in such a way that the surface topology received a smooth and uniform device grade polish. This made it possible to obtain data points at shallow depth of indentation, which are consistent with other data from deep indents. The methods used in the operation of the Nano Indenter® implement surface locating algorithms because of the delicate and precise nature of the instrument. These algorithms rely on establishing contact with the surface to determine the thermal drift prior and during the indentation test. The indenter tip moves via a piezo-driven stage to a slightly different site where the surface is undamaged. If the surface is uneven the instrument loses the location of the surface, which could result in either the failure to generate a desired indent or generate an indent that will produce useless load depth data

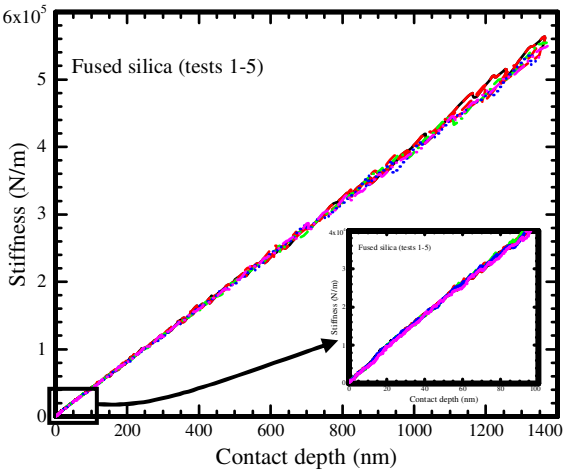

Figure 3. Tip calibration using fused silica

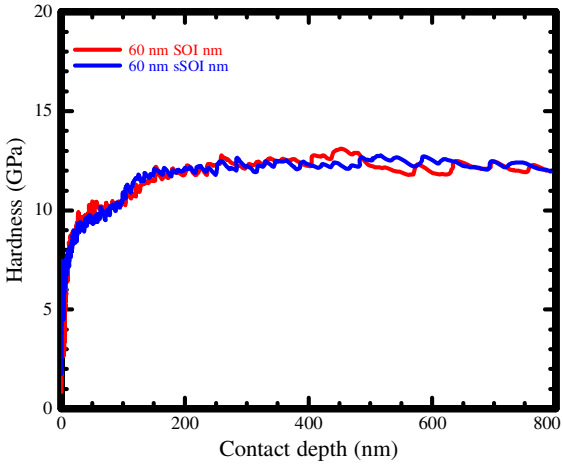

Figure 4. Hardness vs. Contact depth

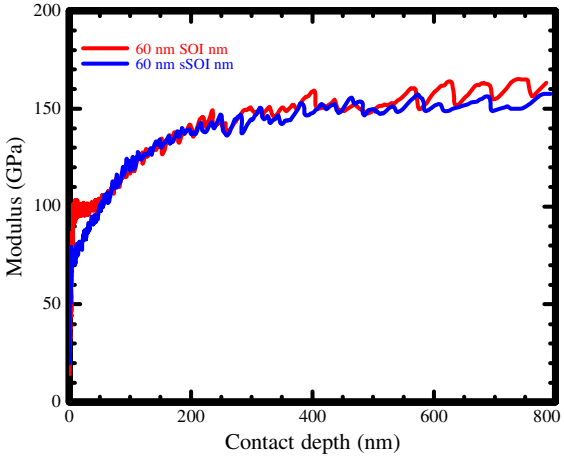

Figure 5. Modulus vs. Contact depth

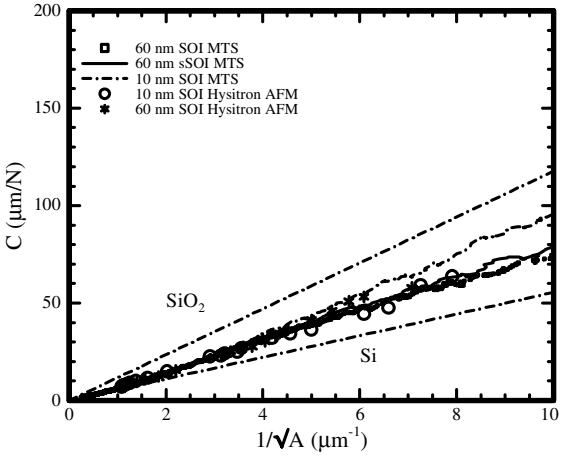

Figure 6. Compliance vs. $1/\sqrt{A}$

Indentation measurements were performed on a fused silica calibration standard using an MTS Nanoindenter XP. The nanoindentation data were taken using a Berkovich tip and a depth-control method with the CSM unit engaged and an oscillating frequency of 50 Hz. The experiments consisted of first loading the indenter into the specimen, then

holding the load constant for 5 seconds, then unloading. To calibrate the indenter tip, we plot the stiffness vs. contact depth for fused silica in Figure 3. As depicted by the figure, the data for the five tests correlate well. The data for contact depth less than 100 nm is blown out and shown by the insert to the right in Figure 3. We also observe that the data for contact depth less than 100 nm correlate well. Subsequent to tip calibration, we performed multiple indents at four different depths for each SOI sample based on the Si film-thickness. The first sets of data were taken at approximately 80% of the film thickness. This was followed by a set of indents penetrating up to the Si/SiO_2 interface and another set which penetrated to twice the film-thickness. Additionally, a set of deep indentation data were taken on each sample to verify bulk-Si material properties on a sample-by-sample basis. For example, the tested sSOI sample, had a device layer film thickness of 15 nm. Accordingly, data were taken at depths of 10 *nm*, 15 nm, 20 *nm*, and 1000 *nm*. Taking data at various depths using the CSM was found redundant, as the nanoindenter yielded consistent results depending on the depth of indentation regardless of the magnitude of the penetration depth. To further illustrate this, when the data that were taken at 15 *nm* depth were superimposed on the first 15 *nm* of the 1000 *nm* depth, little to no *change* was detected between the two data. In Figure 4 we plot hardness versus contact depth of indentation. As we notice from the figure the hardness increases with increasing depth of indentation. To accurately determine the hardness and elastic properties of these individual nanocomposite layers, we have simulated this configuration taking into account the effect of the interface. This will be covered in details in an accompanying publication. Also we noticed the hardness changes at the interface of SOI/SiO_2 and the SiO_2/Si. We also observed similar results for the modulus seen in Figure 5. The areas of the indents were measured using a calibrated AFM Hysitron nanoindentation system. From the compliance data in Figure 6 we observe that the results of the experimental data of all three films from the MTS nanoindentation and the Hysitron AFM nanoindenter correlate well with each other and collapse and cluster around the 60nm sSOI films at shallow and deep indents respectively. As mentioned before, the use of the CSM resulted in a continuous data set that starts
very near the surface and continues to the maximum depth of that particular indent.

VALIDATION OF RESULTS:

In addition to the hardness and moduli measurements obtained from the MTS nanoindentation system, indents were imaged in calibrated optical and field emission scanning electron microscopes (FESEM). However, because of the inaccuracies inherent to “optical” methods, we did not want to rely on them alone. Therefore, we used SEM images to indirectly determine the projected contact area and compare the results with the values obtained from the XP nanoindentation system. We compare the experimental results of hardness and moduli produced in this research for bulk Si substrate of the SOI samples with literature values of bulk Si. The two results correlate well, as demonstrated in Fig 7 a & b showing measured data obtained from the Si substrate underneath the buried oxide layer. Representative scanning electron micrographs of Berkovich indents are shown in Fig. 8. Fig. 8a shows an SEM image of a 1000nm indent in SOI. Fig. 8b shows the same indent with lines drawn to illustrate how the area was calculated. The lines are drawn in Fig. 8b to represent reasonable limits on the areas of the indents based on the way in which the micrographs are interpreted. The distortion generated by the apparent cracking and flaking of the thin-film impeded obtaining accurate measurements

of the area with reasonable certainty. To approximate area measurements while accounting for sink-in, two areas were calculated and averaged. The areas were calculated by fitting a spline, with the use of Autodesk Inventor® to the apparent contact area and to the sink-in affected regions around the indent. The areas enclosed by the two splines were calculated separately using the software and averaged to yield the value used in the development of
the hardness. The hardness was derived by dividing the applied load, provided by the Nano Indenter®, by the SEM calculated area. The resulting hardness were 13.8 GPa on average as compared to the 12.2 GPa obtained from the indenter. The estimated systematic error in the area calculation, for the indents measured using the SEM, is

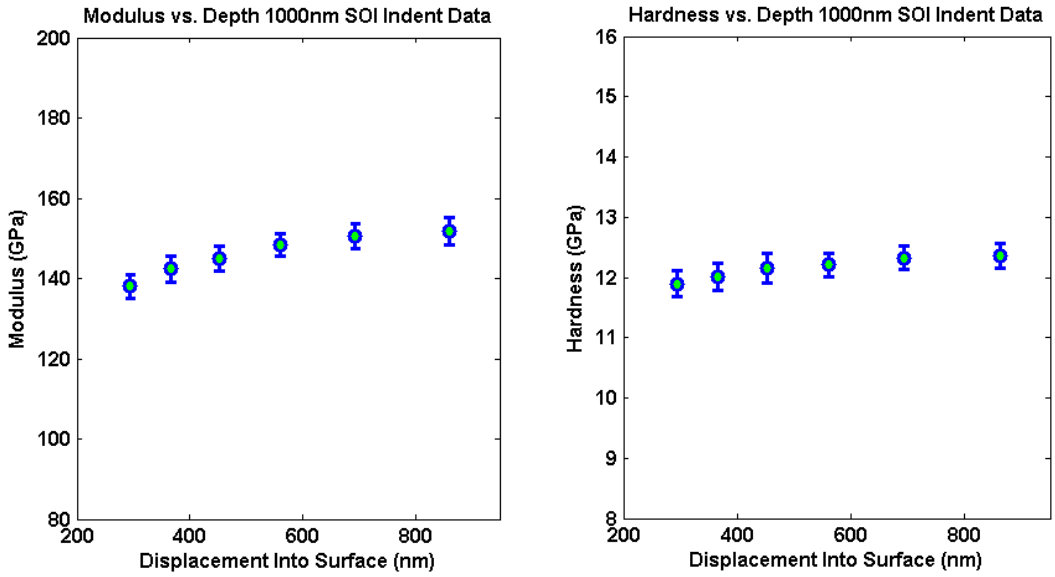

Figure 7. Bulk a) modulus and b) hardness obtained from deep SOI indents are shown above for literature comparison purposes.

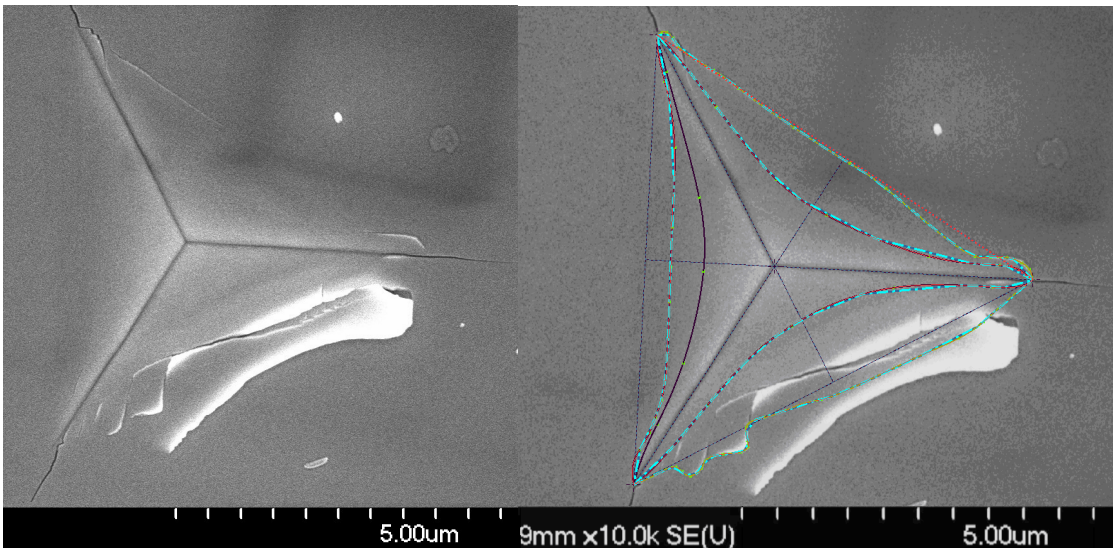

Figure 8. The images above show an example of a) SEM images of a 1000 nm indent, and b) lines are drawn around the same indent in (a) to demonstrate how the area was measured.

significant due to pile-up and sink-in, as seen in Fig. 7. Nevertheless, based on interpreting the SEM images of the indents, apart from potential systematic discrepancies, the hardness and moduli calculations using XP nanoindentation tester and imaging methods are found to correlate well [6].

CONCLUSION:

Using XP CSM Nanoindentation tester from MTS Nano Instruments we measured the properties of relaxed Silicon-on-Insulator (SOI) and bi-axially tensile strained Silicon-on-Insulator (sSOI) thin films of 600Å thickness. The reported moduli and hardness values for relaxed (SOI) and strained (sSOI) films are 105.6, 101.2 and 9.36, 9.23 GPa respectively. The bi-axial tensile strain in sSOI films tends to lower the modulus as compared to the relaxed SOI films. From this preliminary test results, we conclude that the hardness and moduli values of thin single crystal Si films on amorphous SiO_2 are significantly different from known bulk Si values of 12.5 GPa and 160.0 GPa respectively. Further investigation of the substrate effect into the nanolayers composite will be performed.

REFERENCE:

1. T. Akatsu, J.M. Hartmann, A. Abbadie, C. Aulnette, Y.M. LeVaillant, D. Rouchon, Y. Bogumilovicz, L. Portigliatti, C. Colnat, N. Boudou, F. Lallement, F. Triolet, Ch. Figuet, M. Martinez, P. Nguyen, C. Delattre, K. Tsyganenko, B. Berne, F. Allibert Ch. Deguet, M. Kennard, E. Guiot, F. Metral and I. Cayrefourcq ; ECS Transactions, Vol. 3, No (6), (2006), pp. 107 – 117
2. C. Mazure and A.J. Auberton-Herve, Proc. of 35th European Solid-State Device Research Conf. ESSDERC (2005), pp. 29
3. B.Y. Nguyen et al., Solid State Technology (2006), pp. 41
4. H. Yin et al., Symp. on VLSI Tech., Dig. of Tech. Papers, (2004), pp. 76
5. W.C. Oliver and G.M. Pharr, J. Mater. Res. 7, 1564 (1992).
6. A.A. Elmustafa and D.S. Stone, J. Mech. Phys. Solids, 2003, 51, 357.