

Chapter 4

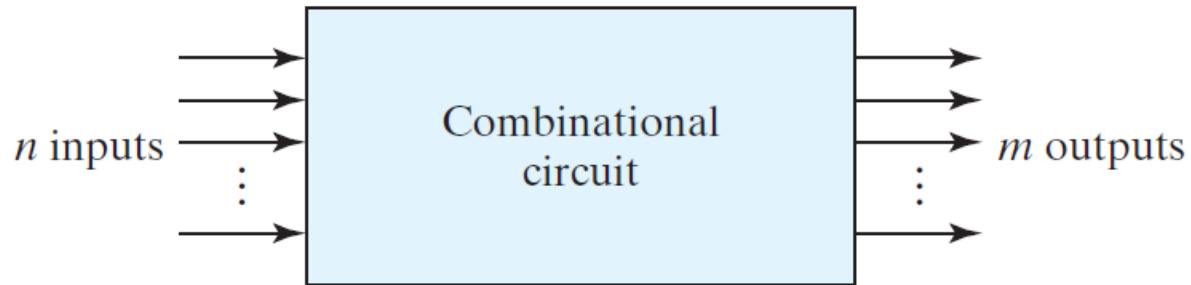
Combinational Logic

Switching Theory

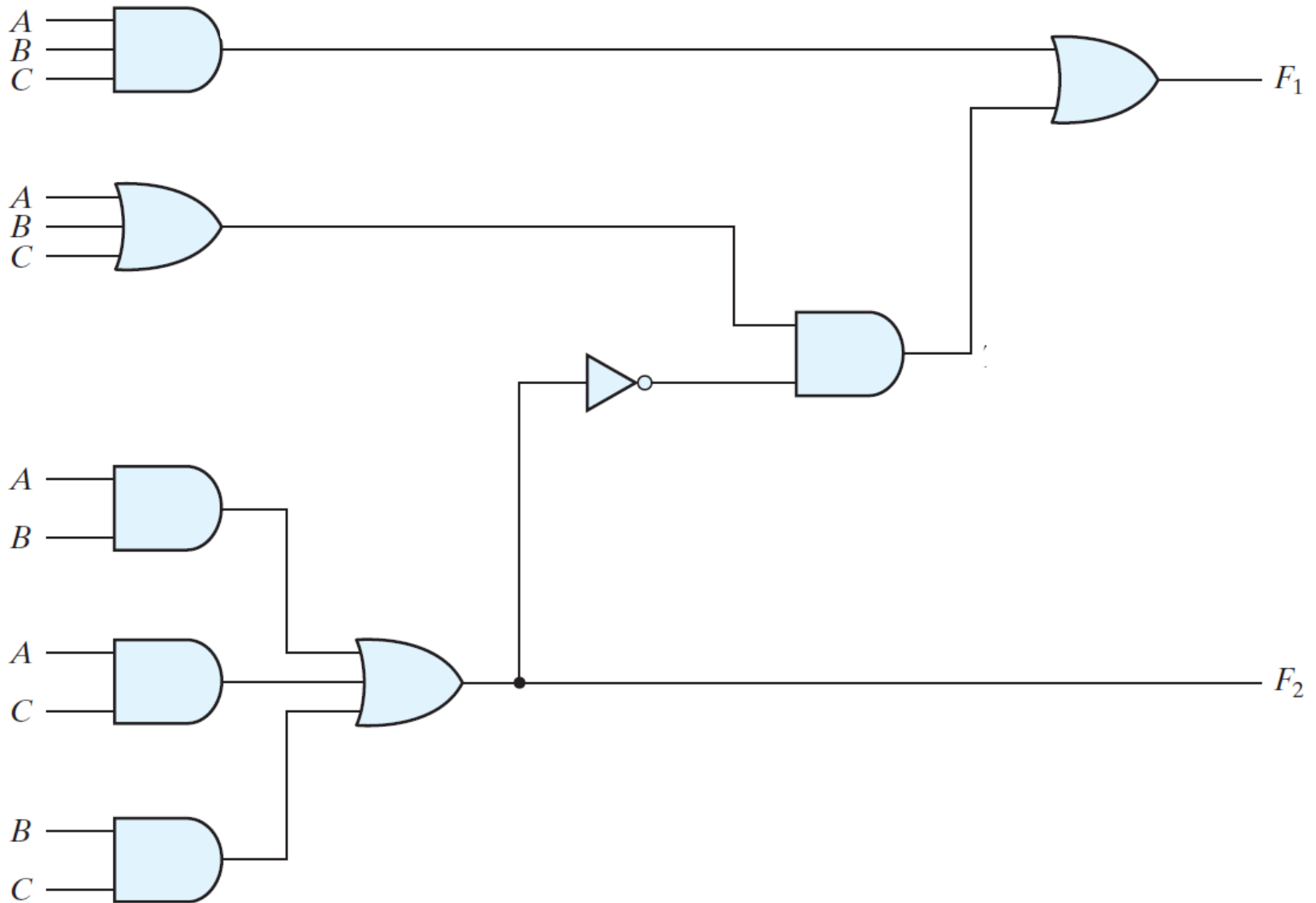
Introduction

- Two Types of Logic Circuits
 - Combinational Logic
 - Sequential Logic

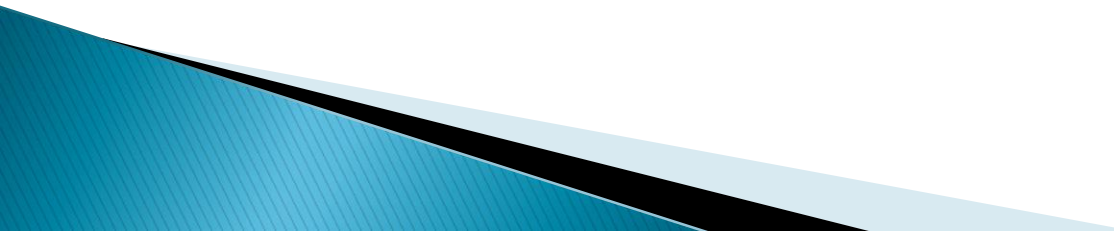
Combinational Circuit



Analysis Procedure



Design Procedure

1. From the specifications of the circuit, determine the required number of inputs and outputs and assign a symbol to each.
 2. Derive the truth table that defines the required relationship between inputs and outputs.
 3. Obtain the simplified Boolean functions for each output as a function of the input variables.
 4. Draw the logic diagram and verify the correctness of the design (manually or by simulation).
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Half-Adder

Table 4.3

Half Adder

| <i>x</i> | <i>y</i> | <i>c</i> | <i>s</i> |
|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

Full Adder

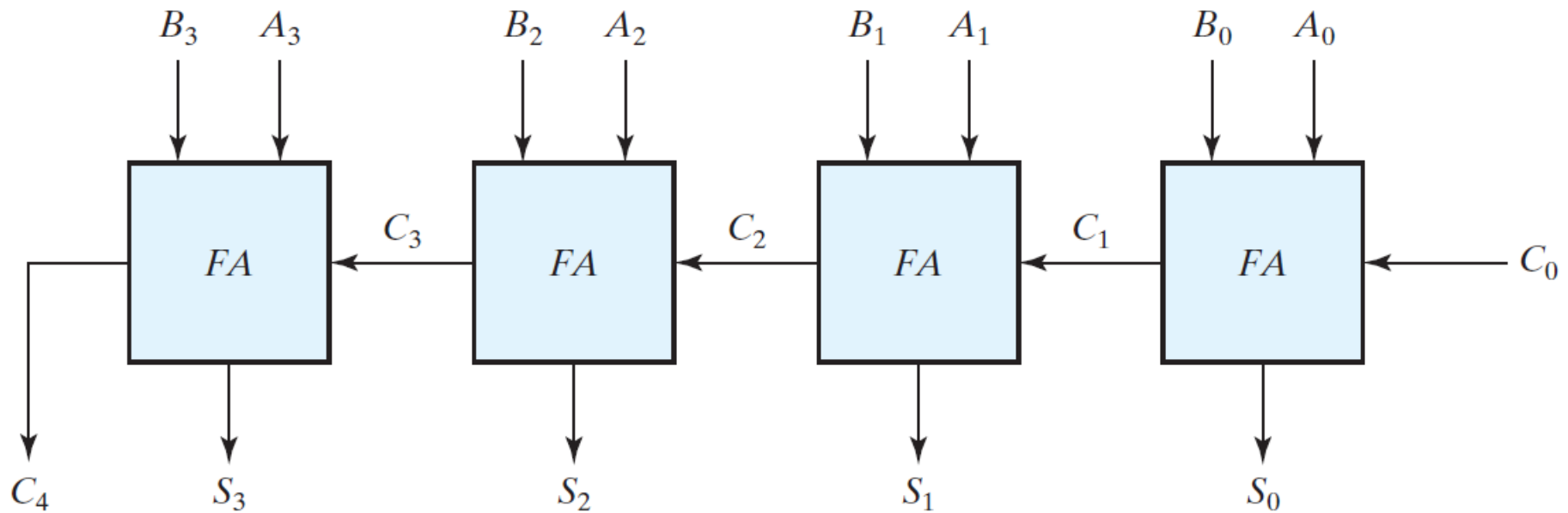
Table 4.4
Full Adder

| <i>x</i> | <i>y</i> | <i>z</i> | <i>C</i> | <i>S</i> |
|-----------------|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

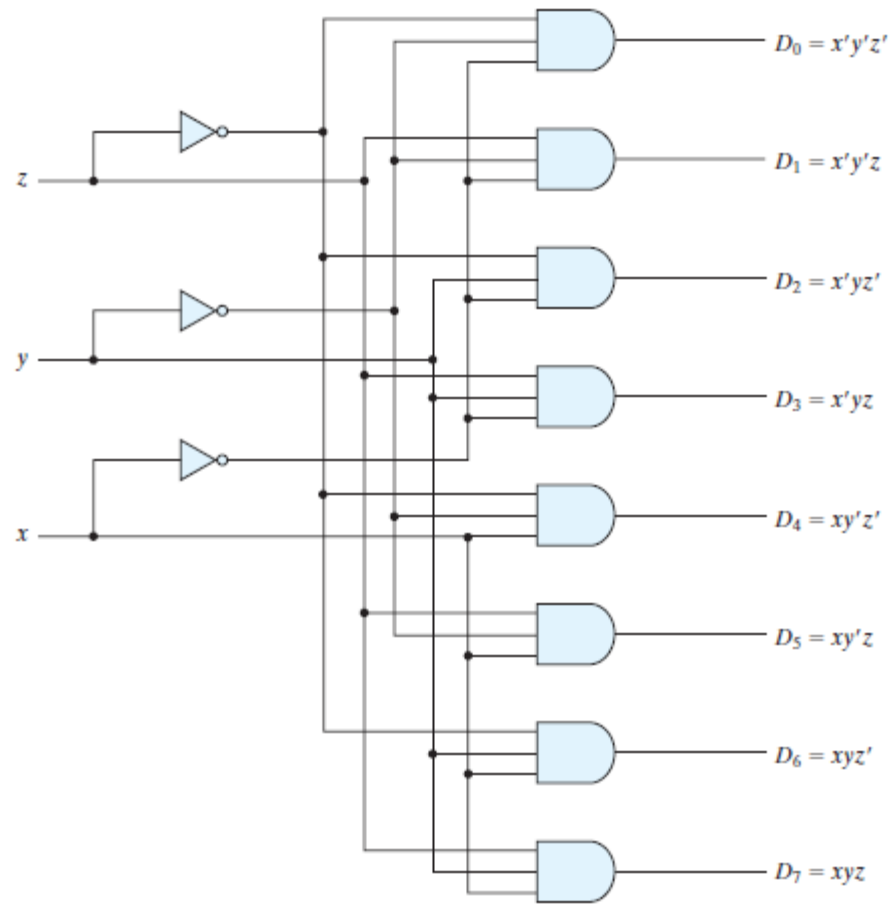
Binary Adder

| Subscript i: | 3 | 2 | 1 | 0 | |
|----------------------------------|----------|----------|----------|----------|-----------|
| Input carry | 0 | 1 | 1 | 0 | C_i |
| Augend | 1 | 0 | 1 | 1 | A_i |
| Addend | 0 | 0 | 1 | 1 | B_i |
| Sum | 1 | 1 | 1 | 0 | S_i |
| Output carry | 0 | 0 | 1 | 1 | C_{i+1} |

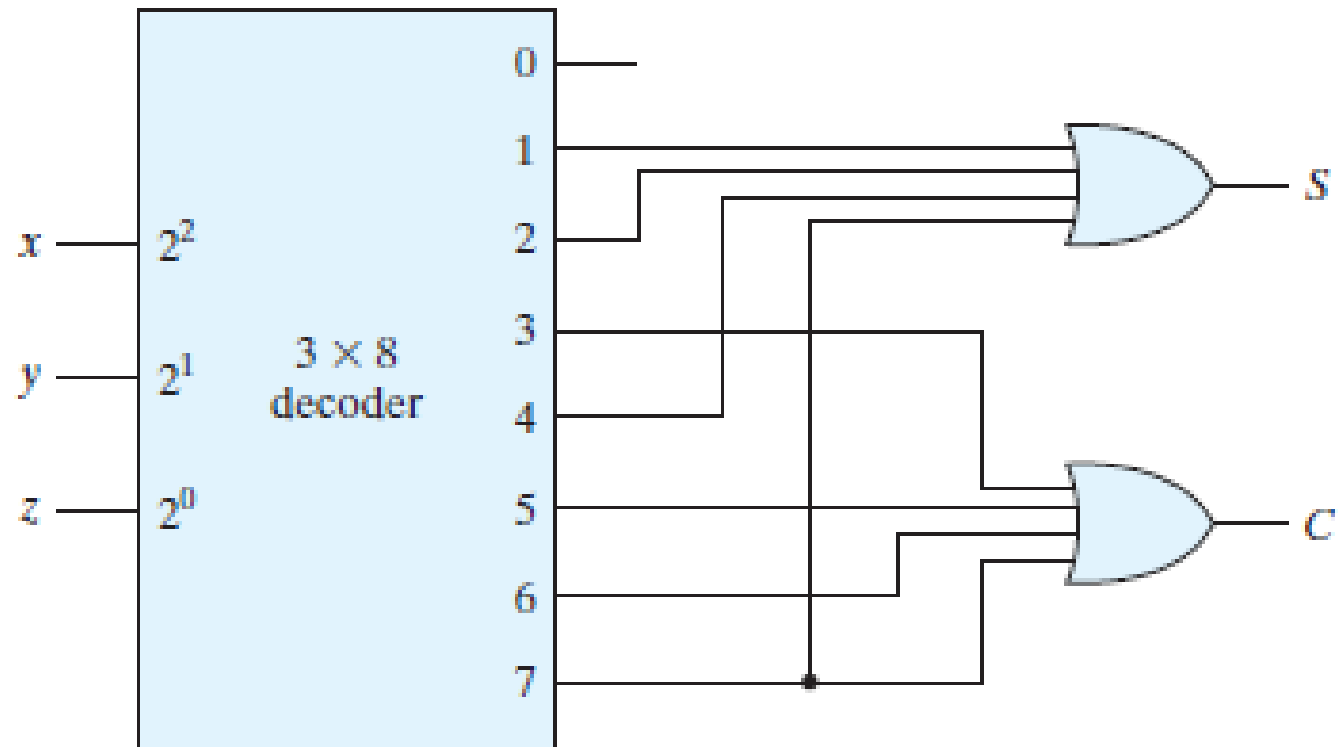
Binary Adder



Decoder



Decoder

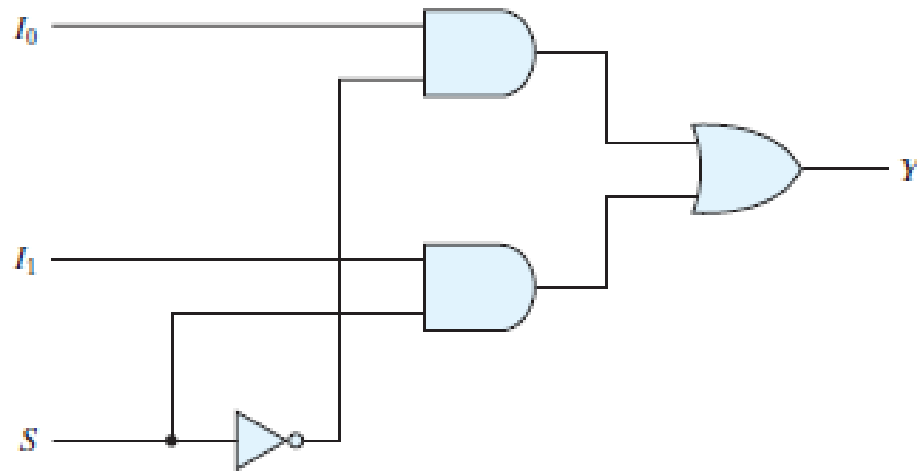


Encoder

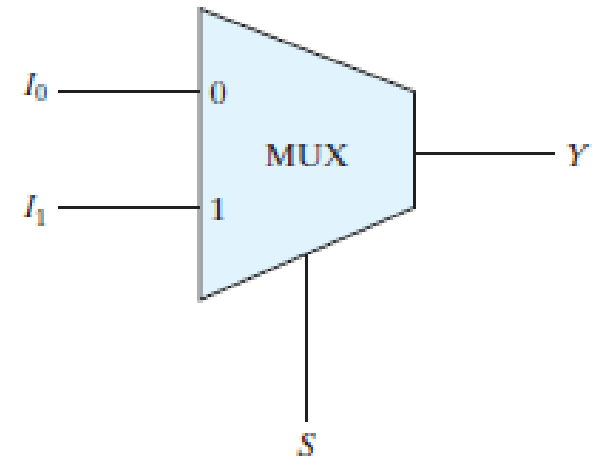
Table 4.7
Truth Table of an Octal-to-Binary Encoder

| Inputs | | | | | | | | Outputs | | |
|--------|-------|-------|-------|-------|-------|-------|-------|---------|-----|-----|
| D_0 | D_1 | D_2 | D_3 | D_4 | D_5 | D_6 | D_7 | x | y | z |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | |

Multiplexer



(a) Logic diagram



(b) Block diagram

Others

| Input BCD | | | | | | | |
|------------------|----------|----------|----------|----------|----------|----------|----------|
| <i>A</i> | <i>B</i> | <i>C</i> | <i>D</i> | <i>w</i> | <i>x</i> | <i>y</i> | <i>z</i> |
| 0 | 0 | 0 | 0 | | | | |
| 0 | 0 | 0 | 1 | | | | |
| 0 | 0 | 1 | 0 | | | | |
| 0 | 0 | 1 | 1 | | | | |
| 0 | 1 | 0 | 0 | | | | |
| 0 | 1 | 0 | 1 | | | | |
| 0 | 1 | 1 | 0 | | | | |
| 0 | 1 | 1 | 1 | | | | |
| 1 | 0 | 0 | 0 | | | | |
| 1 | 0 | 0 | 1 | | | | |

Others

| Input BCD | | | | | | | |
|------------------|----------|----------|----------|----------|----------|----------|----------|
| <i>A</i> | <i>B</i> | <i>C</i> | <i>D</i> | <i>w</i> | <i>x</i> | <i>y</i> | <i>z</i> |
| 0 | 0 | 0 | 0 | | | | |
| 0 | 0 | 0 | 1 | | | | |
| 0 | 0 | 1 | 0 | | | | |
| 0 | 0 | 1 | 1 | | | | |
| 0 | 1 | 0 | 0 | | | | |
| 0 | 1 | 0 | 1 | | | | |
| 0 | 1 | 1 | 0 | | | | |
| 0 | 1 | 1 | 1 | | | | |
| 1 | 0 | 0 | 0 | | | | |
| 1 | 0 | 0 | 1 | | | | |

Quiz 4

Design a logical circuit with minimum number of gates to count the number of zeros in the input BCD code.

| Input BCD | | | |
|-----------|----------|----------|----------|
| <i>A</i> | <i>B</i> | <i>C</i> | <i>D</i> |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |