Chapter 5

Sequential Logic (1/2)

Switching Theory

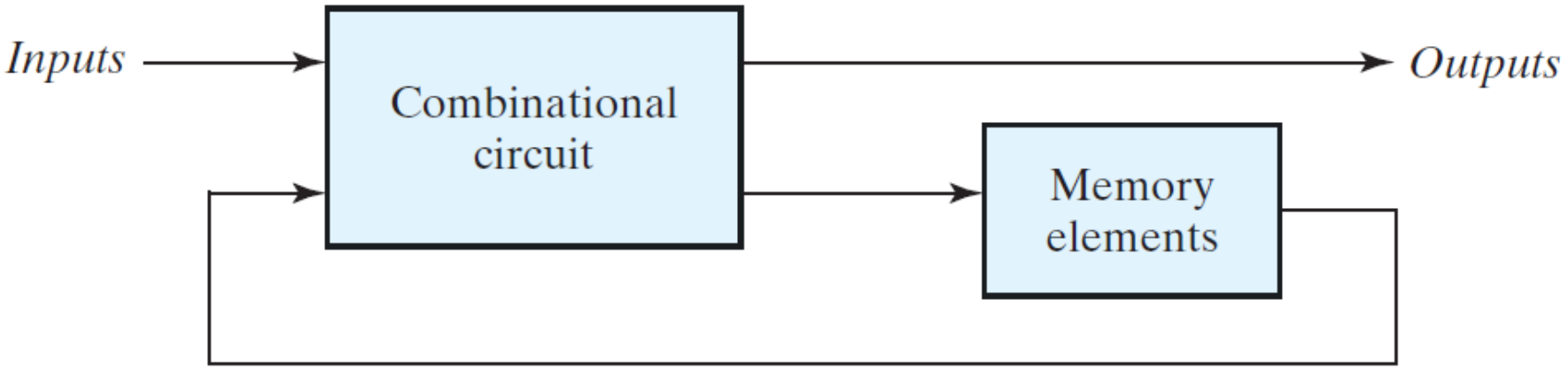
Emad Felemban

Introduction

- Two Types of Logic Circuits
  - Combinational Logic
  - Sequential Logic

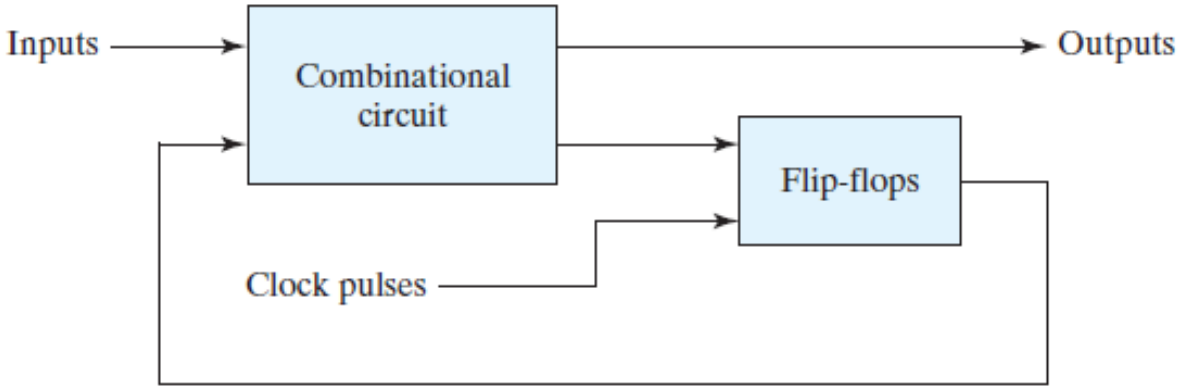
  A sequential circuit is specified by a time sequence of inputs, outputs and internal states

Sequential Circuit



Sequential Circuit

- Two types of Sequential Circuits
  - Synchronous → Timed with a Clock Generator
  - Asynchronous → Affected by change in input signals



(a) Block diagram

(b) Timing diagram of clock pulses

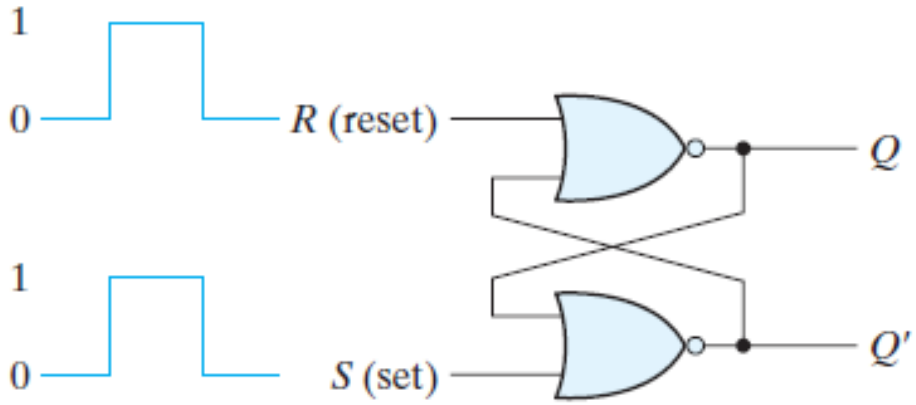
Clock Response

(a) Response to positive level

(b) Positive-edge response

(c) Negative-edge response

Storage Elements : SR Latch



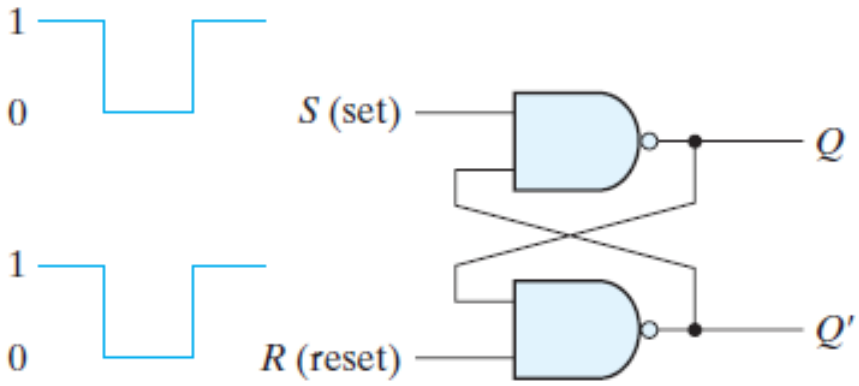
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

FIGURE 5.3
SR latch with NOR gates

Storage Elements : SR Latch



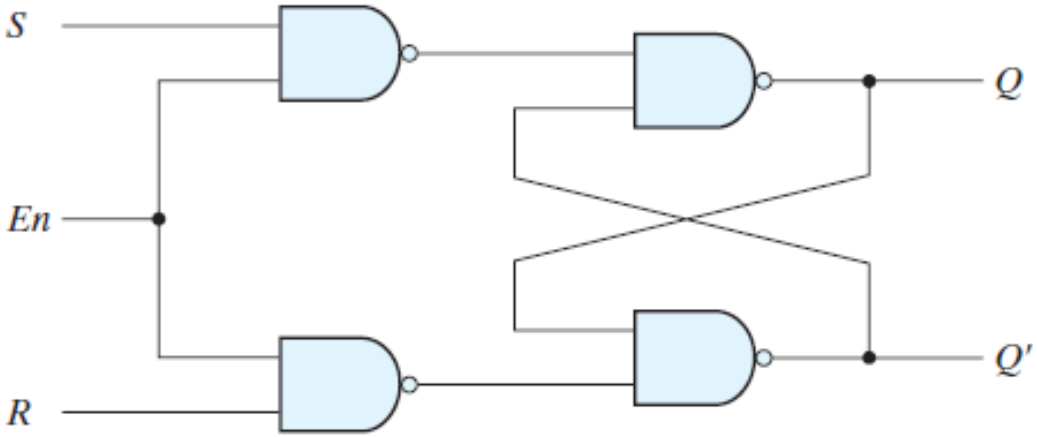
(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

FIGURE 5.4
SR latch with NAND gates

Storage Elements : SR Latch



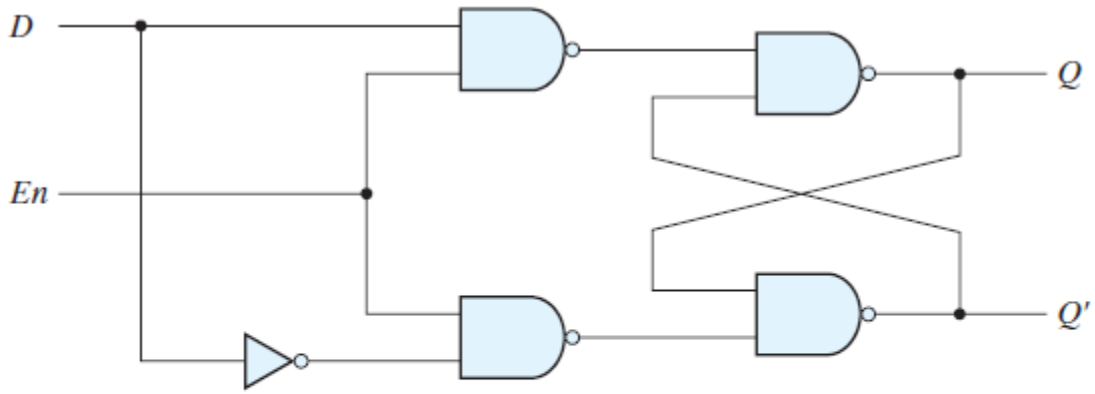
(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

FIGURE 5.5
SR latch with control input

Storage Element : D Latch



(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

FIGURE 5.6
D latch

Graphics Symbols for Latches

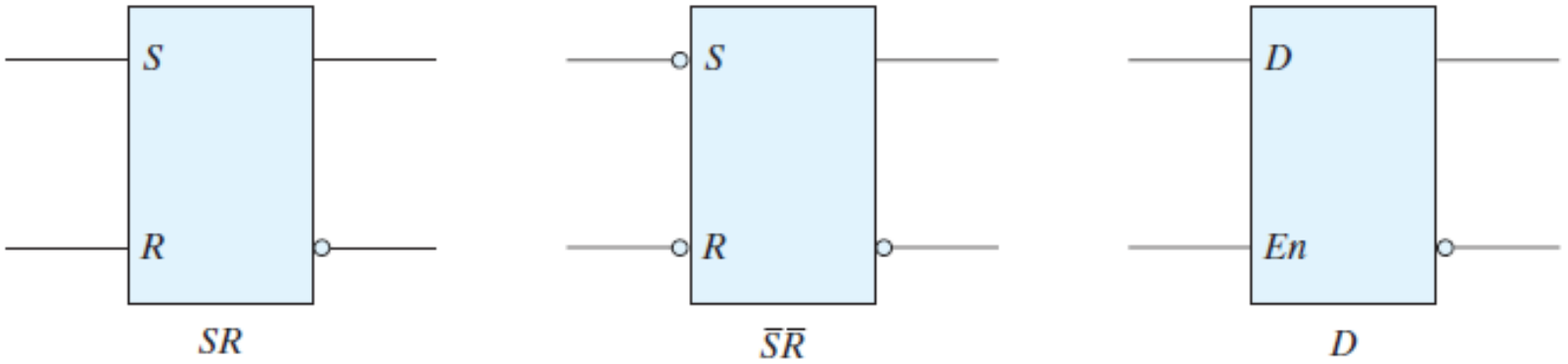
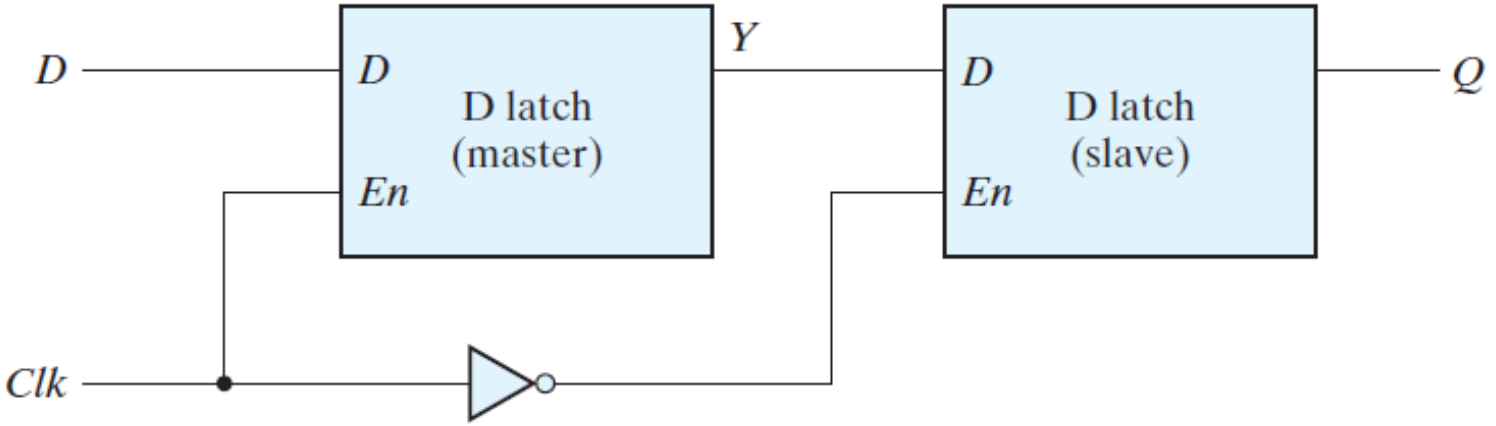
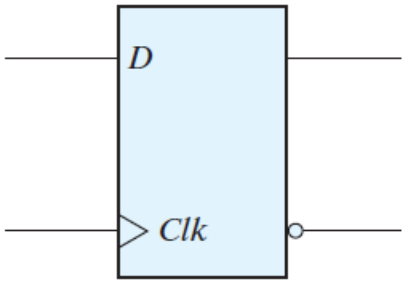


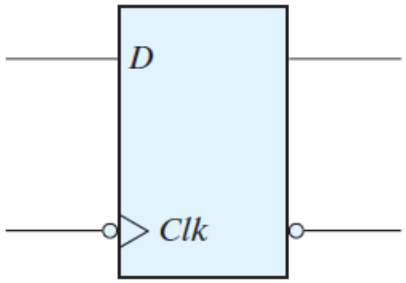
FIGURE 5.7
Graphic symbols for latches

Storage Element : Flip-Flop





(a) Positive-edge

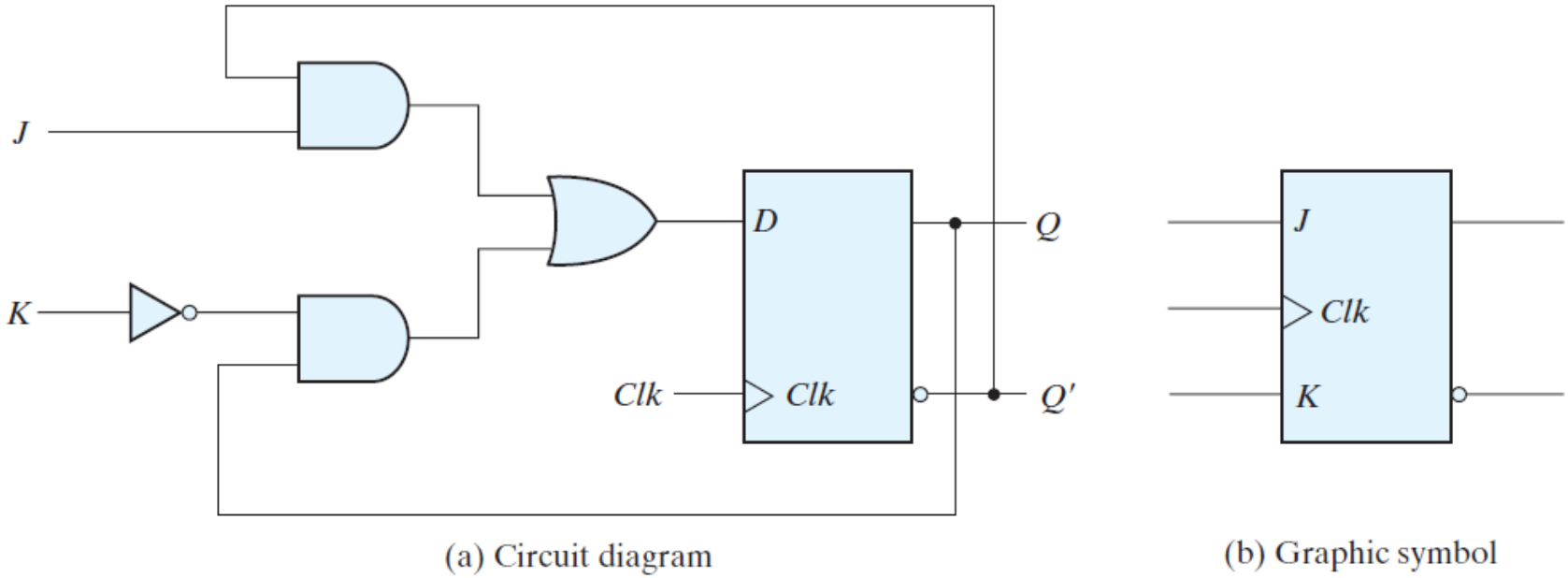


(a) Negative-edge

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

JK Flip-Flop



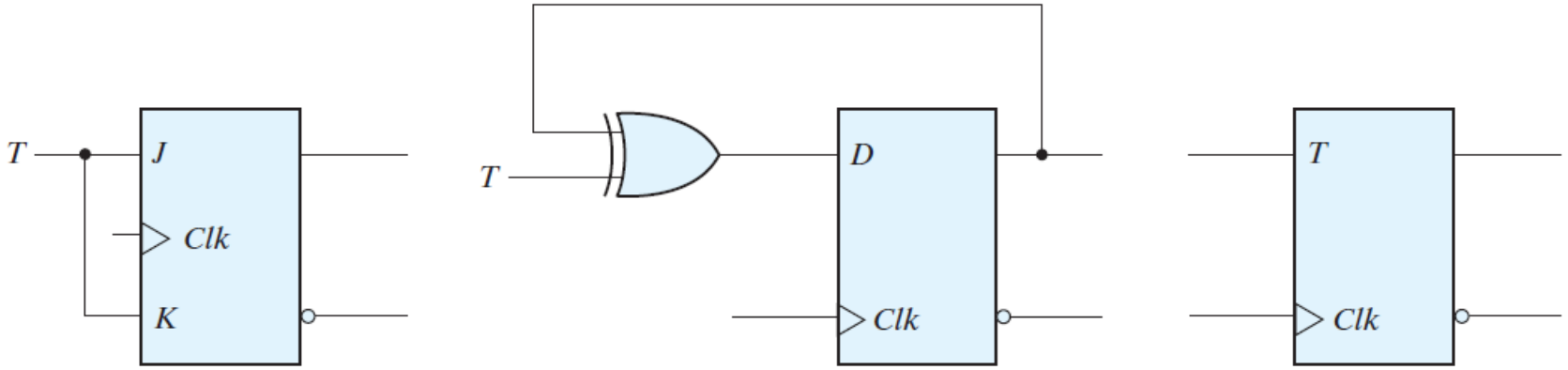
(a) Circuit diagram (b) Graphic symbol

FIGURE 5.12
JK flip-flop

Table 5.1
Flip-Flop Characteristic Tables

***JK* Flip-Flop**			
J	***K***	***Q*(*t* + 1)**	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

T Flip–Flop



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

FIGURE 5.13
T flip-flop

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Characteristic Equations

The logical properties of a flip-flop, as described in the characteristic table, can be expressed algebraically with a characteristic equation. For the D flip-flop, we have the characteristic equation

$$Q(t + 1) = D$$

which states that the next state of the output will be equal to the value of input D in the present state. The characteristic equation for the JK flip-flop can be derived from the characteristic table or from the circuit of Fig. 5.12. We obtain

$$Q(t + 1) = JQ' + K'Q$$

where Q is the value of the flip-flop output prior to the application of a clock edge. The characteristic equation for the T flip-flop is obtained from the circuit of Fig. 5.13:

$$Q(t + 1) = T \oplus Q = TQ' + T'Q$$