



Description

The GM76C256C family is a 262,144 bits static random access memory organized as 32,768 words by 8 bits. Using a 0.6 μ m advanced CMOS technology and operated a single 5.0V supply.

Advanced circuit techniques provide both high speed and low power consumption. The Family can support various operating temperature ranges for user flexibility of system design.

The Family has Chip select /CS, which allows for device selection and data retention control, and output enable (/OE), which provides fast memory access. Thus it is suitable for high speed and low power applications, particularly where battery back-up is required.

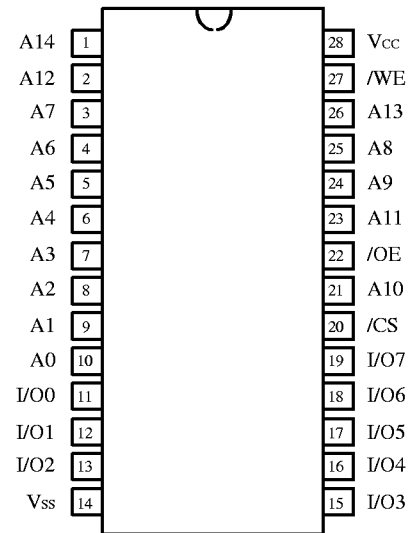
Features

- * High Speed : Fast Access and Cycle Time
55/70ns Max
- * Low Power Standby and Low Power Operation
 - Standby : 165 μ W at $T_A = -25 \sim 85^\circ\text{C}$ (LLE)
 - 110 μ W at $T_A = 0 \sim 70^\circ\text{C}$ (LL)
 - Operation : 385mW at $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$
- * Completely Static RAM : No Clock or Timing strobe required
- * Power Supply Voltage : $5.0\text{V} \pm 0.5\text{V}$
- * Low Data Retention Voltage : 2.0V (Min)
- * Temperature Range
 - GM76C256CL/LL : ($0 \sim 70^\circ\text{C}$)
 - GM76C256CLE/LLE : ($-25 \sim 85^\circ\text{C}$)
- * Package Type : JEDEC Standard
28-DIP, SOP, TSOP(I)

Pin Description

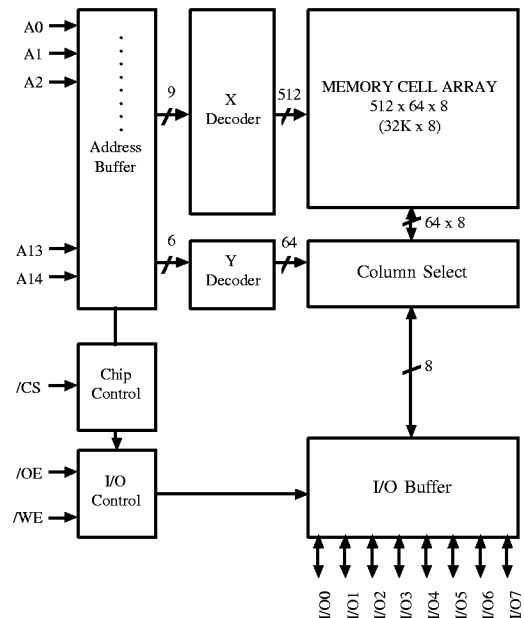
Pin	Function
A0-A14	Address Inputs
/WE	Write Enable Input
/OE	Output Enable Input
/CS	Chip Select Input
I/O0-I/O7	Data Input/Output
V _{CC}	Power Supply
V _{SS}	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings ^{*1}

Symbol	Parameter		Rating	Unit
T _A	Ambient Temperature under Bias	GM76C256CL/LL	0 ~ 70	C
		GM76C256CLE/LLE	-25 ~ 85	C
T _{STG}	Storage Temperature		-65 ~ 150	C
V _{SOL}	Soldering Temperature and Time		260, 10 (at lead)	C, S
V _{CC}	Supply Voltage		-0.3 ~ 4.6	V
V _{IN}	Input Voltage		-0.3 ^{*2} ~ 4.6	V
V _{IO}	Input and Output Voltage		-0.5 ~ V _{CC} + 0.5	V
P _D	Power Dissipation		1.0	W

Notes:

1. Operation at above Absolute Maximum Ratings can adversely affect device reliability.
2. -3.0V at pulse width 50ns Max.

Recommended DC Operating Conditions (T_A = -25 ~ 85C)

Symbol	Parameter	GM76C256C			Unit
		Min	Typ	Max	
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3*	-	0.8	V

*Note: V_{IL}=-3.0V Min for pulse width less than 50ns.

Truth Table

/CS	/WE	/OE	Input/Output	MODE
H	X	X	Hi-Z	Not Selected
L	H	L	Output Data	Read
L	L	X	Input Data	Write
L	H	H	Hi-Z	Output Disable

*Note: X means "don't care".

DC Electrical Characteristics ($V_{CC}=5.0V \pm 0.5V$, $T_A = -25 \sim 85^\circ C$)

Symbol	Parameter	Test Conditions	GM76C256C			Unit
			Min	Typ	Max	
$I_{I(L)}$	Input Leakage Current	$V_{IN} = 0 \text{ to } V_{CC}$	-1	-	1	μA
$I_{O(L)}$	Output Leakage Current	$/CS = V_{IH} \text{ or } /OE = V_{IH} \text{ or } /WE = V_{IL}, V_{\leq} V_{OUT} \leq V_{CC}$	-1	-	1	μA
V_{OH}	High Level Output Voltage	$I_{OH} = -1.0mA$	2.4	-	-	V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2.1mA$	-	-	0.4	V
I_{CC}	Operating Supply Current	$/CS = V_{IL}, V_{IN} = V_{IH}/V_{IL}, I_{IO} = 0mA$	-	-	10	mA
I_{CC1}	Average Operating Current	$/CS = V_{IL}, V_{IN} = V_{IH}/V_{IL}, I_{IO} = 0mA$ tcycle = Min, cycle	-	-	70	mA
I_{CC2}	Average Operating Current	$/CS = V_{IL}, V_{IN} = V_{IH}/V_{IL}, I_{IO} = 0mA$ tcycle = 1 μs , cycle	-	-	10	mA
I_{CCS1}	Standby Current (TTL)	$/CS = V_{IH}$	-	-	1.0	mA
I_{CCS2}	Standby Current (CMOS)	$/CS \leq V_{CC}-0.2V(LL)$	0 to +70°C(LL)		20	μA
			-25 to +85°C(LLE)		30	μA
		$/CS \leq V_{CC}-0.2V(L)$	0 to +70°C(L)		40	μA
			-25 to +85°C(LE)		60	μA

*TYP. Values are measured at 25°C, $V_{CC} = 5.0V$

AC Operating Characteristics ($V_{CC}=5.0V \pm 0.5V$, $T_A = -25 \sim 85^\circ C$)

Read Cycle

Symbol	Parameter	Condi- tions	GM76C256C-55		GM76C256C-70		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	55	-	70	-	ns
t_{AA}	Address Access Time		-	55	-	70	ns
t_{ACS}	Chip Select Access Time		-	55	-	70	ns
t_{OE}	Output Enable Access Time		-	25	-	30	ns
t_{OH}	Output Hold Time		10	-	10	-	ns
t_{CLZ}	Chip Selection to Output in Low-Z	*2	10	-	10	-	ns
t_{OLZ}	Output Disable to Output in Low-Z		5	-	5	-	ns
t_{CHZ}	Chip Deselection to Output in High-Z		0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High-Z		0	20	0	25	ns

Write Cycle

Symbol	Parameter	Condi- tions	GM76C256C-55		GM76C256C-70		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	55	-	70	-	ns
t_{CW}	Chip Select to End of Write		45	-	60	-	ns
t_{AW}	Address Set-up Time to End of Write		45	-	60	-	ns
t_{AS}	Address Set-up Time		0	-	0	-	ns
t_{WP}	Write Pulse Width		40	-	50	-	ns
t_{WR}	Write Recovery Time		0	-	0	-	ns
t_{DW}	Data to Write Time Overlap		25	-	30	-	ns
t_{DH}	Data Hold Time		0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	*2	0	20	0	25	ns
t_{OW}	Output Active from End of Write		5	-	5	-	ns

*1 Test Conditions.

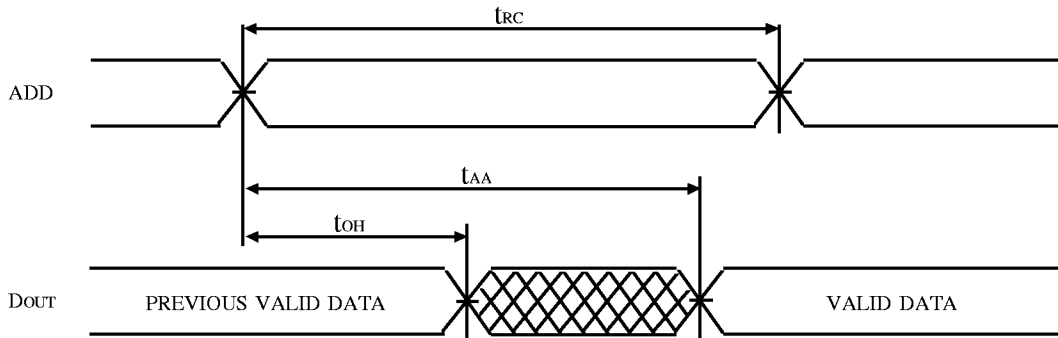
1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5ns$
3. Input/output timing reference level : 1.5V
4. Output load $C_L = 100pF + 1TTL$ Load

*2 Test Conditions.

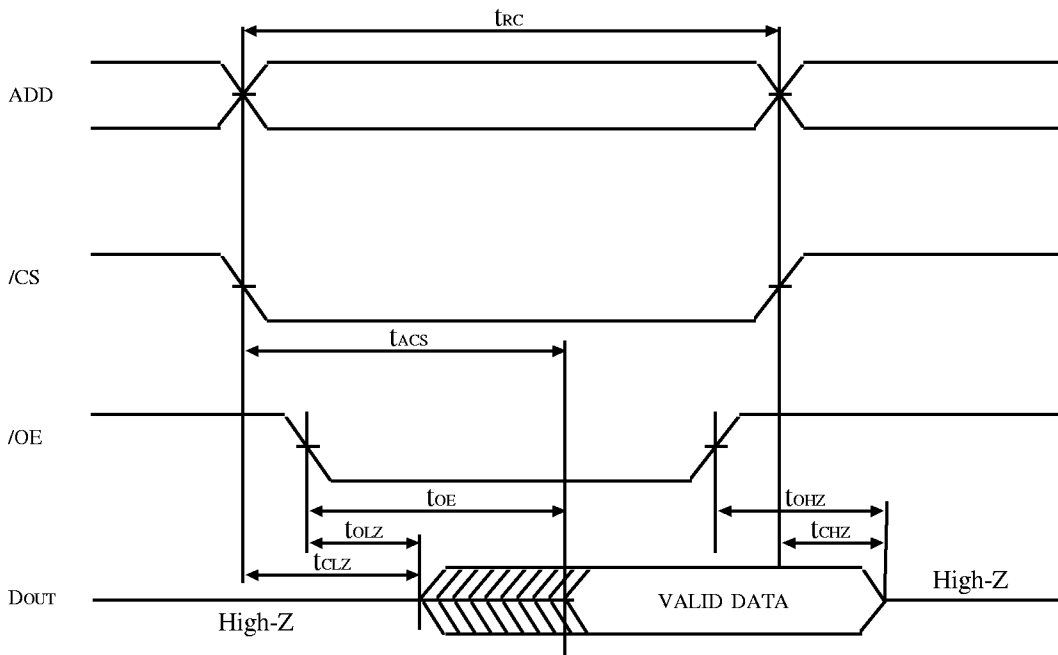
1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5ns$
3. Input timing reference level : 1.5V
4. Output timing reference level :
+/-200mV (the level displacement from
stable output voltage level)
5. Output load $C_L = 5pF + 1TTL$ Load

Timing Waveforms

Read Cycle 1 (Note 1, 2)



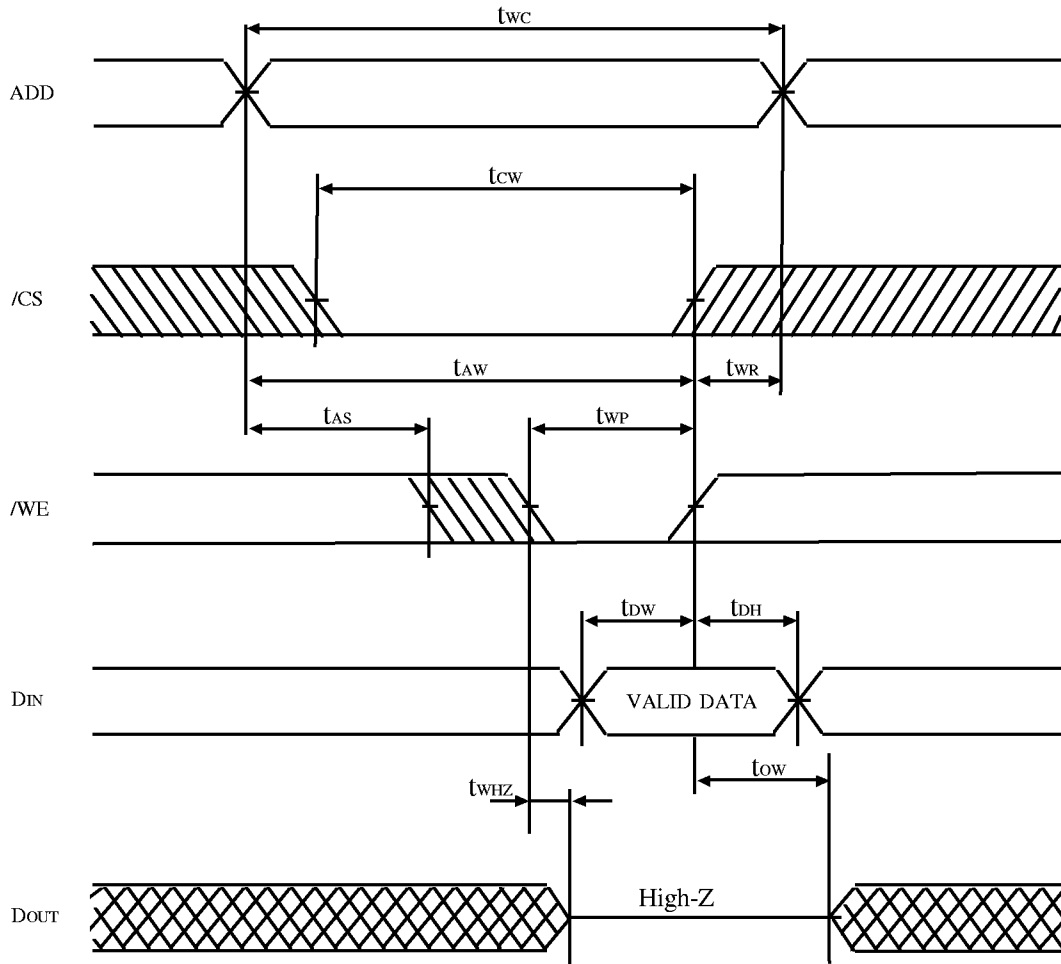
Read Cycle 2 (Note 2)



Notes:

1. Device is continuously selected. $/OE, /CS \leq V_{IL}$.
2. $/WE$ is high for read cycle.

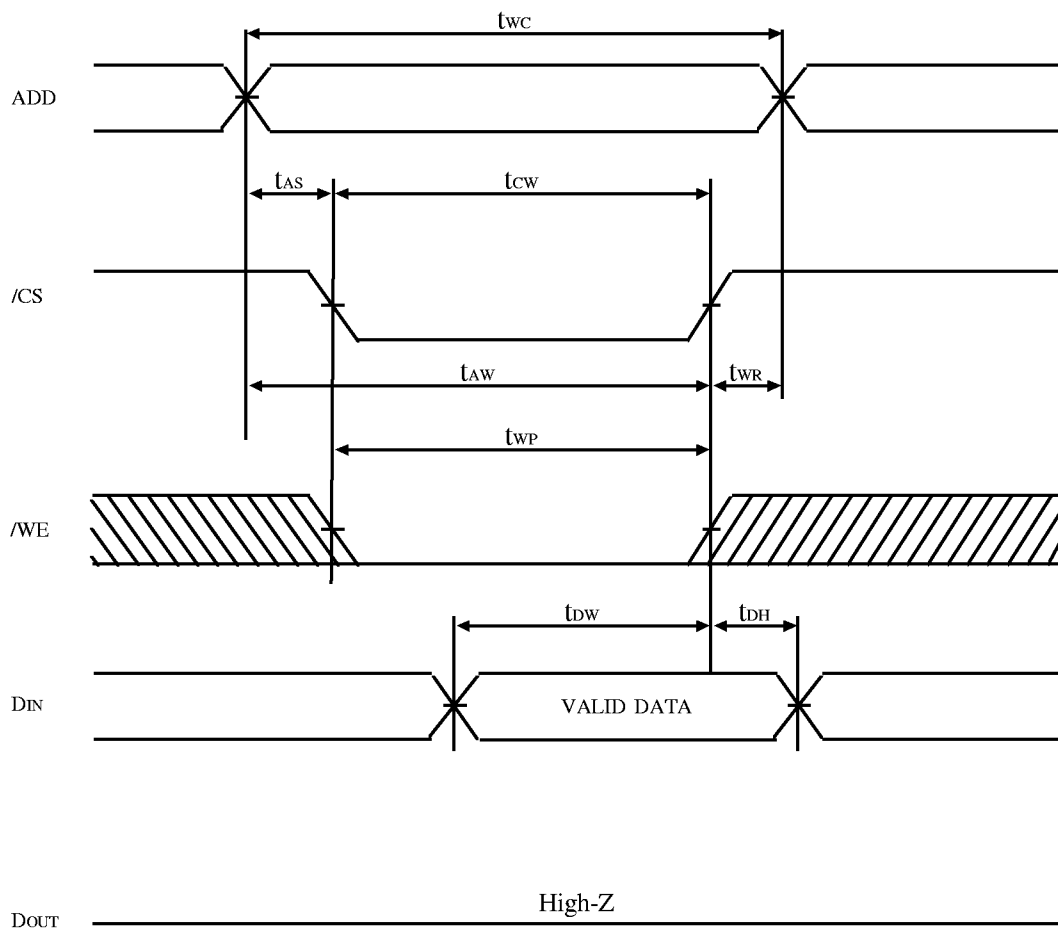
Write Cycle 1 (/WE Controlled) (Note 1, 2)



Notes:

1. The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}$ low and $\overline{\text{WE}}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.

Write Cycle 2 (/CS Controlled) (Note 1, 2, 3)



Notes:

1. The internal write time of the memory is defined by the overlap of /CS low and /WE low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if /OE = V_{IH} .
3. If /CS goes high simultaneously with /WE high, the output remains in a high impedance state.

Capacitance (f = 1MHz, T_A = 25C)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C _{IN}	Input Capacitance	V _I = 0V	-	6	pF
C _{OUT}	Output Capacitance	V _O = 0V	-	8	pF

*Note: This parameter is sampled and not 100% tested.

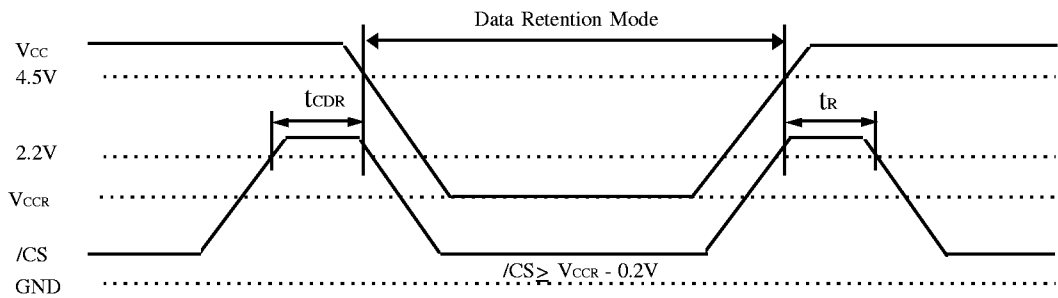
Data Retention Characteristics (T_A = -25 ~ 85C)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V _{CCR}	Data Retention Supply Voltage		/CS ≥ V _{CCR} - 0.2V	2.0	-	5.5	V
I _{CCR}	Data Retention Current	0 to +70C(LL)	V _{CC} = 3.0V /CS ≥ 2.8V	-	0.5 ^{*1}	7	uA
		-25 to +85C(LLE)		-	0.5 ^{*1}	10	
		0 to +70C(L)		-	1 ^{*1}	15	
		-25 to +85C(LE)		-	1 ^{*1}	20	
t _{CDR}	Chip Select to Data Retention Time		Refer to the figure below	0	-	-	ns
t _{tr}	Operation Recovery Time			5	-	-	ms

Notes:

1. Typ, Values are measured at 25C

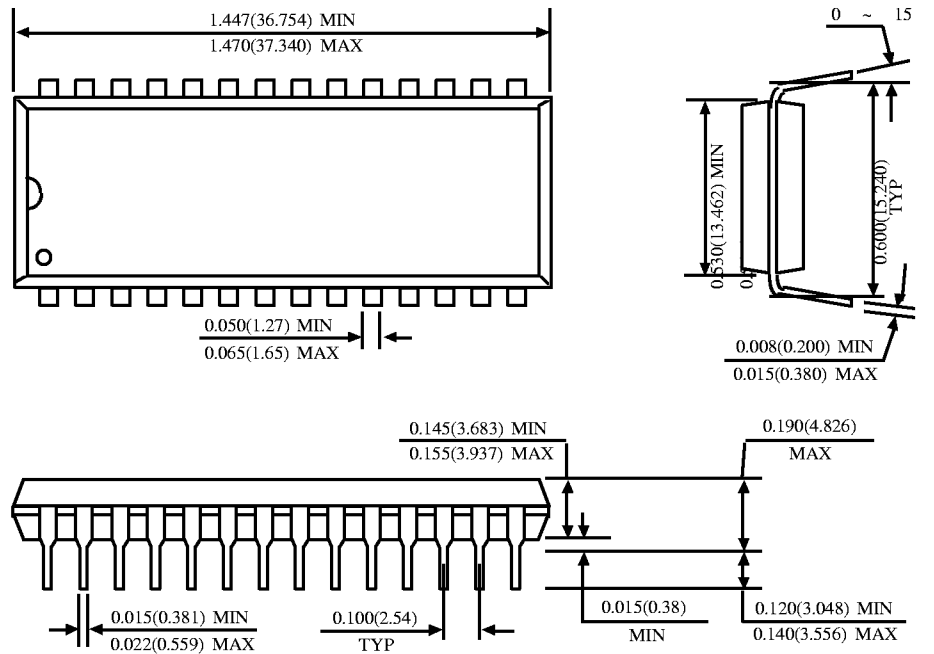
Data Retention Timing



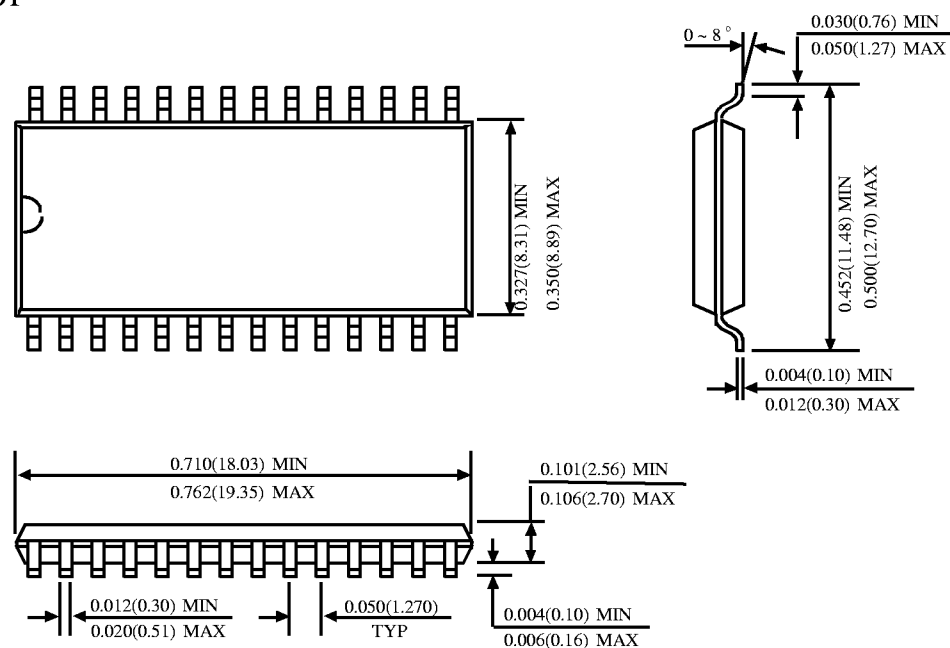
Note: When retaining data in standby mode, supply voltage can be lowered within a certain range.
Read or write cycle cannot be performed while the supply voltage is low.

Package Dimensions

Unit: Inches (mm)



28 SOP



Unit: Inches (mm)

28 TSOP-I

