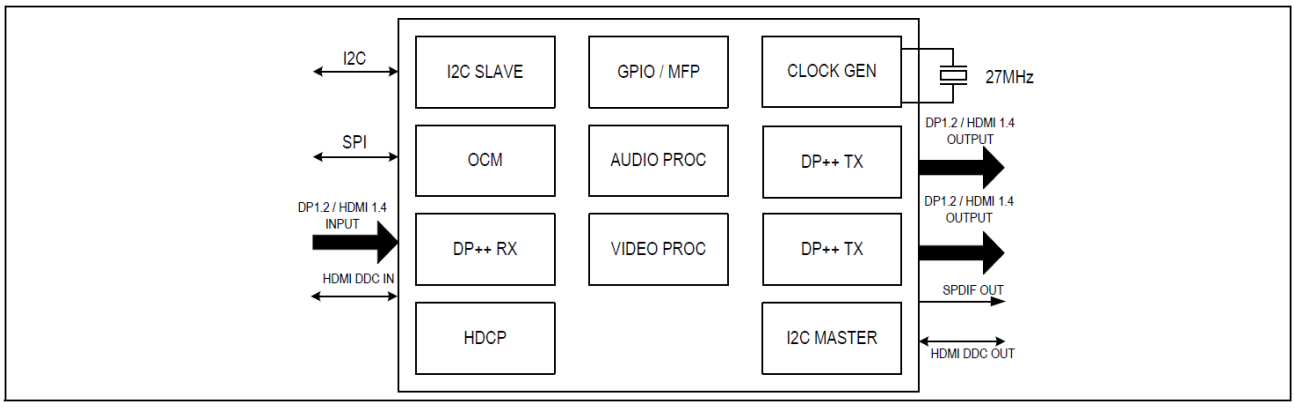
STDP4320
DisplayPort 1.2a Splitter

Features

- DisplayPort™ dual mode receiver
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - SST or MST (up to eight streams)
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - HPD out
  - HDMI/DVI operation (3.2 Gbps link rate)
  - Functions as eDP and MyDP receiver
- DisplayPort dual mode transmitters
  - Two transmitter ports
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - SST or MST (up to eight streams)
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - HPD in
  - HDMI/DVI operation (3.2 Gbps link rate) with external level translator
  - Functions as eDP transmitter
- SPDIF audio output
  - Two SPDIF port pins
  - 192 kHz/24 bits
  - Compressed/LPCM
- Conversion from DP SST to TMDS format and vice versa
- HDCP repeater with embedded keys
- AUX to I2C bridge for EDID/MCCS pass through
  - Maps on DDC ports
- Device configuration options
  - SPI Flash
  - I2C host interface
- Deep color support
  - RGB/YCC (4:4:4) – 16-bit color
  - YCC (4:2:2) – 16-bit color
- Spread spectrum on DisplayPort interface for EMI reduction
- Bandwidth
  - Video resolution up to 4K2K @ 60 Hz
  - Audio 7.1 Ch up to 192 kHz sample rate
- Low power operation
  - Standby 30 mW
- Package
  - 172 LFBGA (12 x 12 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Audio-video router for PC/notebooks, docking stations, hub, 4K2K TVs, daisy chain monitors, digital signage



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1. Description

The STDP4320 is a high-speed DisplayPort dual mode splitter IC targeted for audio-video de-multiplexing and routing in applications such as notebooks, docking stations, video hub, 4K2K TVs, daisy chainable monitors, digital signage, etc. It consists of one dual mode input port and two dual mode output ports configurable as either DisplayPort or HDMI/DVI. STDP4320 is a VESA DP Standard Ver. 1.2a compliant device that supports advanced features such as MST, HBR2, 3D formats and GTC assist. Designs based on STDP4320 have the flexibility to offer either DP or HDMI/DVI connectors on its end product to interface with legacy and new generation video sources and sinks. In addition, STDP4320-based products with a DisplayPort output connector are DP++ compliant and work with any HDMI or single link DVI sink through a passive level translator (dongle).

The STDP4320 uses Kinetic's latest generation DisplayPort dual mode receiver and transmitter technology that supports both DisplayPort and TMDS signal formats. This device receives MST format up to eight audio-video streams, which can be further routed on either of the two outputs in any combination of eight streams depending on the capability of downstream sinks. This device can also replicate the incoming video streams on both output ports simultaneously, thus allowing cloning on two downstream sinks. For example, a 4K2K 60 Hz video input is replicated on two output ports simultaneously. The DisplayPort receiver and transmitters support HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. In HDMI mode, this device supports link rates up to 3.2 Gbps corresponding to a pixel rate of 300 MHz, adequate for supporting video resolution up to FHD 120 Hz with all 3D formats. The device is also capable of delivering deep color video up to 16-bits per color. The STDP4320 allows audio transport from the source to the desired audio rendering devices over the video output port or through an SPDIF port.

The STDP4320 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. The STDP4320 features the HDCP 1.3 content protection scheme with embedded keys for secure transmission of protected audio-video content. It also operates as an HDCP repeater for the downstream sinks.

The DDC ports in the STDP4320 allow the upstream source to access EDID and transfer MCCS commands to downstream sinks when the physical ports are either HDMI or DVI type. If both the upstream source and downstream sinks are DP type, I2C transactions take place over the AUX CH. If one of them is a DP type and the other is either a HDMI or DVI type, STDP4320 converts the I2C over AUX message protocol to I2C commands and sends it on the DDC port.

The device has an on-chip microcontroller with SPI, UART, and I2C interface. The STDP4320 uses an external SPI Flash ROM for storing device configuration firmware. It has an I2C slave port for external host communication. Other system interface signals include general-purpose IO for source, sink communication, detection, monitoring, etc. When the downstream sink is disconnected, STDP4320 automatically turns off the inactive port for power saving purposes.

2. Application overview

Figure 1. STDP4320 in video hub application

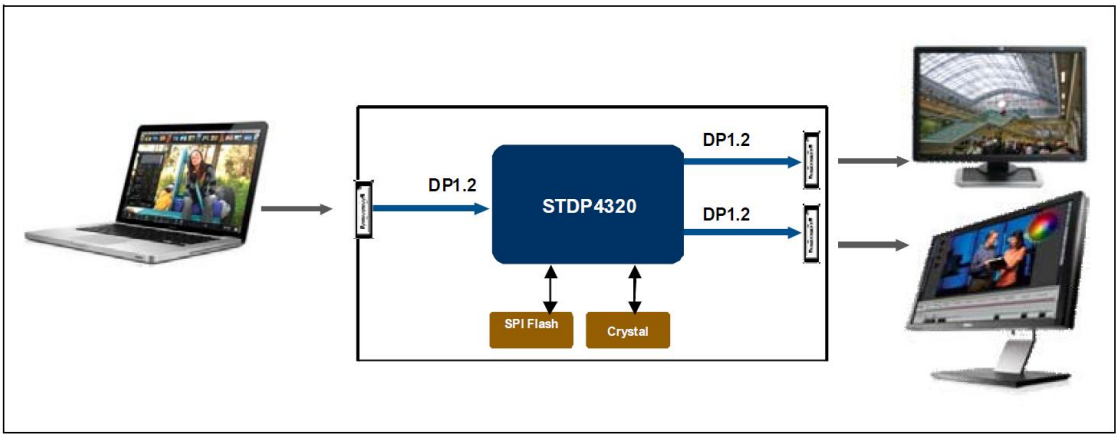
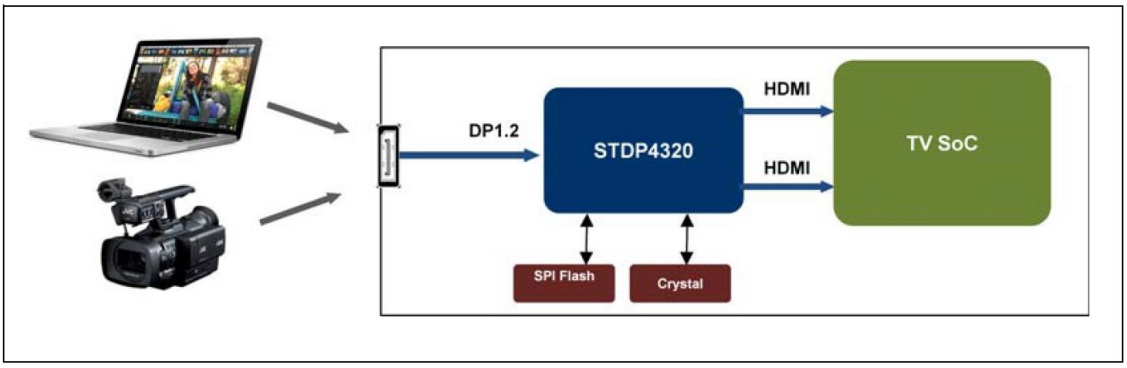


Figure 2. STDP4320 in 4K2K TV application



3. Feature attributes

3.1 Input interface

- Single DP++ interface featuring
  - DisplayPort Ver. 1.2a compliant receiver; supports eDP and MyDP
  - HDMI 1.4 compliant receiver
- Main link configuration
  - SST or MST (up to eight streams)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: 1 Mbps Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB, YCC422, or YCC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 3.2 Gbps/data pair max

3.2 Output interface

- Two DP++ interfaces featuring
  - AC coupled DisplayPort Ver. 1.2a compliant transmitter: supports eDP
  - AC coupled HDMI 1.4 transmitter
- DP main link configuration
  - SST or MST (up to eight streams)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB, YCC422, or YCC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 3.2 Gbps/data pair max

3.3 Supported video timings

- 4K2K 60 Hz: 24 bits/pixel in DP 1.2a configuration
- 1920 x 1080 (FHD) 240 Hz, 24 bits/pixel
- All 3D formats defined in DP 1.2a and HDMI 1.4 standards
- All standard CEA861 timing formats

3.4 Supported audio timings

- All audio formats as specified in DP 1.2a and HDMI 1.4 standards
- SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz (applicable in DP SST/HDMI output use case)

3.5 Control channel interfaces

- AUX CH, DDC, I2C host interface, and UART (UART for test/debug purposes only)

3.6 HDCP 1.3 support

- Key sets for DP/HDMI RX and DP/HDMI TX integrated in one-time programmable ROM (OTP)
- Standalone HDCP repeater capability

3.7 Package

- 172 LFBGA (12 x 12 mm), 0.8 ball pitch

3.8 Power supply voltages

- 3.3 V I/O; 1.2 V core

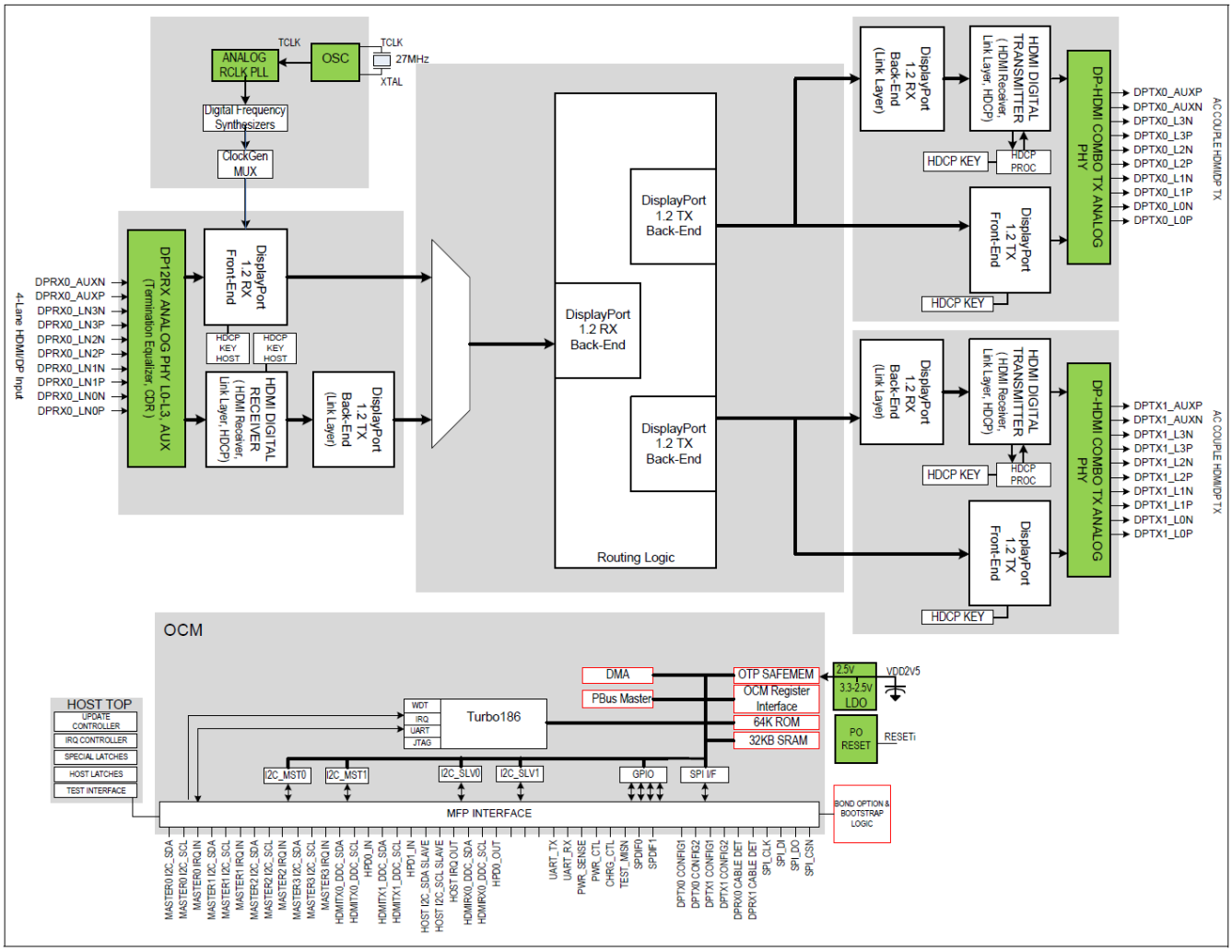
3.9 ESD

- 2 kV HBM, 450 V CDM

4. Functional block description

4.1 Block diagram

Figure 3. STDP4320 block diagram



4.2 Power sequence

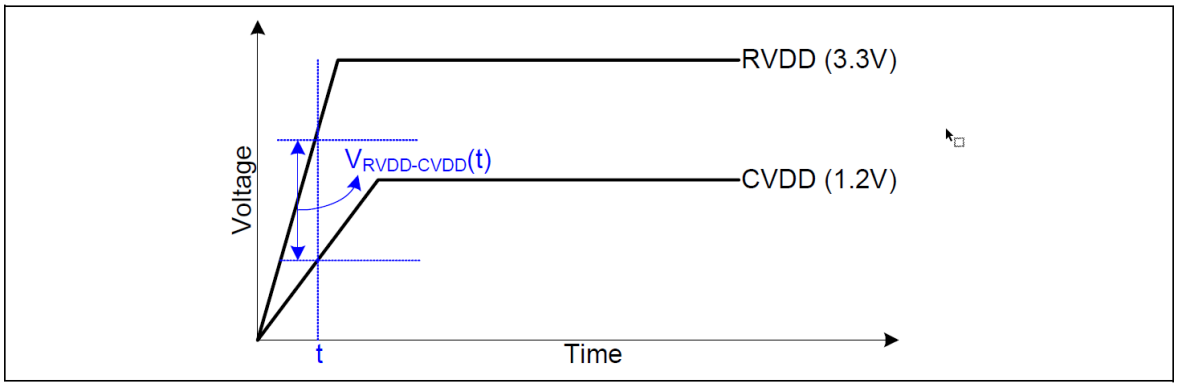
When using linear regulators for the 3.3 V and 1.2 V supplies, precautions must be taken in designing the power supply system to meet the following requirements.

At any time during the power-up sequence, the actual voltage of the 3.3 V ring VDD (RVDD) power supply should always be equal to or higher than the actual voltage of the 1.2 V core VDD (CVDD). In mathematical terms, VRVDD >= VCVDD at all times.

Table 1. Power sequencing requirements

Parameter	Min	Typ	Max
VRVDD-VCVDD (for all t>0)	0 V	1.50 V	

Figure 4. Correct power sequencing



4.3 Power-on reset

The STDP4320 device has an integrated reset pulse generator. The internal reset pulse generator performs hardware reset under the following conditions:

- During system power-up, after the RVDD_3V3 voltage has reached reset threshold voltage VT
- In the event RVDD_3V3 voltage drops below threshold VT for more than approximately 150 ns
- Manually holding the RESETn pin low for a minimum of 1 ms

The active-low reset pulse on the RESETn pin generated by the internal reset pulse generator is described in the table below. During the reset period, all internal circuits and logic are reset to the default power-on state. To ensure proper chip operation, TCLK (generated by crystal oscillator or from the external clock source) must be applied during and after the reset.

The following figure shows the relationship between RVDD_3V3 and RESETn during system power-up.

Figure 5. Power-on reset timings

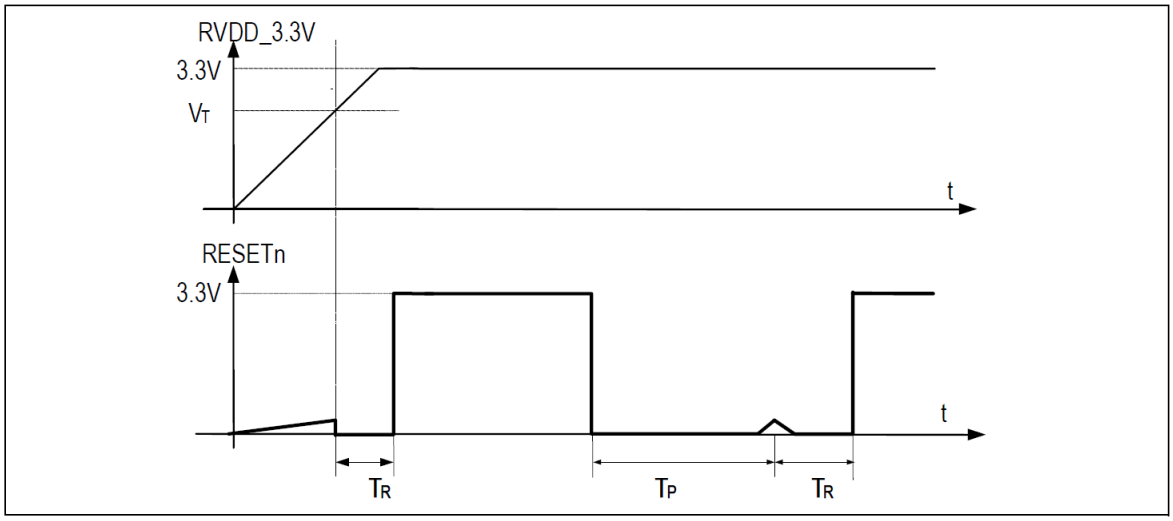


Table 2. Power-on reset characteristics

Description	Symbol	Min	Typ	Max
Power-on reset threshold voltage	V_T	2.60 V	2.70 V	2.80 V
Reset pulse duration	T_R	80 ms	100 ms	150 ms
Push-button hold time	T_P	1 ms	-	-

The glitch filter inside the internal reset pulse generator ignores the RVDD_3V3 power line glitch if the duration of the glitch is shorter than approximately 150 ns. However, if RVDD_3V3 voltage drops below the threshold V_T for more than 150 ns in duration, reset will be asserted and RESETn signal will go low. The following figure illustrates the RVDD_3V3 glitch.

Figure 6. RVDD_3V3 glitch

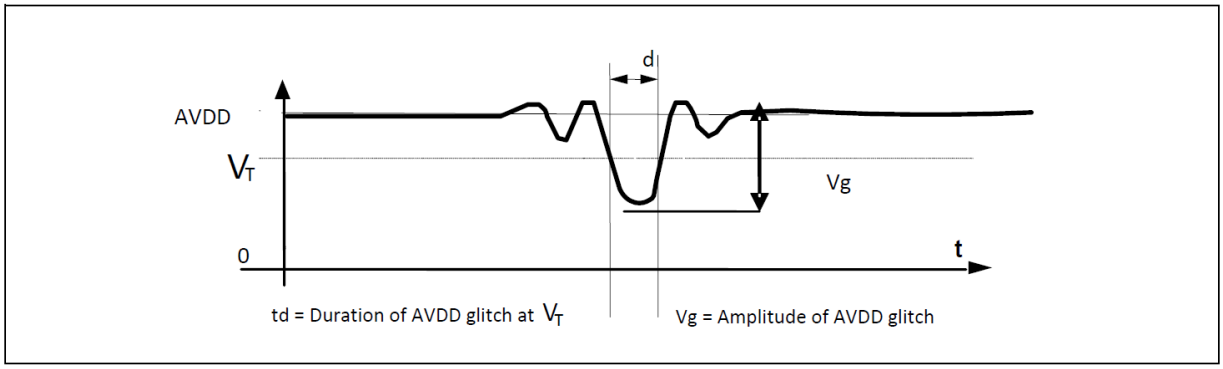


Table 3. Reset glitch specifications

Description	Symbol	Min	Typ	Max
RVDD_3V3 glitch duration	tg	150 ns		
RVDD_3V3 glitch amplitude	Vg	0.9 V		1.2 V

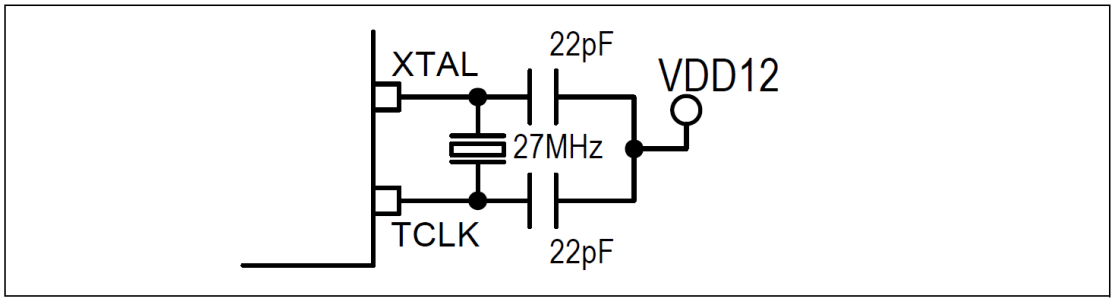
The RESETn pin requires a connection to ground with a 4.7 nF capacitor and a pull-up resistor of 1.2 K to RVDD_3V3 to avoid spurious reset conditions caused by board noise.

4.4 Clock generation

TCLK is the main timing clock for this device. All other internal clocks are generated from the TCLK. The TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator (27 MHz) or a crystal resonator (27 MHz) to generate a reference frequency source, as shown in the figure below.

The recommended operation uses an external crystal, which in turn, uses an internal oscillator circuit to generate the main chip clock. The internal oscillator provides a low jitter and low harmonic clock to the internal circuitry. The internal oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

Figure 7. Internal crystal oscillator operation

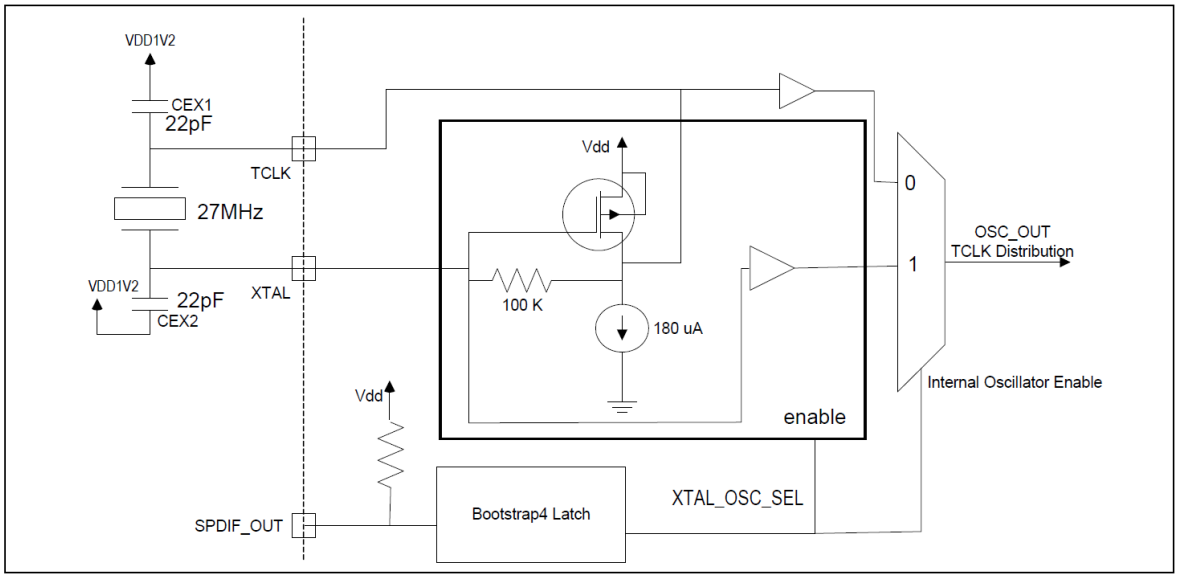


4.4.1 Internal crystal oscillator operation

A crystal resonator is connected between the XTAL pin and the TCLK pin with the appropriately sized loading capacitors CEX1 and CEX2. The logic level on the SPDIF pin is latched during the de-asserting edge of the RESETn signal and provides the XTAL_OSC_SEL bootstrap signal. A ‘1’ latched on this pin enables the crystal oscillator. The SPDIF pad has an internal pullup and should not be driven low during RESETn going high edge. Note that a ‘0’ latched turns off the oscillator and the availability of an external oscillator on the TCLK pin is assumed.

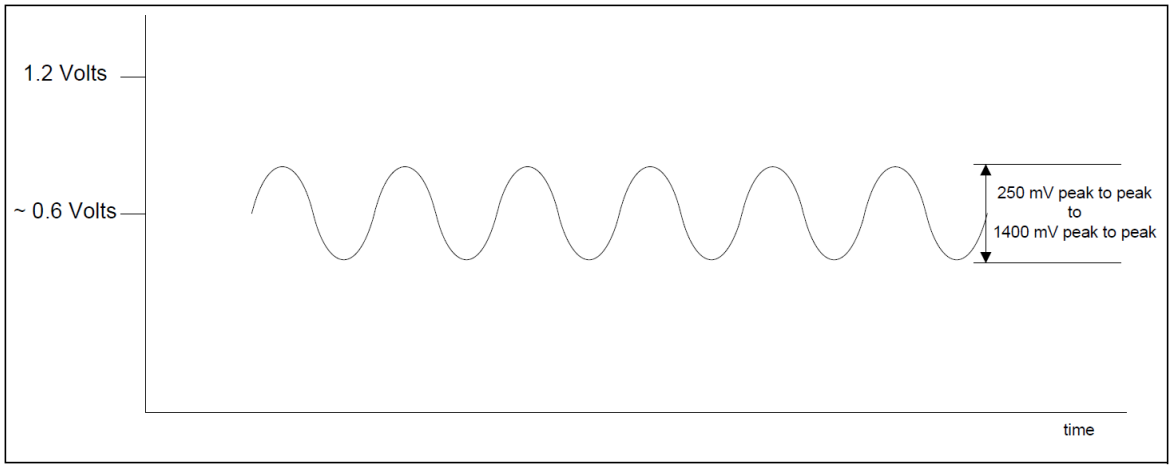
Note: *The size of CL1 and CL2 are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the device and the printed circuitboard traces. The loading capacitors are terminated to the RPLL_VDDA_1V2 power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.*

Figure 8. Internal crystal oscillator circuit with an external crystal



The internal oscillator circuit is a Pierce Oscillator circuit and a simplified schematic is shown in the figure above. The peak-to-peak voltage of the output can range from 250 mV to 1400 mV, depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator feeds to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50 mV peak-to-peak to function correctly. The buffered output signal of the comparator distributes to the rest of the STDP4320 circuits.

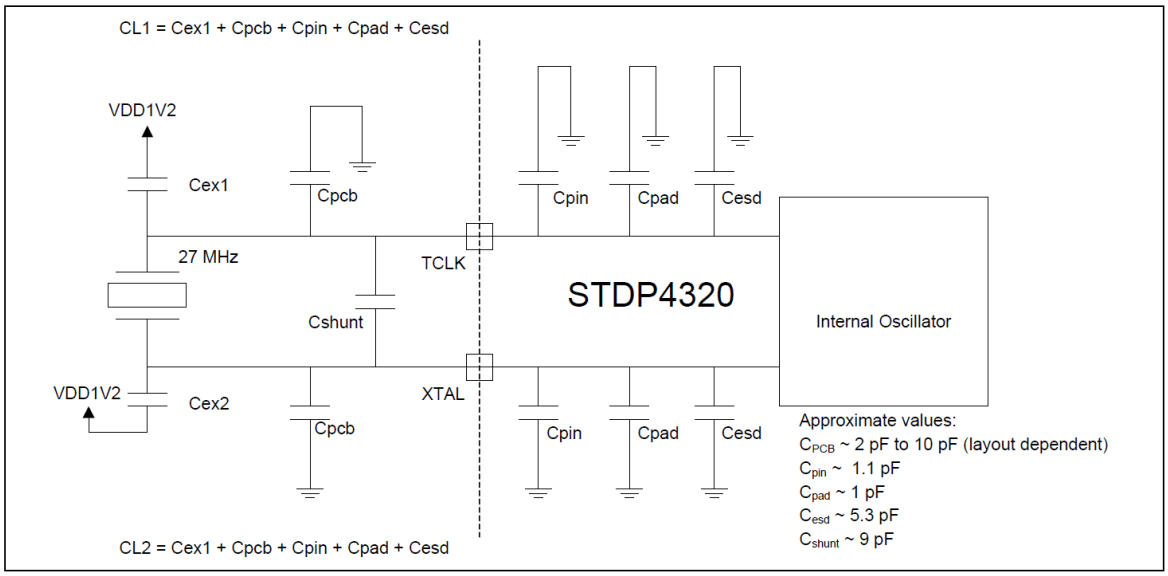
Figure 9. Internal oscillator output



One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal, as shown below. The loading capacitance (C_{load}) on the crystal is the combination of CL1 and CL2 and is calculated by C_{load} = ((CL1 * CL2)/(CL1 + CL2)) + C_{shunt}. The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For STDP4320, this is

approximately 9 pF. CL1 and CL2 are a parallel combination of the external loading capacitors (Cex), the PCB board capacitance (C_{pcb}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{esd}). The capacitances are symmetrical so that CL1 = CL2 = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}. The correct value of Cex must be calculated based on the values of the load capacitances.

Figure 10. Parasitic capacitance sources



Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of C_{load} that is specified by the manufacturer should not be exceeded to avoid potential start-up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less than 90 Ω.

It is recommended to utilize a minimum 50 ppm crystal oscillator for all applications. This will ensure optimum performance.

4.4.2 Recommendations for crystal specifications

While the selection of a crystal mainly depends on the specific PCB layout and the crystal manufacturer's specifications, the following are general recommendations.

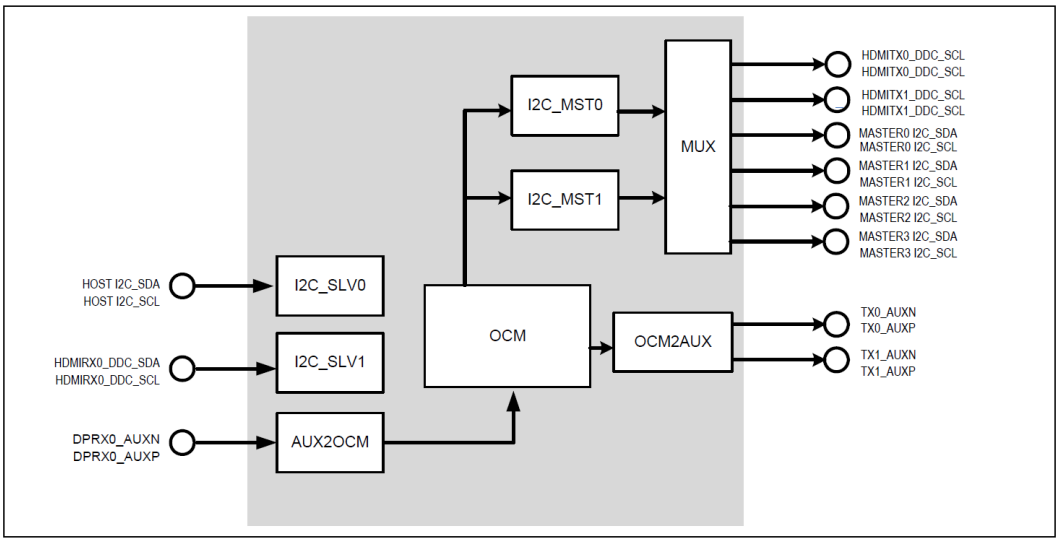
Table 4. Recommended crystal specifications

Parameters	Specifications
Frequency	27.000 MHz
Operation mode	Fundamental
Operating temperature	-10°C to +70°C
Frequency tolerance @25°C	+/- 50 ppm max
Frequency stability over temperature	+/- 100 ppm max
Load capacitance CL Shunt capacitance C0	8pF to 18pF 0.5pF to 7pF
Equivalent series resistance	< 80 ohms

4.5 I2C interface

The STDP4320 implements I2C master and slave ports for inter-device communication purposes. The I2C interface pins for host and slave device access are shown below.

Figure 11. I2C devices



There are two I2C Masters and two I2C Slaves inside STDP4320. The I2C Masters can communicate with an external slave device in the system through any of the six I2C master ports. The two I2C Slaves have dedicated port pins; one is used for host interface from an external system master in case STDP4320 is used as a slave device, and the second I2C Slave is used for HDMI RX DDC interface. In addition, the I2C over AUX communication from the upstream DP source can be sent out on any of the Master I2C ports or over the downstream AUX Channel. The following table provides a summary of all port pin pairs through which I2C Slaves, Masters, and AUX2OCM are accessible.

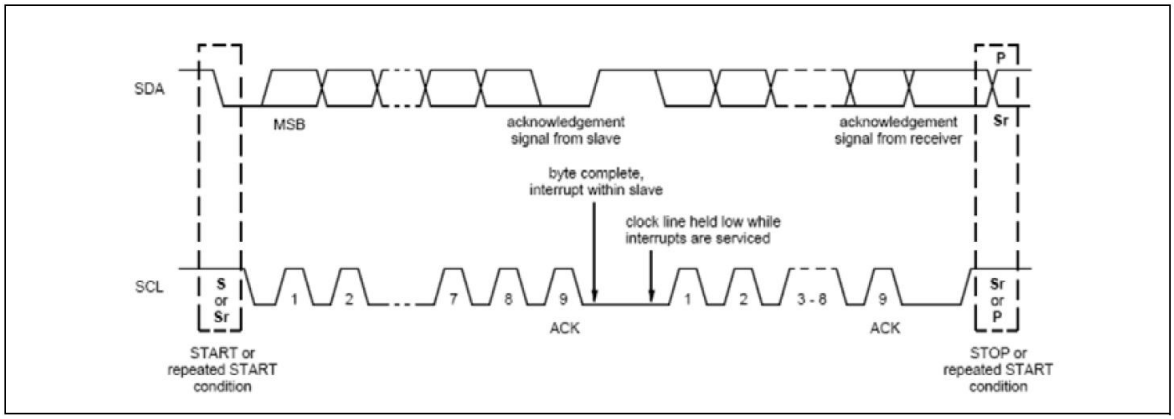
Table 5. I2C device-pin map

I2C Master0	I2C Master1	I2C over AUX	I2C Slave0	I2C Slave1	Port pins
From OCM to external slave device	From OCM to external slave device	From upstream DP source to external slave device	x	x	MASTER0 I2C_SDA MASTER0 I2C_SCL
From OCM to external slave device	From OCM to external slave device	From upstream DP source to external slave device	x	x	MASTER1 I2C_SDA MASTER1 I2C_SCL
From OCM to external slave device	From OCM to external slave device	From upstream DP source to external slave device	x	x	MASTER2 I2C_SDA MASTER2 I2C_SCL
From OCM to external slave device	From OCM to external slave device	From upstream DP source to external slave device	x	x	MASTER3 I2C_SDA MASTER3 I2C_SCL
From OCM to downstream HDMI sink	From OCM to downstream HDMI sink	From upstream DP source to downstream HDMI sink	x	x	HDMITX0_DDC_SDA HDMITX0_DDC_SCL
From OCM to downstream HDMI sink	From OCM to downstream HDMI sink	From upstream DP source to downstream HDMI sink	x	x	HDMITX1_DDC_SDA HDMITX1_DDC_SCL
x	x	From upstream DP source to downstream DP sink	x	x	TX0_AUX_P TX0_AUX_N
x	x	From upstream DP source to downstream DP sink	x	x	TX1_AUX_P TX1_AUX_N
x	x	x	Host interface	x	HOST I2C_SDA HOST I2C_SCL
x	x	x	x	To upstream HDMI source	HDMIRX0_DDC_SDA HDMIRX0_DDC_SCL

HDMI_DDC_SDA/HDMI_DDC_SCL signal pairs are also used for HDCP transactions between STDP4320 and connected HDMI source or sink.

Access communication protocol over all of the above I2C ports is identical. Every byte on the SDA line must be 8-bits long and the number of bytes in each transfer is unrestricted. Data transferred is with MSB first. If a slave cannot send or receive a complete transfer until it has performed some other function, such as servicing an internal interrupt, it can hold the clock line SCL Low to force the master into wait state. Data transfer can resume when the slave is ready for another byte of data after it releases the clock line SCL.

Figure 12. Data transfer in I2C bus



4.5.1 I2C slave interface

The I2C slave0 is intended for host communication purposes. In a typical application, the host controller (external I2C master) communicates with STDP4320 through this interface. STDP4320 contains a set of host interface registers that are directly read and written by the host controller. Whenever the host controller intends to configure or change the behavior of STDP4320, it writes into the corresponding host register. The STDP4320 responds to this instruction by executing the intended function and updating the status flag or result register. The host then reads the status or result registers. The host controller must provide the clocks on SCL for both read and write transactions. The port pins used for the host interface are HOST I2C_SDA and HOST I2C_SCL. When the chip power is turned off, these lines are tri-stated allowing other I2C devices to continue communication over common I2C bus. The host controller can access STDP4320 OCM registers with the device ID E0h/E2h/E4h/E6h and the core registers using configurable I2C device ID. The I2C device address selection is based on the settings of Bootstrap_6 and Bootstrap_7 as follows. Refer to *Section 6.2: Bootstrap configuration* for bootstrap pin descriptions.

Table 6. I2C device address selection

Bootstrap_7	Bootstrap_6	12C device address
Low	Low	E2h
Low	High	E0h
High	Low	E4h
High	High	E6h

4.5.2 HDMI Rx DDC interface

The HDMIRX DDC interface is a 3.3 V tolerant open-drain I2C slave interface. A 5 V to 3.3 V external level shifter is recommended for these signal pairs to connect with the HDMI source. This interface handles the EDID, MCCS, or HDCP protocols with the upstream source.

4.5.3 HDMI Tx DDC interface

The HDMITX DDC interface is a 3.3 V tolerant open-drain I2C master interface. A 3.3 V to 5 V external level shifter is recommended for these signal pairs to connect with the HDMI sinks. This interface handles the EDID, MCCS, or HDCP protocols with the downstream sinks.

4.5.4 I2C over AUX interface

The I2C over AUX communication between STDP4320 and the upstream DisplayPort source is handled by the On-Chip Micro (OCM). The AUX2OCM block bridges between the upstream DP AUX channel and OCM for I2C message transaction. These I2C commands are further routed out either through one of the I2C masters or through the OCM2AUX Bridge for the downstream DP sinks. The selection of the output port pins are software configurable depending on the application. For ex: If the downstream sinks are HDMI, the I2C commands are sent out on HDMI DDC port pins. Similarly, if the downstream is DP sinks, the I2C commands are sent out on the downstream AUX channel. The EDID access and MCCS command exchange between DisplayPort source and the downstream sinks take place through this interface.

Note: The base firmware handles all AUX transactions through the AUX2OCM and OCM2AUX interface.

4.5.5 I2C transactions

The basic I2C transactions are shown below. Commands in parenthesis are sent by I2C master.

Read sequence:

(SLAVE ADDRESS+R), ACK, DATA, (ACK), DATA, (ACK), DATA,…… (NACK), (Stop)

Write sequence:

(SLAVE ADDRESS+#W), ACK, (DATA), ACK,….. (DATA), ACK (Stop)

Device addressing

S	DevID with R/W	Address

Word write

The slave sends an ACK after every byte. S is *start* condition. P is *stop* condition.

S	DevID with R/W = 0	Address	Data (L)	Data (H)	P

Page write

The slave sends an ACK after every byte. The address is auto-incremented for every word received.

S	DevID with R/W = 0	Address	Data0 (L)	Data0 (H)	Data1 (L)	Data1 (H)	…	DataN-1 (L)	DataN-1 (H)	P

Word read

The master writes the register address. The slave sends an ACK after every byte received.

S	DevID with R/W = 0	Address	P

The data is sent out in the second transaction. The master provides the clocks and sends an ACK after every byte, except the last one. The stop condition marks the end of the transaction.

S	DevID with R/W = 1	Data (L)	Data (H)	P

Sequential read

The master writes the address of the first register to be read. The slave sends an ACK after every byte received.

S	DevID with R/W = 0	Address	P

The data is sent out in the second transaction. The master provides the clock and sends an ACK after every byte, except the last one. The address is auto-incremented after every word sent out on the bus. The stop condition marks the end of the transaction.

S	DevID with R/W = 1	Data0 (L)	Data0 (H)	Data1 (L)	Data1 (H)	…	DataN-1 (L)	DataN-1 (H)	P

Short read

This is similar to the sequential read, except the first write transaction with the address is omitted. The data is read from the current address in the address register. The master provides the clock and sends an ACK after every byte, except the last one. The address is auto-incremented after every word sent out on the bus. The stop condition marks the end of the transaction.

S	DevID with R/W = 1	Data0 (L)	Data0 (H)	Data1 (L)	Data1 (H)	…	DataN-1 (L)	DataN-1 (H)	P

4.6 DP, HDMI dual mode receiver

The STDP4320 has a high speed dual mode digital receiver that can be configured for DisplayPort, HDMI, or DVI operation. This receiver features four high speed differential input channels with a maximum link speed of 5.4 Gbps and a differential AUX Channel with a data rate of 1Mbps. The FastAUX feature is not supported. The Phy is configurable for DisplayPort mode or for HDMI/ DVI mode. The receiver has an internal differential termination of 100 ohms (50 ohms on each line to AVDD33). This can be either calibrated to 1/5th the external resistor value or manually programmable using register bits.

Inputs are AC-coupled in DisplayPort mode and DC-Coupled in HDMI / DVI modes. The dual mode receiver characteristics meet HBR2 operation in accordance with DisplayPort-1.2a specification. The Phy is also configurable for HDMI-1.4 operations up to 3.2 Gbps. The lane ordering of the receiver is programmable to optimize the board layout for each of the interface standards.

Note: The HDMI1.4 LAN and the audio back channel features are not supported.

In case of DisplayPort input, the data first goes through de-serialization and clock recovery, followed by 10b-8b conversion, symbol recovery, lane-de-skew, and HDCP decryption. The receiver back-end block receives the input packets and converts into video raster and audio samples. The video de-packetizer generates a raster video stream of up to 16 bits/color at up to 300 MHz video clock rate from 1, 2, or 4 lanes of DisplayPort traffic. The data may be in RGB 444 or 422 formats. 422 is only supported for YUV. 3D-formatted packets and VSC packets conveying in-band 3D signals can also be received. The secondary packets received may be CEA861E info frames or audio stream packets, recovered into buffers or audio-FIFOs.

The received audio packet may be a 2-channel layout or an 8-channel layout. Coding types can be either IEC61937 or IEC60958 style encoded data for 1 to 8 channels of LPCM, AC3, and DTS audio streams. Other formats including HBR audio (based on audio InfoFrame support definition of the sink device DDC) are also supported. Audio copy management is supported.

The DisplayPort Aux channel is a bidirectional, AC-coupled, doubly terminated differential signal pair. It is capable of transmitting and receiving data at 1 Mbps. The Aux channel is for link management and device control purposes. The Aux channel in the STDP4320 handles the following functions:

- Link training/Link management
- Native AUX and I2C-over-AUX communication

The HPD output signal serves as a cable-plug event indicator, as well as an interrupt request to the source device. The HPD output signal is in low state as long as the receiver is inactive. Once the sink device is ready to receive data, it sets the HPD signal to an active high state. This indicates to the source device that the sink is ready to receive data over the DisplayPort interface. When the receiver needs to interrupt the source, it shortly brings the HPD signal to low state. Refer to HPD-IRQ event described in the DisplayPort 1.2a specification.

In the case of HDMI mode, the receiver supports a max link rate of 3.2Gbps of operation with all possible video timing up to 4K2K 30Hz and color depths up to 48 bpp depending on available bandwidth. All 3D TV formats and color formats are supported including RGB/YUV444/YUV422 and xvYCC. The receiver supports automatic video and audio mute based on link conditions.The data island packet processor handles GCP packets, ACR packets, and AVI info packets. The HDMI receiver supports an HPD out signal. HEAC is not supported.

The received signal first goes through de-serialization and clock recovery. The receiver block then recovers sync presence, monitors and measures link clock, and detects symbol boundaries, lane alignment, and detects HDMI/DVI protocol and decodes the signal into video and data island streams. The video format is also detected. The signals then go through HDCP decryption. Video and audio streams are recovered from HDMI decoding.

4.7 HDMI formatter and controller

This block formats and encodes the video (TMDS), audio (TERC4), and auxiliary information as per the HDMI 1.4 specifications, including the BCH error encoding. The input video data to the formatter can be up to 16-bits/color and is to be accompanied by EIA/CEA 861 standard Hsync/Vsync and video clock up to 300 MHz. Input data can be either 444 RGB or YCbCr or 422 YCbCr. Pixel repeat of 1 to 4 is supported. Various 3D video formats can be transmitted. The 3D video format is indicated in the VIC Code in the AVI InfoFrame in conjunction with the 3D_Structure values defined in Table H-2 of the HDMI
1.4 spec in the HDMI Vendor Specific InfoFrame. In addition, STDP4320 contains logic to map DisplayPort 3D structures to HDMI 3D structure.

The HDMI formatter also takes in 8-channel, IEC60958, and IEC61937 formatted audio data up to 192 kHz. This includes two-channel or multi-channel PCM, LBR compressed, and HBR audio. The HDMI does not compress or decompress audio, but simply inserts the received audio into appropriate fields of the selected audio packets type in the HDMI frame. The HDMI frame formatter interfaces to the transmitter serializer on three 10-bit parallel buses, which are synchronous with the TMDS clock.

The encoded 30-bit stream can be sent to DisplayPort++ compliant transmitter for serialization and transmission.

4.8 DisplayPort formatter and controller

The DisplayPort formatter encodes 24-bit audio and 48-bit video signals into 1/2/4 lanes of DisplayPort single-stream packets. The encoded data is sent to the DisplayPort++ transmitter for serialization and transmission. All link rates from 1.62 Gbps (RBR), 2.7 Gbps (HBR), and 5.4 Gbps (HBR2) are supported.

The video formatter inputs a raster video stream of up to 16 bits per color at up to 300 MHz video clock rate. The data is converted to primary stream packets and can be mapped in 1, 2, or 4 lane formats as defined by DP 1.2a specifications. Input data may be in RGB or YUV 444 or 422 formats. Transfer units are formed with appropriate symbol stuffing as defined in the DisplayPort 1.2a specifications. MSA for all DP 1.2a color encoding formats up to 16-bits per color are supported. VSC packets can be used to send 3D in-band signals.

Secondary packets may be CEA861E Info Frames or audio stream packets. These are inserted into the main stream along with bit stuffing and MSA data stuffing. Inter-lane skewing is performed as defined by DP 1.2a specifications.

Audio stream data is formatted into secondary packets. The packet may be a 2-channel layout or an 8-channel layout. Coding types can be either IEC61937 or IEC60958 style encoded data for 1 to 8 channels of LPCM, AC2, and DTS audio streams. Other formats (based on audio InfoFrame support definition of the sink device DDC) and also audio copy management are supported.

The DPTX front-end block then performs data scrambling, 8b-10 encoding and DisplayPort specific formatting of the input data and generates one to four 20-bit parallel streams for each DP++ transmitter to serialize and output. An Aux channel controller handles link initiation, HDCP authentication communications, and DPCD messaging with the sink device. Side-band messages as defined in the DP 1.2a specification are also supported.

The AUX channel is used for link management and device control and handles the following functions:

- Link training
- Exchanging DPCD AUX and I2C communication

The HPD line is used to detect the presence of the sink device and to receive the interrupt requests from a DisplayPort sink device. The transmitter monitors the activity on the HPD line and responds to the receiver’s interrupt request by initiating the Aux channel transaction. The HPD line remains low when the sink device is not present and high when the sink device is ready to receive DisplayPort signals. An active low short pulse on the HPD line indicates an interrupt request from the sink device for an AUX transaction.

4.9 3D formats

The DisplayPort receiver and DisplayPort ++ transmitter supports all compatible 3D formats defined the DP1.2a and HDMI1.4 specifications. Following table lists the mapping of various 3D formats when converting DisplayPort input to HDMI output:

Table 7. 3D format mapping from DP 1.2a to HDMI 1.4

From DP 1.2a format	To HDMI 1.4b format
Frame/field sequential (VSC=0x01, 0x11, 0x21)	Frame packing (0x00)
Stacked frame (VSC=0x02)	Frame packing (0x00)
Frame/Field Sequential (VSC=0x01, 0x11, 0x21)	Frame Packing (0x00)
Stacked Frame (VSC=0x02)	Frame Packing (0x00)
Pixel Interleaved Right on Even Line (VSC=0x03)	Line Alternative(0x02)
Pixel Interleaved Right on Odd Line (VSC=0x013)	Line Alternative(0x02)
Pixel Interleaved Checker Board (VSC=0x23)	-
Pixel Interleaved Left First Vertical Line (VSC=0x33)	-
Pixel Interleaved Right First Vertical Line (VSC=0x43)	-
Side-by-Side Left View on Left Side (VSC=0x04)	Side-by-Side (Full, 0x03)
Side-by-Side Left View on Left Side (VSC=0x14)	Side-by-Side (Full, 0x03)

4.10 DisplayPort++ transmitter

The DisplayPort++ transmitter can receive lane signals from either the HDMI formatter or the DisplayPort formatter blocks. The main lanes are unidirectional, AC-coupled, doubly terminated differential pairs, to transport the audio-video streams. The serializer and PLL can operate in HDMI or DisplayPort modes. In HDMI mode, an external level translator is needed to make the output levels HDMI compliant. In DP++ modes, the AUX+/- can be shorted with HDMI_DDC_SDA/SCL. Configuration pins on the TX connector can be used to identify the presence of a passive dongle so the transmitters can be reconfigured as appropriate.

The transmitter supports all bit rates, 5.4 Gbps per lane (HBR2), 2.7 Gbps (HBR), and 1.62 Gbps (RBR). The transmitter locks to one of the bit rates after negotiating with the receiver (sink device). The transmitter supports down-spreading of link frequency.

The DisplayPort Aux channel is a half-duplex bidirectional, AC-coupled, doubly terminated differential pair. It is capable of transmitting and receiving bits at 1 Mbps.

4.11 HDCP

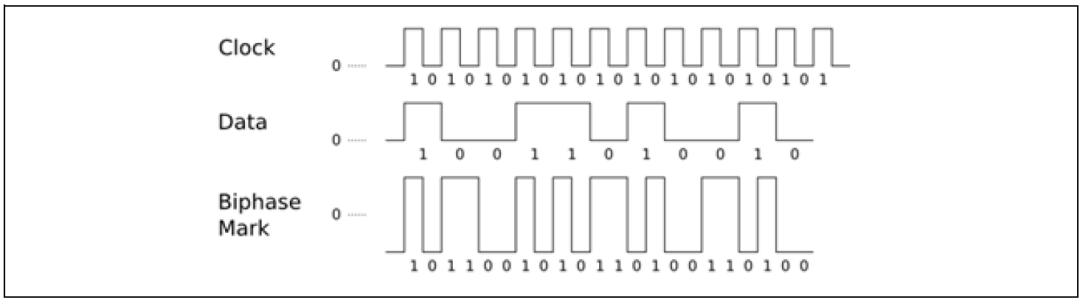
The HDCP block in STDP4320 establishes a secure channel for the transmission of high-definition multimedia data from an upstream source device to downstream receiving device(s). The HDCP cipher is used to provide key and messaging information to authenticate the transmission. Signals from the input video source device instruct the HDCP engine when to generate encryption keys, which are used by the transmitter to encrypt outgoing video data. An encrypted input stream from the DisplayPort or HDMI receiver will be re-transmitted as an encrypted stream with an HDCP repeater implementation. A driver controls HDCP authentication and synchronization of the HDCP receiver to allow encrypted data and identification of the receiver capabilities via AUX Channel or DDC. STDP4320 stores two separate sets of HDCP transmitter keys and one set of receiver keys within the OTP memory space.

4.12 SPDIF audio transmitter

STDP4320 includes two IEC60958 compliant SPDIF transmitters. Audio signals received over the DisplayPort or HDMI input can be transmitted on the SPDIF output port pins to either drive external audio DAC/amplifiers or an external audio processor. The SPDIF audio output is available as optional, besides the audio being transmitted over the DP or HDMI output. The feature is available in DP SST and/or HDMI output use cases. It is not available in DP MST output use cases. Audio outputs from DP or HDMI transmitter and SPDIF transmitter can be enabled simultaneously. Any two channels from an 8-channel DP or HDMI LPCM audio stream can be transmitted on the SPDIF output. The channel selection is through register configuration. The SPDIF transmitter also supports multi-channel compressed audio formats such as AC3 and DTS. There is no internal processing done on the audio stream. The output signal however, can be auto-muted based on receiver line conditions to avoid output of transient audio glitches during signal transition conditions.

The coding format used is BiPhase Mark Code (BMC) shown below.

Figure 13. SPDIF format



For each sample, two 32 bit words are sent out resulting in the following bit rates. The sample size can be 16, 20, or 24 bits. The data may be PCM or Compressed Audio.

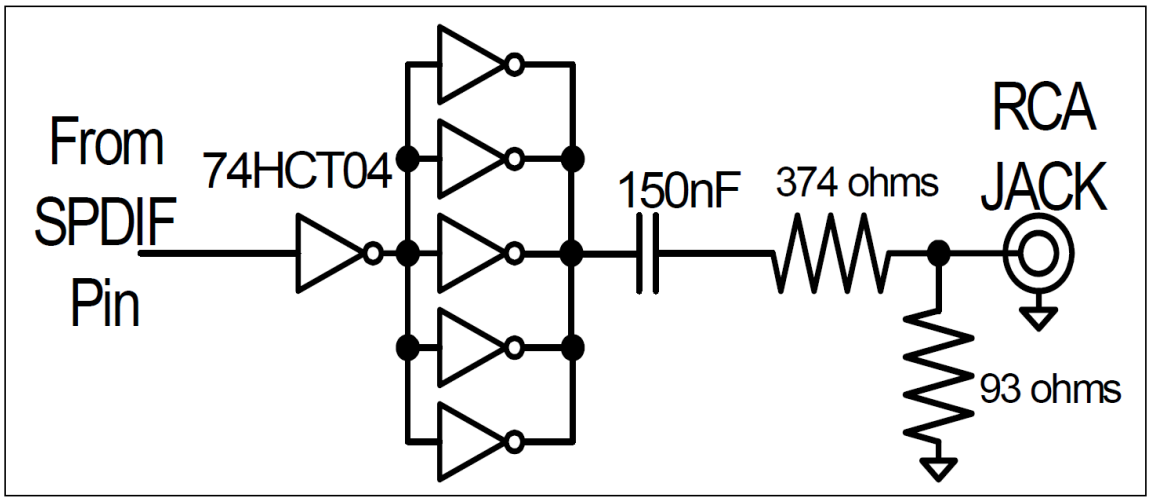
Table 8. SPDIF sample rates and line bit rates

	Sample rate	Bit rate
1	44.1 kHz	2.822 Mbps
2	48.0 kHz	3.072 Mbps
3	88.2 kHz	5.645 Mbps
4	96.0 kHz	6.144 Mbps
5	192.0 kHz	12.288 Mbps

4.12.1 SPDIF audio output signal conditioning

SPDIF output needs to have a circuit to make the voltage-down shift of the LVTTL signal to specific SPDIF signal. An example of such a conversion circuit is shown below.

Figure 14. SPDIF output circuit



4.13 Input-output maximum video timing support matrix

Maximum input-to-output timings are provided in the tables below. Note that the data path has a limit of 300 MHz on the HDMI output, thus maximum video timing with HDMI input or output configuration is limited to 4k2k 30Hz. Higher video timings up to 4k2k 60Hz is supported with the DisplayPort input, output configuration.

4.13.1 HDMI output mode maximum video timing

Table 9. HDMI output mode maximum video timings

	Input video DP or HDMI mode	Video resolution	Color depth	Video clock	HDMI output video timing
1	1L 5.4 GHz Or 2L 2.7 GHz	1920 x 1080p 60 Hz, reduced blanking	10 bits	148.5 MHz	1920 x 1080p 60 Hz, 10 bit, 185.6 MHz
2	2L 5.4 GHz Or 4L 2.7 GHz	1920 x 1080p 60 Hz, standard blanking	16 bits	148.5 MHz	1920 x 1080p 60 Hz, 16 bit, 297.0 MHz
3	2L 5.4 GHz Or 4L 2.7 GHz	2560 x 1440 60 Hz, reduced blanking	10 bits	241.5 MHz	2560 x 1440 60 Hz, 10 bit 301.88 MHz
4	2L 5.4 GHz Or 4L 2.7 GHz	2560 x 1600 60 Hz, reduced blanking	8 bits	268.50 MHz	2560 x 1600 60 Hz, 8 bit, 268.5 MHz
5	2L 5.4 GHz Or 4L 2.7 GHz	1920 x 1080p 120 Hz, standard blanking	8 bits	297.0 MHz	1920 x 1080p 120 Hz, 8 bit 297.0 MHz
6	2L 5.4 GHz Or 4L 2.7 GHz	4K x 2K, 24 Hz, reduced blanking	12 bits	211.5 MHz	4K x 2K 240 Hz, 12 bit, 317.0 MHz
7	2L 5.4 GHz Or 4L 2.7 GHz	4K x 2K, 30 Hz, reduced blanking	8 bits	265.0 MHz	4K x 2K 30 Hz, 8 bit, 265.0 MHz
8	HDMI1.4	4K x 2K, 24 Hz, standard blanking	12 bits	211.5 MHz	4K x 2K 30 Hz, 12 bit, 317.0 MHz
9	HDMI1.4	4K x 2K, 30 Hz, reduced blanking	8 bits	265.0 MHz	4K x 2K 30 Hz, 8 bit, 265.0 MHz

4.14 DisplayPort output maximum video timings

Table 10. DisplayPort output mode maximum video timings

	Input DP	Video resolution	Output color depth	Video clock	DisplayPort output video timing		
1	1L 5.4 GHz Or 2L 2.7 GHz	1920 x 1080p 60 Hz, reduced blanking	10 bits	148.5 MHz	2L 5.4 GHz	4L 2.7 GHz	4L 1.62 GHz
2	2L 5.4 GHz Or 4L 2.7 GHz	1920 x 1080p 60 Hz, 16b, standard blanking	16 bits	148.5 MHz	2L 5.4 GHz	4L 2.7 GHz	-
3	2L 5.4 GHz Or 4L 2.7 GHz	2560 x 1440 60 Hz, reduced blanking	10 bits	241.5 MHz	2L 5.4 GHz	4L 2.7 GHz	-
4	2L 5.4 GHz Or 4L 2.7 GHz	2560 x 1600 60 Hz, reduced blanking	8 bits	268.50 MHz	2L 5.4 GHz	4L 2.7 GHz	-
5	2L 5.4 GHz Or 4L 2.7 GHz	1920 x 1080p 120 Hz, standard blanking	8 bits	97.0 MHz	2L 5.4 GHz	4L 2.7 GHz	-
6	2L 5.4 GHz Or 4L 2.7 GHz	4K x 2K, 24 Hz, reduced blanking	12 bits	211.5 MHz	2L 5.4 GHz	4L 2.7 GHz	-
7	2L 5.4 GHz Or 4L 2.7 GHz	4K x 2K, 30 Hz, reduced blanking	8 bits	265.0 MHz	2L 5.4 GHz	4L 2.7 GHz	-
8	HDMI1.4	4K x 2K, 24 Hz, standard blanking	12 bits	211.5 MHz	2L 5.4 GHz	4L 2.7 GHz	-
9	HDMI1.4	4K x 2K, 30 Hz, reduced blanking	8 bits	265.0 MHz	2L 5.4 GHz	4L 2.7 GHz	-
	42L 5.4 GHz	4K x 2K, 60 Hz, reduced blanking	10 bits	538.5 MHz	4L 5.4 GHz	-	-

4.15 On-chip microcontroller (OCM)

The STDP4320 features a 16-bit on-chip microcontroller. On Power-on Reset, the OCM executes code from internal ROM. Following initial chip configuration, the execution can transfer to external Flash memory. The OCM is used to initialize various modules and provide firmware drivers for the receivers and transmitters, as well as execute customer-specific application code involved in the chip deployment. The OCM can execute at 150 MHz clock and can be tuned to optimize power consumption and processing requirements. Among the various peripheral controllers that are part of OCM are timers, interrupt controller, I2C master and slave controllers, UART, and general-purpose input-output pins. The GPIO pins are used to monitor and control external TTL outputs. Some of the monitoring functions include cable detection, host power detection etc. External power supply units can be controlled by programmable outputs to control the way the system is powered.

The chip supports a SPI interface to connect a commercial serial Flash ROM device. The chip supports

SPI Flash ROMs of sizes up to 4 MBits. Contact Kinetic for the list of SPI Flash devices supported in the ISP driver tool.

4.16 Serial peripheral interface for SPI Flash ROM

The SPI interface between STDP4320 and a serial Flash ROM is as follows:
SPI_CSn <-> CE# of SPI memory
SPI_CLK <-> SCK of SPI memory
SPI_DO <-> SI of SPI memory
SPI_DI <-> SO of SPI memory

As an option, the SPI Flash can be partitioned to hold two executable images; only one of them is valid for execution at a time. A Flash image can be updated through In-System Programming (ISP). Once the update is successful, the old image is invalidated. During the next boot-up, the new Flash image will be executed. It is possible to connect GPIO pins to control other pins the Flash memory might need to interface to. Pins of WP# and HOLD# of SPI memory are options for controlling the SPI device. WP#, if pulled low, disables writing to the memory. HOLD# is used when multiple devices are used in daisy-chain configuration. They can be pulled-high at all times to disable their functions or they can be controlled with GPIOs for more flexibility. The SPI pins must not be driven during RESETn low, as this can cause potential lock-ups due to boot-failure. The levels on these pins during reset are used for bootstrap configuration and this could change the way the chip boots.

4.17 Test, debug, and development

The following sections are useful for chip test, debug, and development purposes.

4.17.1 UART interface

The OCM has an integrated Universal Asynchronous Receiver and Transmitter (UART) port that can be used as a factory debug port. The UART interface is optional and described only to give information for developmental/debug purposes. In particular, the UART can be used to 1) read/write chip registers; 2) In-System-Programming of the SPI Flash. The UART_RX and UART_TX pins also share functionality with GPIO. When unused, these pins are available as GPIO pins. The UART baud rate is set to 115200 baud.

4.17.2 In-system-programming (ISP) of external Flash ROM

It is possible to program the serial ROM devices via the standard UART or I2C or through DisplayPort AUX channel or HDMI DDC interface. The embedded boot firmware performs the programming of external Flash ROM. However, ISP requires an external hardware and software tool (GProbe). Contact Kinetic for the ISP tool and procedure.

5. BGA footprint and pin lists

5.1 Ball grid array diagram

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

The STDP4320 is available in a 172-pin LFBGA package.

White = no ball at this location

n/c = no connect: ball present, but must not be connected

Figure 15. STDP4320 BGA diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	RX0_LN2_N			RX0_LN0_P	RX0_AUX_P	RX0_AUX_N	n/c	n/c	n/c			n/c	VSS	A
B	RX0_LN3_P	RX0_LN2_P			RX0_LN0_N	VSS	VSS	VSS	VSS	n/c			n/c	n/c	B
C	RX0_LN3_N	AVDD33_RX	RX0_LN1_N	RX0_LN1_P	AVDD12_RX	AVDD12_RX	AVDD33_RX	AVDD33_RX	AVDD12_RX	AVDD12_RX	n/c	n/c	AVDD33_RX	n/c	C
D	TX1_HPD	TEST	VSS	VSS	VSS	RX0_REXT	VSS	VSS	n/c	VSS	VSS	VSS	HDMI_TX0_DDC_SCL	HDMI_TX0_DDC_SDA	D
E	n/c	SPDIF_OUT0	HDMI_CEC	TX0_HPD	DVDD12					DVDD12	HDMI_TX1_DDC_SDA	GPIO8	GPIO6	HDMI_TX1_DDC_SCL	E
F	MASTER1_IRQ_IN	GPO	SPDIF_OUT1	RX0_HPD	DVDD12	VSS	VSS	VSS	VSS	DVDD12	GPIO9	GPIO10	GPIO11	GPIO7	F
G	MASTER2_IRQ_IN	MASTER3_IRQ_IN	GPIO13	MASTER0_IRQ_IN	DVDD12	VSS	VSS	VSS	VSS	DVDD12	MASTER2_I2C_SDA	MASTER2_I2C_SCL	MASTER0_I2C_SDA	MASTER0_I2C_SCL	G
H	GPIO12	HOST_IRQ_OUT	SPI_CLK	UART_TX	DVDD12	VSS	VSS	VSS	VSS	DVDD12	HDMI_RX0_DDC_SCL	RESET_N	MASTER1_I2C_SDA	MASTER1_I2C_SCL	H
J	SPI_DI	UART_RX	SPI_CSN	GPIO2	DVDD33	VSS	VSS	VSS	VSS	DVDD33	n/c	HOST_I2C_SCL	MASTER3_I2C_SCL	MASTER3_I2C_SDA	J
K	TCLK_3V3_OUT	SPI_DO	GPIO0	GPIO1	DVDD25_SM					GPIO5	n/c	HDMI_RX0_DDC_SDA	AVDD12_PLL	HOST_I2C_SDA	K
L	TCLK_1V2_OUT	TX0_REXT	VSS	VSS	GPIO3	VSS	VSS	VSS	VSS	GPIO4	VSS	VSS	AVDD12_OSC1	AVDD33_RCOSC	L
M	TX0_AUX_N	AVDD12_TX0	TX0_LN2_N	TX0_LN2_P	AVDD12_TX0	AVDD12_OSC0	VSS	VSS	TX1_REXT	AVDD12_TX1	TX1_LN2_N	TX1_LN2_P	AVDD33_TX1	TX1_LN0_P	M
N	TX0_AUX_P	TX0_LN3_P			TX0_LN1_N	AVDD33_TX0	TCLK	XTAL	AVDD12_TX1	TX1_LN3_P			TX1_LN1_N	TX1_LN0_N	N
P	VSS	TX0_LN3_N			TX0_LN1_P	TX0_LN0_N	TX0_LN0_P	TX1_AUX_N	TX1_AUX_P	TX1_LN3_N			TX1_LN1_P	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

5.2 Full pin list sorted by pin number

Table 11. Pin list

Pin number	Net name
A1	VSS
A2	RX0_LN2_N
A5	RX0_LN0_P
A6	RX0_AUX_P
A7	RX0_AUX_N
A8, A9, A10, A13	n/c
A14	VSS
B1	RX0_LN3_P
B2	RX0_LN2_P
B5	RX0_LN0_N
B6, B7, B8, B9	VSS
B10, B13, B14	n/c
C1	RX0_LN3_N
C2	AVDD33_RX
C3	RX0_LN1_N
C4	RX0_LN1_P
C5, C6	AVDD12_RX
C7, C8	AVDD33_RX
C9, C10	AVDD12_RX
C11, C12	n/c
C13	AVDD33_RX
C14	n/c
D1	TX1_HPD
D2	TEST
D3, D4, D5	VSS
D6	RX0_REXT
D7, D8	VSS
D9	n/c
D10, D11, D12	VSS
D13	HDMI_TX0_DDC_SCL
D14	HDMI_TX0_DDC_SDA
E1	n/c
E2	SPDIF_OUT0

Table 11. Pin list (continued)

Pin number	Net name
E3	HDMI_CEC
E4	TX0_HPD
E5	DVDD12
E10	DVDD12
E11	HDMI_TX1_DDC_SDA
E12	GPIO8
E13	GPIO6
E14	HDMI_TX1_DDC_SCL
F1	MASTER1_IRQ_IN
F2	GPO
F3	SPDIF_OUT1
F4	RX0_HPD
F5	DVDD12
F6, F7, F8, F9	VSS
F10	DVDD12
F11	GPIO9
F12	GPIO10
F13	GPIO11
F14	GPIO7
G1	MASTER2_IRQ_IN
G2	MASTER3_IRQ_IN
G3	GPIO13/TX1_CONFIG2
G4	MASTER0_IRQ_IN
G5	DVDD12
G6, G7, G8, G9	VSS
G10	DVDD12
G11	MASTER2_I2C_SDA
G12	MASTER2_I2C_SCL
G13	MASTER0_I2C_SDA
G14	MASTER0_I2C_SCL
H1	GPIO12/TX1_CONFIG1
H2	HOST_IRQ_OUT
H3	SPI_CLK
H4	UART_TX
H5	DVDD12

Table 11. Pin list (continued)

Pin number	Net name
H6, H7, H8, H9	VSS
H10	DVDD12
H11	HDMI_RX0_DDC_SCL
H12	RESETn
H13	MASTER1_I2C_SDA
H14	MASTER1_I2C_SCL
J1	SPI_DI
J2	UART_RX
J3	SPI_CSN
J4	GPIO2
J5	DVDD33
J6, J7, J8, J9	VSS
J10	DVDD33
J11	n/c
J12	HOST_I2C_SCL
J13	MASTER3_I2C_SCL
J14	MASTER3_I2C_SDA
K1	TCLK_3V3_OUT
K2	SPI_DO
K3	GPIO0/TX0_CONFIG1
K4	GPIO1/TX0_CONFIG2
K5	DVDD25_SM
K10	GPIO5
K11	n/c
K12	HDMI_RX0_DDC_SDA
K13	AVDD12_PLL
K14	HOST_I2C_SDA
L1	TCLK_1V2_OUT
L2	TX0_REXT
L3, L4	VSS
L5	GPIO3/RX0_CABLE_DET0
L6, L7, L8, L9	VSS
L10	GPIO4/RX0_CABLE_DET1
L11, L12	VSS
L13	AVDD12_OSC1

Table 11. Pin list (continued)

Pin number	Net name
L14	AVDD33_RCOSC
M1	TX0_AUX_N
M2	AVDD12_TX0
M3	TX0_LN2_N
M4	TX0_LN2_P
M5	AVDD12_TX0
M6	AVDD12_OSC0
M7, M8	VSS
M9	TX1_REXT
M10	AVDD12_TX1
M11	TX1_LN2_N
M12	TX1_LN2_P
M13	AVDD33_TX1
M14	TX1_LN0_P
N1	TX0_AUX_P
N2	TX0_LN3_P
N5	TX0_LN1_N
N6	AVDD33_TX0
N7	TCLK
N8	XTAL
N9	AVDD12_TX1
N10	TX1_LN3_P
N13	TX1_LN1_N
N14	TX1_LN0_N
P1	VSS
P2	TX0_LN3_N
P5	TX0_LN1_P
P6	TX0_LN0_N
P7	TX0_LN0_P
P8	TX1_AUX_N
P9	TX1_AUX_P
P10	TX1_LN3_N
P13	TX1_LN1_P
P14	VSS

6. Connections

6.1 Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground; IO = Bi-direction; AI = Analog input; AO = Analog output; AIO = Analog I/O; TRI = Tristate; TOL = Tolerance; PD = Internal 50K pulldown; PU = Internal 50K pull-up; OPENDR = Open drain output

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 12. DisplayPort receiver pins

Pin	Assignment	I/O	Description	Reset state
D6	RX0_REXT	AIO, 3V3 TOL	Connect to External 249 Ohm Resistor to VDD33	NA
A5	RX0_LN0_P	AIO, 3V3 TOL	DUAL MODE RX HDMI CLOCKP OR DP RX_LN0P.	TRISTATE
B5	RX0_LN0_N	AIO, 3V3 TOL	DUAL MODE RX HDMI CLOCKN OR DP RX_LN0N.	TRISTATE
C4	RX0_LN1_P	AIO, 3V3 TOL	DUAL MODE RX HDMI RX0P OR DP RX_LN1P.	TRISTATE
C3	RX0_LN1_N	AIO, 3V3 TOL	DUAL MODE RX HDMI RX0N OR DP RX_LN1N.	TRISTATE
B2	RX0_LN2_P	AIO, 3V3 TOL	DUAL MODE RX HDMI RX1P OR DP RX_LN2P.	TRISTATE
A2	RX0_LN2_N	AIO, 3V3 TOL	DUAL MODE RX HDMI RX1N OR DP RX_LN2N.	TRISTATE
B1	RX0_LN3_P	AIO, 3V3 TOL	DUAL MODE RX HDMI RX2P OR DP RX_LN3P.	TRISTATE
C1	RX0_LN3_N	AIO, 3V3 TOL	DUAL MODE RX HDMI RX2N OR DP RX_LN3N.	TRISTATE
A6	RX0_AUX_P	AIO, 1V2 TOL	DUAL MODE RX DP RX_AUXP. AC Couple 0.1uF. Use 20 Ohm damping resistor in series and 1M Ohm pull up to 3.3 V before cap.	TRISTATE
A7	RX0_AUX_N	AIO, 1V2 TOL	DUAL MODE RX DP RX_AUXN. AC Couple 0.1uF. Use 20 Ohm damping resistor in series and 1M Ohm pull down to GND before cap.	TRISTATE

Note: The default DP and HDMI input signals mapping match the standard DP and HDMI connector pin mapping. However, lane swapping and polarity swapping are possible through software configuration.

Table 13. System function pins

Pin	Assignment	I/O	Description	Reset state
D2	TEST	I, 3V3 TOL, INT PD	Connect to GND	INPUT, Internal PD
N7	TCLK	AIO, 1V2 TOL	Connect to 27 MHz crystal oscillator with 22 pF to 1.2 V.	NA
N8	XTAL			
K1	TCLK_3V3_OUT	IO, 3V3 TOL	TCLK output, Tristate 3.3 V pad	TRISTATE
L1	TCLK_1V2_OUT	IO, 1V2 TOL	TCLK output, Tristate 1.2 V pad	TRISTATE
H12	RESETn	AIO, 3V3 TOL	Use external 3K ohm resistor to 3.3 V	TRISTATE, INPUT
J3	SPI_CSN	IO, 3V3 TOL, TRI, INT PU	To SPI chip select. Also see *Table 18: Bootstrap configuration*.	TRISTATE, Internal PU
K2	SPI_DO	IO, 3V3 TOL, TRI, INT PD	To SPI data out. Also see *Table 18: Bootstrap configuration*.	TRISTATE, Internal PD
J1	SPI_DI	I, 3V3 TOL, INT PD	From SPI data in.	INPUT with Internal PD
H3	SPI_CLK	IO, 3V3 TOL, TRI, INT PD	To SPI clock. Also see *Table 18: Bootstrap configuration*.	TRISTATE, Internal PD

Table 14. Multi-function pins

Pin	Assignment	I/O	Description	Reset state
E3	HDMI_CEC	IO, 3.3 TOL, TRI	HDMI CEC not supported in the current silicon rev. Connect this pin to external pull-up DVDD3V3.	TRISTATE
F4	RX0_HPD		To the upstream HPD signal pin on the DP connector. 100K res to GND.	TRISTATE
L5	GPIO3/ RX0_CABLE_DET0		Cable detect1 for DisplayPort connector	TRISTATE
L10	GPIO4/ RX0_CABLE_DET1		Cable detect2 for DisplayPort connector	TRISTATE
K12	HDMI_RX0_DDC_SDA		DDC SDA for upstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
H11	HDMI_RX0_DDC_SCL		DDC SCL for upstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
E2	SPDIF_OUT0	IO, 3.3 TOL, TRI, INT PU	To external buffer for SPDIF output [Audio corresponding to video on Port0]	TRISTATE, Internal PU
F3	SPDIF_OUT1		To external buffer for SPDIF output [Audio corresponding to video on Port1]	TRISTATE, Internal PU

Table 14. Multi-function pins (continue)

Pin	Assignment	I/O	Description	Reset state
E4	TX0_HPD	IO, 3.3 TOL, TRI	HPD in for Downstream DP/HDMI port0	TRISTATE
J4	GPIO2		General Purpose input/output, Tristate 3.3 V pad	TRISTATE
D14	HDMI_TX0_DDC_SDA		DDC SDA for downstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
D13	HDMI_TX0_DDC_SCL		DDC SCL for downstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
K3	GPIO0/TX0_CONFIG1		Config1 input for Downstream DP port0 or GPIO	TRISTATE
K4	GPIO1/TX0_CONFIG2		Config2 input for Downstream DP port0 or GPIO	TRISTATE
D1	TX1_HPD		HPD in for Downstream DP/HDMI port1	TRISTATE
K10	GPIO5		General Purpose input/output, Tristate 3.3 V pad	TRISTATE
E11	HDMI_TX1_DDC_SDA	IO, 3.3 TOL, TRI	DDC SDA for downstream HDMI port1. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
E14	HDMI_TX1_DDC_SCL		DDC SCL for downstream HDMI port1 . Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
H1	GPIO12/ TX1_CONFIG1		Config1 input for Downstream DP port1 or GPIO	TRISTATE
G3	GPIO13/ TX1_CONFIG2		Config2 input for Downstream DP port1 or GPIO	TRISTATE
H4	UART_TX	IO, 3.3 TOL, TRI, INT PU	To debug port UART_TX. Also see *Table 18: Bootstrap configuration*.	TRI, Internal PU
J2	UART_RX	IO, 3.3 TOL, TRI	To debug port UART_RX	TRISTATE
G14	MASTER0_I2C_SCL		Master I2C SCL Port0. Connect to I2C Slave with external Pull Up	TRISTATE
G13	MASTER0_I2C_SDA		Master I2C SDA Port0. Connect to I2C Slave with external Pull Up	TRISTATE
G4	MASTER0_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port0 interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
H14	MASTER1_I2C_SCL	IO, 3.3 TOL, TRI	Master I2C SCL Port1. Connect to I2C Slave with external Pull Up	TRISTATE
H13	MASTER1_I2C_SDA		Master I2C SDA Port1. Connect to I2C Slave with external Pull Up	TRISTATE
F1	MASTER1_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port01interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
G12	MASTER2_I2C_SCL	IO, 3.3 TOL, TRI	Master I2C SCL Port2. Connect to I2C Slave with external Pull Up	TRISTATE
G11	MASTER2_I2C_SDA		Master I2C SDA Port2. Connect to I2C Slave with external Pull Up	TRISTATE

Table 14. Multi-function pins (continue)

Pin	Assignment	I/O	Description	Reset state
G1	MASTER2_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port2 interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
J13	MASTER3_I2C_SCL	IO, 3.3 TOL, TRI	Master I2C SCL Port3. Connect to I2C Slave with external Pull Up	TRISTATE,
J14	MASTER3_I2C_SDA		Master I2C SDA Port3. Connect to I2C Slave with external Pull Up	TRISTATE,
G2	MASTER3_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port3 interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
J12	HOST_I2C_SCL	IO, 3.3 TOL, TRI	Slave I2C SCL. Connect to I2C Master with external Pull Up	TRISTATE
K14	HOST_I2C_SDA		Slave I2C SDA. Connect to I2C Master with external Pull Up	TRISTATE
H2	HOST_IRQ_OUT	IO, 3.3 TOL, TRI, INT PD	Interrupt out. Connect to interrupt in of Master	TRISTATE, Internal PD
E13	GPIO6	IO, 3.3 TOL, TRI	General purpose input/output	TRISTATE
F14	GPIO7	IO, 3.3 TOL, TRI		
E12	GPIO8	IO, 3.3 TOL, TRI		
F11	GPIO9	IO, 3.3 TOL, TRI		
F12	GPIO10	IO, 3.3 TOL, TRI		
F13	GPIO11	IO, 3.3 TOL, TRI		
F2	GPO	IO, 3.3 TOL, TRI, INT PD	General purpose input/output. See *Table 18: Bootstrap configuration*.	TRISTATE, Internal PD

Table 15. Transmitter pins

Pin	Assignment	I/O	Description	Reset state
L2	TX0_REXT	AI, 1V2 TOL	TX, EXTERNAL 249 Ohm RESISTOR TO VDD12	NA
N1	TX0_AUX_P	AIO, 1V2 TOL	DUAL MODE TX Port0 DP TX_AUXP. AC Couple to TX Connector. External 100K Resistor to GND.	TRISTATE
M1	TX0_AUX_N	AIO, 1V2 TOL	DUAL MODE TX Port0 DP TX_AUXN. AC Couple to TX Connector. External 100K Resistor to VDD33.	TRISTATE
N2	TX0_LN3_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TXCKP OR DP TX_LN3P. AC Couple to TX Connector.	TRISTATE
P2	TX0_LN3_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TXCKN OR DP TX_LN3N. AC Couple to TX Connector	TRISTATE
M4	TX0_LN2_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX2P OR DP TX_LN2P. AC Couple to TX Connector	TRISTATE
M3	TX0_LN2_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX2N OR DP TX_LN2N. AC Couple to TX Connector	TRISTATE
P5	TX0_LN1_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX1P OR DP TX_LN1P. AC Couple to TX Connector	TRISTATE
N5	TX0_LN1_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX1N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
P7	TX0_LN0_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX0P OR DP TX_LN1P. AC Couple to TX Connector	TRISTATE
P6	TX0_LN0_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX0N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
M9	TX1_REXT	AI, 1V2 TOL	TX, EXTERNAL 249 Ohm RESISTOR TO VDD12	NA
P9	TX1_AUX_P	AO, 1V2 TOL	DUAL MODE TX Port1 DP TX_AUXP. AC Couple to TX Connector. External 100K Resistor to GND.	TRISTATE
P8	TX1_AUX_N	AO, 1V2 TOL	DUAL MODE TX Port1 DP TX_AUXN. AC Couple to TX Connector. External 100K Resistor to VDD33.	TRISTATE
N10	TX1_LN3_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TXCKP OR DP TX_LN3P. AC Couple to TX Connector.	TRISTATE
P10	TX1_LN3_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TXCKN OR DP TX_LN3N. AC Couple to TX Connector	TRISTATE
M12	TX1_LN2_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX2P OR DP TX_LN2P. AC Couple to TX Connector	TRISTATE
M11	TX1_LN2_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX2N OR DP TX_LN2N. AC Couple to TX Connector	TRISTATE
P13	TX1_LN1_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX1P OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
N13	TX1_LN1_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX1N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
M14	TX1_LN0_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX0P OR DP TX_LN1P. AC Couple to TX Connector	TRISTATE
N14	TX1_LN0_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX0N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE

Table 16. System power and ground

Pin	Assignment	Description
J5, J10	DVDD33	I/O VDD, 3.3V digital supply. De-couple using 100 nF.
E5, E10, F5, F10, G5, G10, H5, H10	DVDD12	Core VDD, 1.2V digital supply. De-couple using 100 nF.
L14	AVDD33_RCOSC	3.3V RC-oscillator analog supply. De-couple using 100 nF.
K13	AVDD12_PLL	1.2V analog PLL supply. De-couple using 10 uF and 100 nF.
C5, C6, C9, C10	AVDD12_RX	1.2V analog receiver supply. EMI filter rail and de-couple using 10 uF and 100 nF.
C2, C7, C8, C13	AVDD33_RX	3.3V analog receiver supply. EMI filter rail and de-couple using 10 uF and 100 nF.
N6	AVDD33_TX0	3.3V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M13	AVDD33_TX1	3.3V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M2, M5	AVDD12_TX0	1.2V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M10, N9	AVDD12_TX1	1.2V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M6	AVDD12_OSC0	1.2V analog crystal oscillator supply. De-couple using 100 nF.
L13	AVDD12_OSC1	1.2V analog crystal oscillator supply. De-couple using 100 nF.
K5	DVDD25_SM	2.5V LDO supply. De-couple using 10 uF and 100 nF.
A1, A14, B6, B7, B8, B9, D3, D4, D5, D7, D8, D10, D11, D12, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, L3, L4, L6, L7, L8, L9, L11, L12, M7, M8, P1, P14	VSS	Common GND. Connect to GND plane

Table 17. Reserved pins

Pin	Assignment	Description
A8, A9, A10, A13, B10, B13, B14, C11, C12, C14, D9, E1, J11, K11	n/c	Reserved. Do not connect

6.2 Bootstrap configuration

DC levels on some of the pins are specified during de-asserting edge of power-on reset (RESETn goes high). The levels specified below must be adhered for normal function of the device.

Table 18. Bootstrap configuration

Bootstrap signal name	Internal PU/PD	Pin assignment	Function
Bootstrap_0	PULLUP	UART_TX (H4)	0: Reserved for ATE Test
			1: Normal Operation (Recommended)
Bootstrap_1	PULLDN	GPO (F2)	0: Crystal_OSC is enabled (Recommended)
			1: RC_OSC is enabled,
Bootstrap_2	PULLDN	SPI_CLK (H3)	0: OCM boot up from internal ROM (Recommended)
			1: OCM boot up from external ROM
Bootstrap_3	PULLDN	SPI_DO (K2)	0: Reserved for Testing (Recommended)
			1: Reserved for Testing
Bootstrap_4	PULLUP	SPDIF_OUT0 (E2)	0: Select External OSC Operation
			1: Select Internal OSC Operation (Recommended)
Bootstrap_5	PULLUP	SPI_CSN (J3)	0: Debug Mode
			1: Normal Operation (Recommended)
Bootstrap_6	PULLUP	SPDIF_OUT1 (F3)	0: Software Bootstrap for I2C address selection
			1: Software Bootstrap for I2C address selection
Bootstrap_7	PULLDN	HOST_IRQ_OUT (H2)	0: Software Bootstrap for I2C address selection
			1: Software Bootstrap for I2C address selection

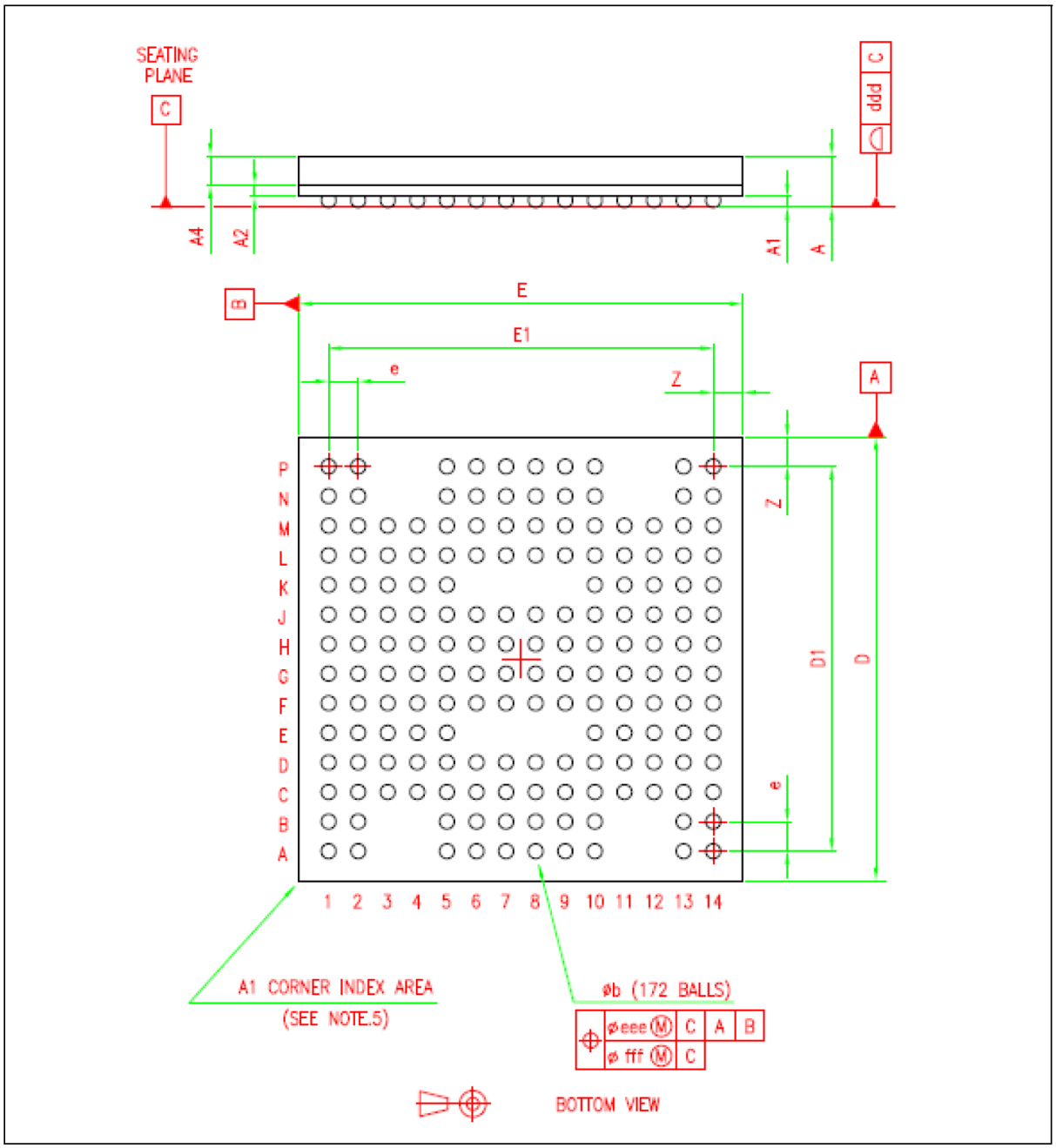
Note: When the pin corresponding to a specific bootstrap is left NC, it takes the value of the assigned by the internal PULLUP (Level 1) or PULLDN (Level0). The internal resistor used is around 50 k ohm. To select a non-default value on a bootstrap, an external PULLUP or PULLDN resistor is tied to the opposite direction that overcomes the internal PULLUP or PULLDN needs to be used.

7. Package specifications

Package type: 172 LFBGA (12 x 12 mm / ball pitch 0.8 mm)

7.1 Package drawing

Figure 16. Package drawing



7.2 Package dimensions

Figure 17. Package dimensions

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.70			1.43	(1)
A1	0.21			0.25	0.30	0.35	
A2		0.28		0.26	0.28	0.32	
A4			0.80	0.77	0.785	0.80	
b	0.35	0.40	0.45	0.35	0.40	0.45	(2)
D	11.85	12.00	12.15	11.90	12.00	12.10	
D1		10.40			10.40		
E	11.85	12.00	12.15	11.90	12.00	12.10	
E1		10.40			10.40		
e		0.80			0.80		
Z		0.80			0.80		
ddd			0.10			0.10	
eee			0.15			0.15	(3)
fff			0.08			0.08	(4)

NOTES:

(1) – LFBGA stands for Low profile Fine Pitch Ball Grid Array.
– Low Profile: 1.20mm < A ≤ 1.70mm / Fine pitch: e < 1.00mm.
– The total profile height (Dim A) is measured from the seating plane "C" to the top of the component.
– The maximum total package height is calculated by the RSS method (Root Sum Square):
A Max = A1 Typ + A2 Typ + A4 Typ +√ ($A1^2 + A2^2 + A4^2$ tolerance values).

(2) – The typical ball diameter before mounting is 0.40mm.

(3) – The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

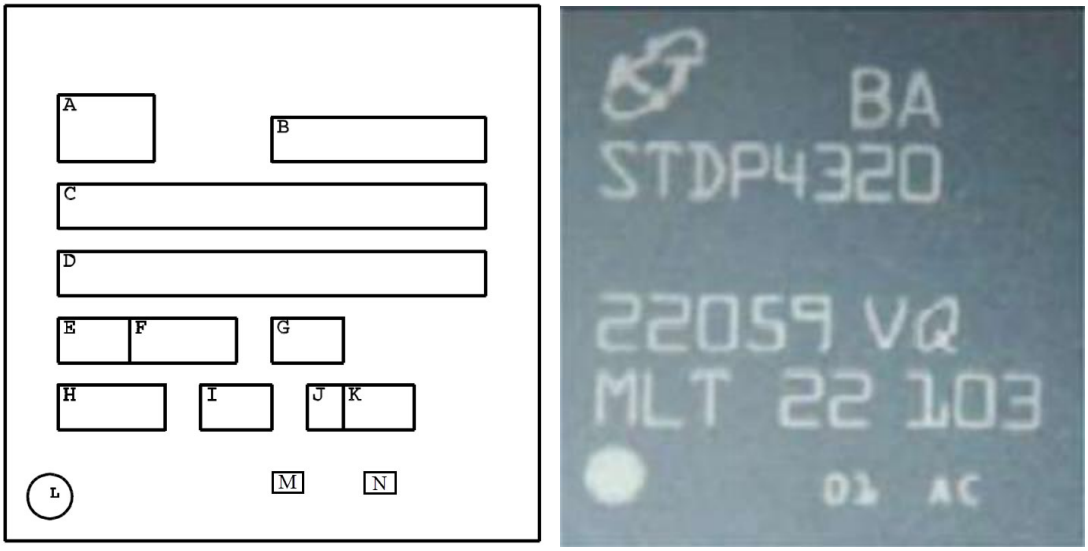
(4) – The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

(5) – The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
– A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

7.3 Marking field template and descriptors

The STDP4320 marking template is shown below.

Figure 18. Marking template



Field descriptors are shown below.

Table 19. Field descriptors

Field	Description	Marking
A	Company logo	
B	2-character version code	BA
C	Product code	STDP4320
D	Optional marking	<blank>
E	2-character assembly plant code	22
F	3-character BE sequence code	“XYZ”
G	2-character diffusion plant code	VQ
H	3-character country of origin code	MLT
I	2-character test plant code	22
J	1-digit assembly year	“Y”
K	2-digit assembly week	“WW”
L	Ball A1 identifier	a DOT
M	SS SUBLOT ASSY	01
N	ADDITIONAL INFORMATION	AC

7.4 Classification reflow profile

Please refer to the DisplayPort Application Note: Classification reflow profile for SMD devices (C0353-APN-06) for reflow diagram and details

8. Electrical specifications

8.1 Preliminary DC characteristics: absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 20. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1,2)	$V_{VDD\_3.3}$	-0.3	3.3	3.63	V
1.2 V supply voltages (1.2)	$V_{VDD\_1.2}$	-0.3	1.2	1.26	V
Input voltage for tolerance for 5 V I/O pin(1,2)	$V_{IN5Vtol}$	-0.3	-	5.5	V
Input voltage tolerance for 3.3 V I/O pin(1,2)	$V_{IN3V3tol}$	-0.3	-	3.63	V
ESD - Human Body Model (HBM)	V_{ESD}	-	-	±2	kV
ESD - Charged Device Model (CDM)	V_{ESD}	-	-	±450	V
Latch-up	I_{LA}	-	-	±200	mA
Ambient operating temperature	T_A	0	-	70	°C
Storage temperature	T_{STG}	-40	-	125	°C
Operating junction temperature	T_J	0	-	125	°C
Thermal resistance (Junction to Ambient)	θ_{JA}	-	36.5	-	°C/W
PSI (J-C) (Junction to Case)	ψ_{JC}	-	1.6	-	°C/W
Peak IR reflow soldering temperature (<10 sec.)	T_{SOL}	-	-	260	°C

Note (1): All voltages are measured with respect to GND.

Note (2): Absolute maximum voltage ranges are for transient voltage excursions.

8.2 DC characteristics

Table 21. DC characteristics

Parameter	Symbol	Min	Typ	Max(1)	Units
Power					
3.3 V supply voltages (analog and digital)	$V_{VDD\_3.3}$	3.14	3.3	3.47	V
1.2 V supply voltages (analog and digital)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
Power					
Measurement conditions: 4K x 2K / 60 Hz MST (2K x 2K, two streams) Test pattern: ON-OFF dot				914	mW
Sleep mode			30		mW
Supply current					
Measurement conditions: 4K x 2K / 60 Hz MST (2K x 2K, two streams) Test pattern: ON-OFF dot Moire In all configurations, 8 bits output is used		-		-	mA
VDD (analog and digital power) = 3.3 V				58	
VDD (analog and digital power) = 1.2 V				565	
Inputs					
High voltage	V_{IH}	2.0	-	-	V
Low voltage	V_{IL}	-	-	0.8	V
Input hysteresis voltage	V_{HYST}	300	-	-	mV
High current (V_{IN} = 3.3 V)	I_{IH}	-	-	±10	µA
Low current (V_{IN} = 0 V)	I_{IL}	-	-	±10	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}	-	-	5	pF
Outputs					
High voltage (I_{OH} = 8 mA)	V_{OH}	2.4	-	-	V
Low voltage (I_{OL} = -8 mA)	V_{OL}	-	-	0.4	V
Tri-state leakage current	I_{OZ}	-	-	±10	µA

Note: The values in the Max column represent absolute maximum current consumption under high voltage (+5%) and nominal temperature. These values are measured in an environment that includes some discreet components. Other conditions include: a) Power measurement values are to be used for regulator sizing only, and not directly for package thermal calculations. b) IC performance is only guaranteed when operating within the "DC Characteristics". c) All inputs are 3.3 V tolerant.

8.3 AC characteristics

Table 22. Maximum speed of operation

Clock domain	Max speed of operation
Reference Input Clock (TCLK)	27 MHz
Reference Internal Clock (RCLK)	324 MHz
On-Chip Microcontroller Clock (OCLK)	150 MHz
SPDIF audio output	192 kHz
2-Wire Serial Slave (SLAVE_SCL)	400 kHz
2-Wire DDC2bi Slave (HDMI_SCL)	400 kHz
2-Wire Serial Master (MSTRx_SCL)	400 kHz

8.3.1 DisplayPort receiver

Table 23. DisplayPort receiver electrical parameters

Parameter	Symbol	Min	Typ	Max	Units	Comments
DisplayPort receiver system parameters						
HBR2 unit interval (5.4 Gbps)	UI_HBR2	-	185	-	ps	DisplayPort link RX does not require local crystal for link clock generation
HBR unit interval (2.7 Gbps)	UI_HBR	-	370	-	ps	
RBR unit interval (1.62 Gbps)	UI_RBR	-	617	-	ps	
Link clock down spreading	Down spread amplitude	0	-	0.5	%	Modulation frequency range 0f 30 kHz to 33 kHz
DisplayPort receiver TP3 parameters						
Minimum receiver eye width at Rx-side connector pins	T_{RX-EYE_CONN}	0.25	-	-	UI	For RBR
Lane intra-pair skew tolerance	$L_{RX-SKEW\_INTRA\_PAIR\_HBR2}$	-	-	50	ps	For HBR2. Represents the skew contribution from the cable in addition to the stressed EYE at TP3_EQ.
Lane intra-pair skew tolerance	$L_{RX-SKEW\_INTRA\_PAIR\_HBR}$	-	-	60	ps	For HBR. Represents the skew contribution from the cable in addition to the stressed EYE at TP3.
Lane intra-pair skew tolerance	$L_{RX-SKEW\_INTRA\_PAIR\_RBR}$	-	-	260	ps	For RBR. Represents the skew contribution from the cable in addition to the stressed EYE at TP3.
Jitter closed loop tracking bandwidth	$F_{RX-TRACKING-BW\_RBR}$	5.4	-	-	MHz	Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern
Jitter closed loop tracking bandwidth	$F_{RX-TRACKING-BW\_HBR}$	10	-	-	MHz	Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern
Jitter closed loop tracking bandwidth	$F_{RX-TRACKING-BW\_HBR2}$	10	-	-	MHz	Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern
DisplayPort receiver TP3_EQ parameters						
Minimum receiver eye width	$T_{RX-TJ\_8b10b\_HBR2}$	0.38	-	-	UI	For HBR2. Measured at 1E-9 BER using HBR2 Compliance EYE pattern.
RX differential peak-to-peak EYE voltage	$T_{RX-DIFFp-p\_HBR2}$	90	-	-	mV	For HBR2. Measured at 1E-9 BER using HBR2 compliance EYE pattern.

8.3.2 DisplayPort transmitter

Table 24. DisplayPort transmitter electrical parameters

Parameter	Symbol	Min	Typ	Max	Units	Comments
DisplayPort transmitter system parameters						
HBR2 unit interval (5.4Gbps)	UI_HBR2	-	185	-	ps	Frequency high limit = +300ppm Frequency low limit = 5300ppm
HBR unit interval (2.7Gbps)	UI_HBR	-	370	-	ps	
RBR unit interval (1.62Gbps)	UI_RBR	-	617	-	ps	
Link clock down spreading	Down spread amplitude	0	-	0.5	%	Modulation frequency range 0f 30 kHz to 33 kHz
DisplayPort transmitter TP2 parameters						
Ratio of output voltage level 1/level 0	$V_{TX-OUTPUT\_RATION\_RBR\_HBR}$	0.8	-	6.0	dB	Measured on non- transition bits at pre- emphasis level 0 setting
Ratio of output voltage level 2/level 1		0.1	-	5.1	dB	
Ratio of Output Voltage level 3/level 2		0.8	-	6.0	dB	
Ratio of output voltage level 1/level 0	$V_{TX-OUTPUT\_RATION\_RBR\_HBR2}$	5.2		6.9	dB	Measured on non- transition bits at pre- emphasis level 0 setting
Ratio of Output Voltage level 2/level 1		1.6		3.5		
Ratio of output voltage level 3/level 2		1		4.4		
Maximum pre-emphasis when disabled	$v_{TX-PREEMP-OFF}$			0.25	dB	
Max output voltage level	$v_{TX-DIFFp-p-MAX}$			1.2	V	
Lane-to-lane output skew	$L_{TX-SKEW-INTER\_PAIR\_HBR\_RBR}$			2	UI	Applied to all pairwise combinations of supported lanes.
Lane-to-lane output skew	$L_{TX-SKEW-INTER\_PAIR\_HBR2}$			4 UI + 500 ps		Applied to all pairwise combinations of supported lanes.
Lane intra-pair output skew	$L_{TX-SKEW-INTRA\_PAIR}$			30	ps	Applies to all support lanes.
Delta of pre-emphasis level 1 vs. level 0	$V_{TX-PREEMP-DELTA}$	2			dB	Applied to all valid voltage settings. No Pre-emphasis Post Cursor2 applied.
Delta of pre-emphasis level 2 vs. level 1		1.6			dB	
Delta of pre-emphasis level 3 vs. level 2		1.6			dB	
Non-transition reduction output voltage level 2	$V_{TX-DIFF\_REDUCTION}$			3	dB	V_{Tx_DIFF} at each non- zero nominal pre- emphasis level must not be lower than the specific amount less than V_{Tx_DIFF} at the zero nominal pre- emphasis level. Modulation frequency range 0f 30 kHz to 33 kHz
Non-transition reduction output voltage level 1				3	dB	
Non-transition reduction output voltage level 0				1.4	dB	

Table 24. DisplayPort transmitter electrical parameters (continue)

Parameter	Symbol	Min	Typ	Max	Units	Comments
DisplayPort transmitter TP3_EQ parameters						
Maximum TX total jitter	$T_{TX-TJ\_8b10b\_HBR2}$			0.62	UI	For HBR2. Measured at 1E-9 BER using HBR2 compliance EYE pattern.
Maximum TX deterministic Jjtter	$T_{TX-DJ\_8b10b\_HBR2}$			0.49	UI	
Maximum TX total jitter	$T_{TX-TJ\_D10.2\_HBR2}$			0.4	UI	For HBR2. Measured at 1E-9 BER using D10.2 compliance pattern.
Maximum TX deterministic jitter	$T_{TX-DJ\_D10.2\_HBR2}$			0.25	UI	
Maximum TX random jitter	$T_{TX-RJ\_D10.2\_HBR2}$			0.23	UI	
TX Differential reak-to-peak EYE voltage	$T_{TX-DIFFp-p\_HBR2}$	110			mV	For HBR2. Measured at 1E-9 BER using HBR2 compliance EYE pattern.

8.3.3 HDMI receiver

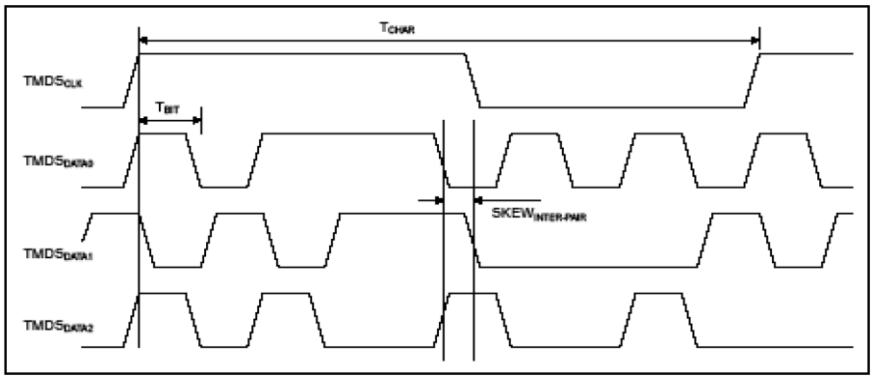
Table 25. HDMI receiver DC characteristics

DC characteristics	Min	Typ	Max	Units	Comments
Input Differential Voltage Level	150		1200	mV	
Input Common Mode Voltage,V_{icm1}	AV_{cc}-400 mV		AV_{cc}-37.5 mV		

Table 26. HDMI receiver AC characteristics

AC characteristics	Min	Typ	Max	Units	Comments
Input clock frequency	25		297	MHz	
Differential input (peak-to-peak)	150		1560	mV	
Intra-pair skew tolerance			0.4	T_{bit}	TMDS clock rates 222.75 MHz and below
Inter-pair skew tolerance			$0.2T_{bit}$ + 112 ps	ps	TMDS clock rates above 222.75 MHz
Input clock jitter tolerance			0.3	T_{bit}	

Figure 19. HDMI and DVI receiver AC characteristics



8.3.4 HDMI transmitter

Table 27. HDMI transmitter (DP++) DC characteristics

DC characteristics	Min	Typ	Max	Units	Comments
Single-ended output voltage	400	500		mV	
Single-ended high level output voltage, V_H		AV_{DD}			AV_{DD}=1.2 volt
Single-ended low level output voltage, V_L		AV_{DD} -500 mV			AV_{DD}=1.2 volt

Table 28. HDMI transmitter AC characteristics

DC characteristics	Min	Typ	Max	Units	Comments
Intra-pair skew at source connector, max	-	-	0.15	T_{bit}	
Intra-pair skew at source connector, max	-	-	0.2	$T_{character}$	
TMDS differential clock jitter,max	-	-	0.25	T_{bit}	
Rise time/fall time	75	-	-	ps	

8.3.5 Crystal specification

Mode: fundamental

Table 29. Crystal specifications

Parameters	Min	Typ	Max	Units	Comments
Nominal frequency	-	27	-	MHz	
Tolerance	-	± 50	-	ppm	
Load capacitance	-	22	-	pF	
ESR (effective series resistance)	-	-	40	Ohm	
Drive level	-	-	100	uW	
Shunt capacitance	-	7	-	pF	

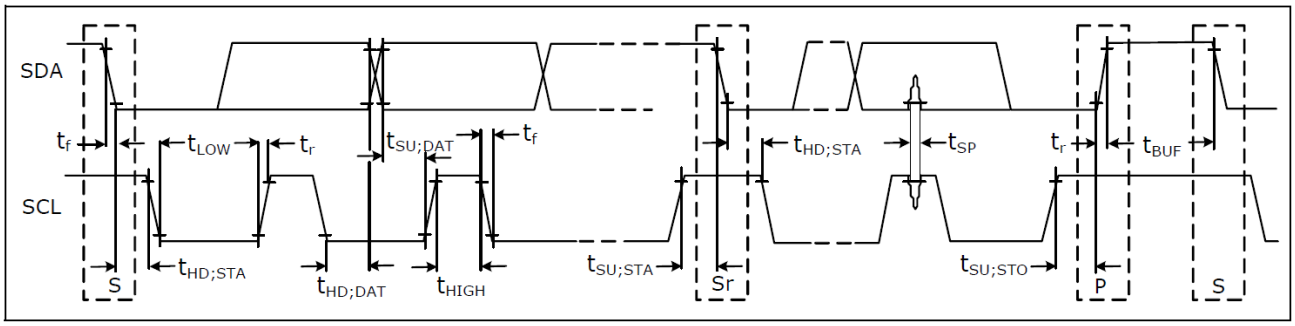
8.3.6 I2C interface timing

Table 30. I2C interface timing

Symbol	Parameter	Conditions	Min	Measured	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	393	400	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	0.6	0.95	-	µs
t_{LOW}	Low period of clock	SCL	1.3	1.1	-	µs
t_{HIGH}	High period of clock	SCL	0.6	0.75	-	µs
$T_{su;STA}$	Setup time for a repeated START		0.6	1.09	-	µs
$t_{HD;DAT}$	Data hold time		0	0.96	0.9(1)	µs
$t_{SU;DAT}$	Data setup time		100	600	-	ns
T_{BUF}	Bus free time between STOP and START		1.3	1.7 ms	-	µs
C_b	Capacitance load for each bus line		-		400	pF
t_r	Rise time		20	220	300	ns
t_f	Fall time		20	25	300	ns
V_{nh}	Noise margin at high level		0.2 VDD	0.3	-	V
V_{nl}	Noise margin at low level		0.1 VDD	0.28	-	V

Note: The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.

Figure 20. I2C timing



8.3.7 SPI interface timing

Table 31. SPI interface timing, VDD = 3.3 V

Symbol	Parameter	Min	Typ	Max	Units
F_{CLK}	Serial clock frequency	-		75	MHz
T_{SCKH}	Serial clock high time	6		-	ns
T_{SCKL}	Serial clock low time	6		-	ns
T_{SCKR}	Serial clock rise time (slew rate)	-	3.0	-	V/ns
T_{SCKF}	Serial clock fall time (slew rate)	-	3.0	-	V/ns
T_{CES}	CE# active setup time	5		-	ns
T_{CEH}	CE# active hold time	5		-	ns
T_{CHS}	CE# not active setup time	5		-	ns
T_{CHH}	CE# not active hold time	5		-	ns
T_{CPH}	CE# high time	50		-	ns
T_{CHZ}	CE# high to high-Z output	-		7	ns
T_{CLZ}	SCK low to low-Z output	0		-	ns
T_{DS}	Data in setup time	2		-	ns
T_{DH}	Data in hold time	2		-	ns
T_{OH}	Output hold from SCK change	0		-	ns
T_V	Output valid from SCK	1.5	3.5	-	ns

Figure 21. SPI input timing

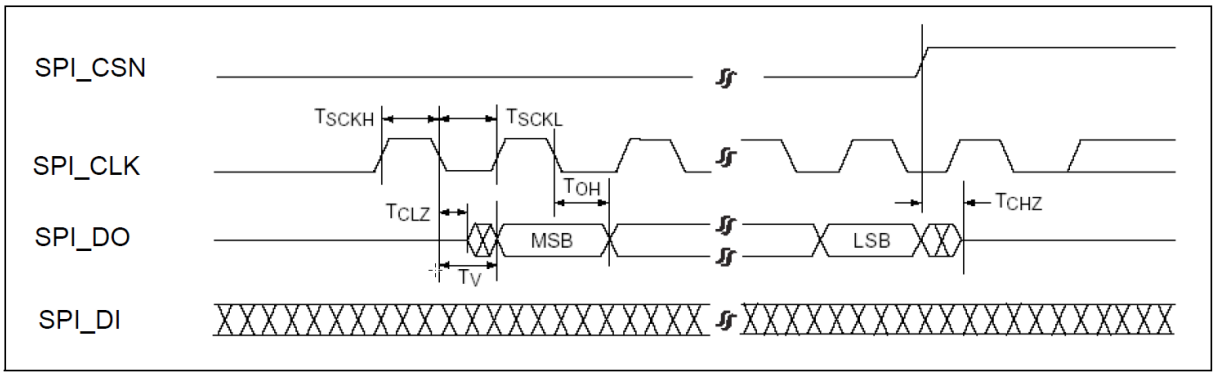
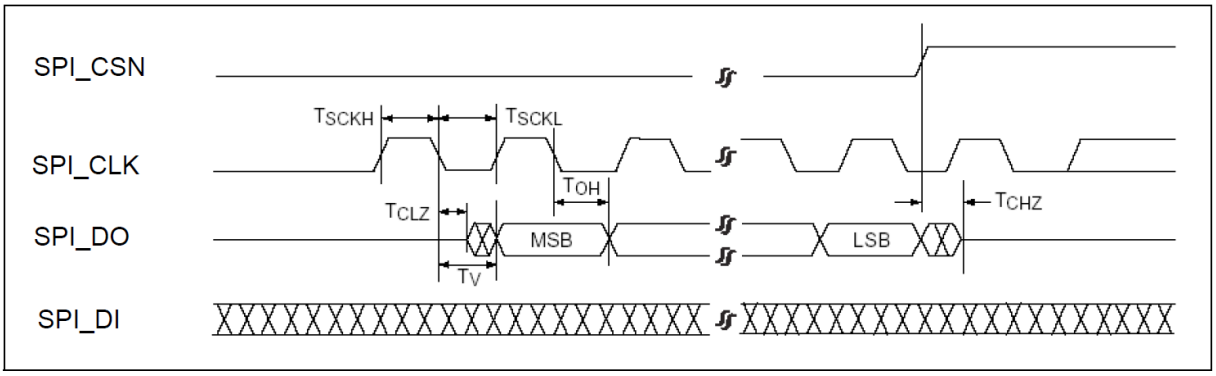


Figure 22. SPI output timing



9. Ordering information

Table 32. Order codes

Part Number	Operating Temperature	Package
STDP4320-BA	0°C to +70°C	172 LFBGA (12 x 12 mm)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Kinetic Technologies:

STDP4320-BA RD5-4320