

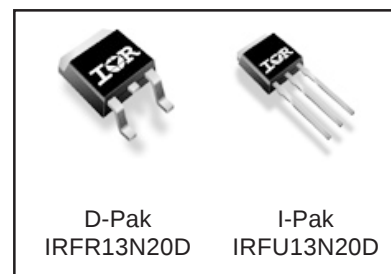
Applications

- High frequency DC-DC converters

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	0.235 Ω	13A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	13	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	9.2	
I_{DM}	Pulsed Drain Current ①	52	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	2.2	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Telecom 48V input Forward Converters

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.235	Ω	$V_{GS} = 10V, I_D = 8.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	6.2	—	—	S	$V_{DS} = 50V, I_D = 7.8A$
Q_g	Total Gate Charge	—	25	38	nC	$I_D = 7.8A$
Q_{gs}	Gate-to-Source Charge	—	7.3	11		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	12	18		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	27	—		$I_D = 7.8A$
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	10	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	830	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	140	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	35	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	990	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	57	—		$V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	59	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	130	mJ
I_{AR}	Avalanche Current①	—	7.8	A
E_{AR}	Repetitive Avalanche Energy①	—	11	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	13	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	52		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 7.8A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	140	210	ns	$T_J = 25^\circ\text{C}, I_F = 7.8A$
Q_{rr}	Reverse Recovery Charge	—	750	1120	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

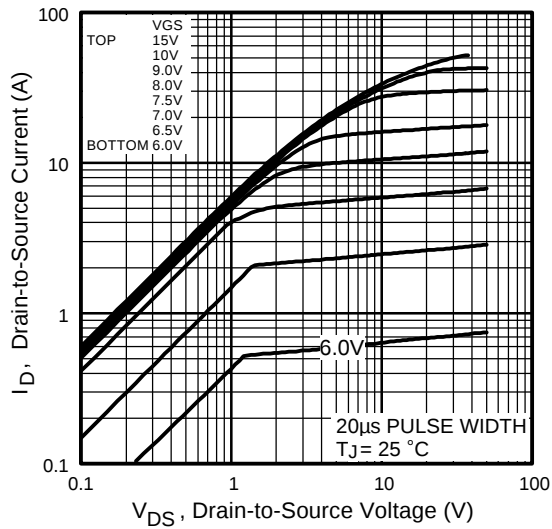


Fig 1. Typical Output Characteristics

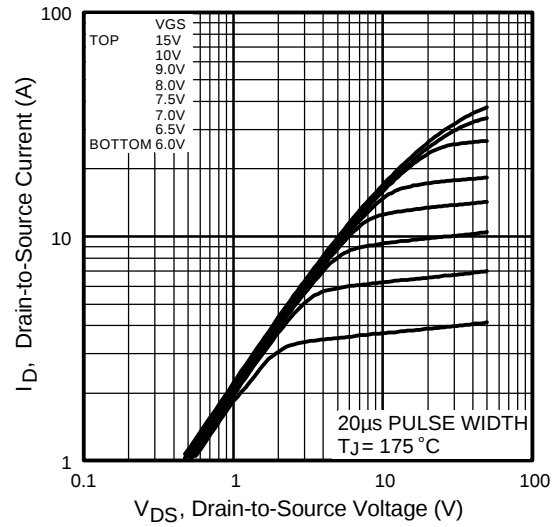


Fig 2. Typical Output Characteristics

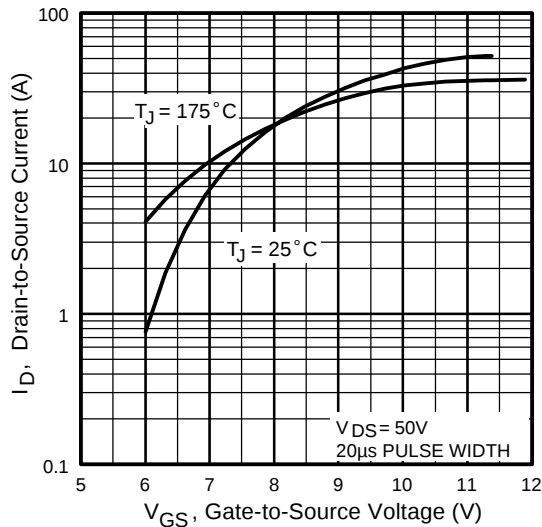


Fig 3. Typical Transfer Characteristics

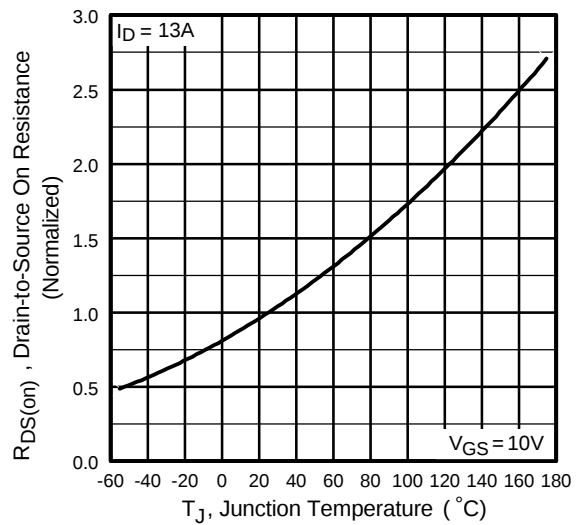


Fig 4. Normalized On-Resistance Vs. Temperature

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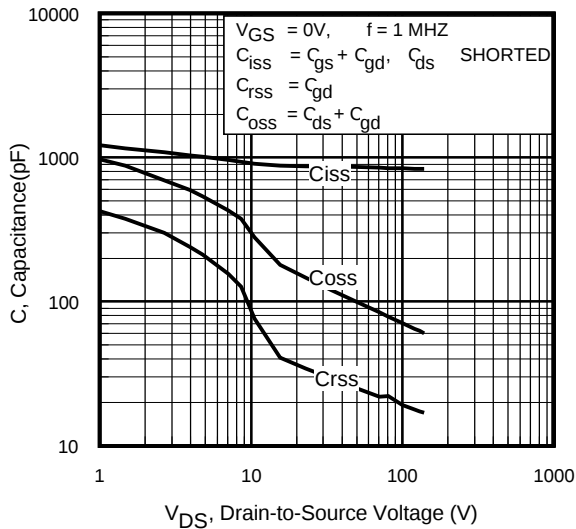


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

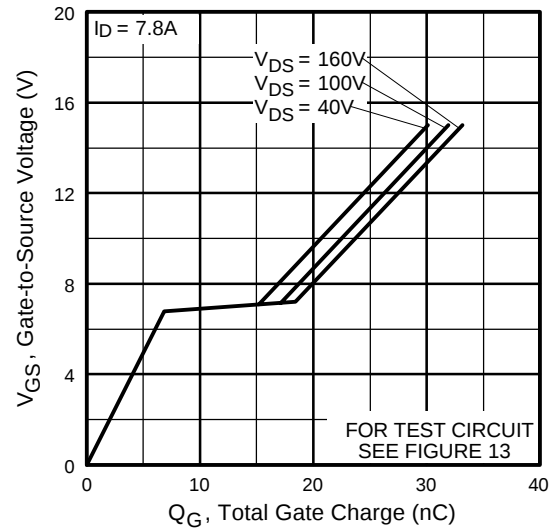


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

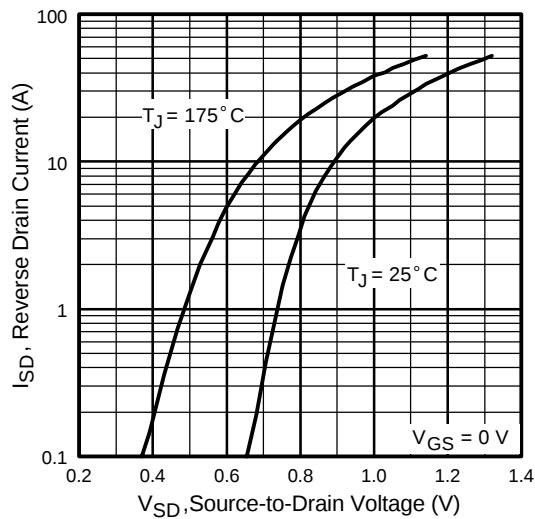


Fig 7. Typical Source-Drain Diode Forward Voltage

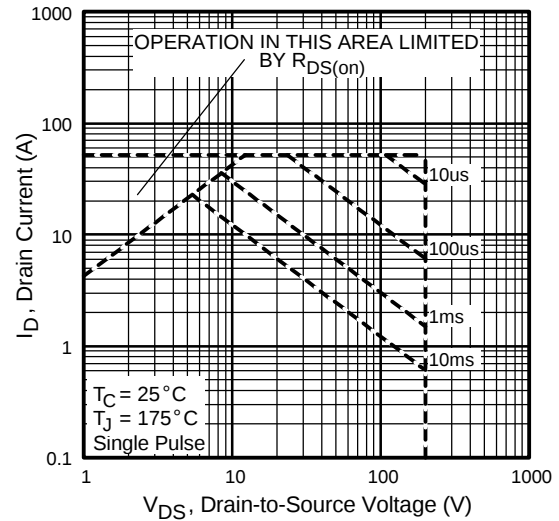


Fig 8. Maximum Safe Operating Area

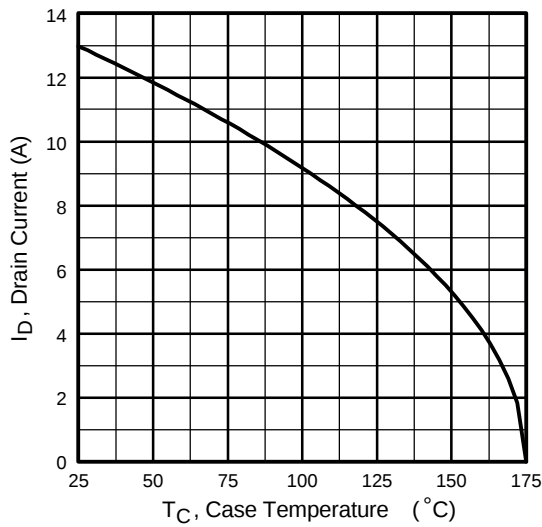


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

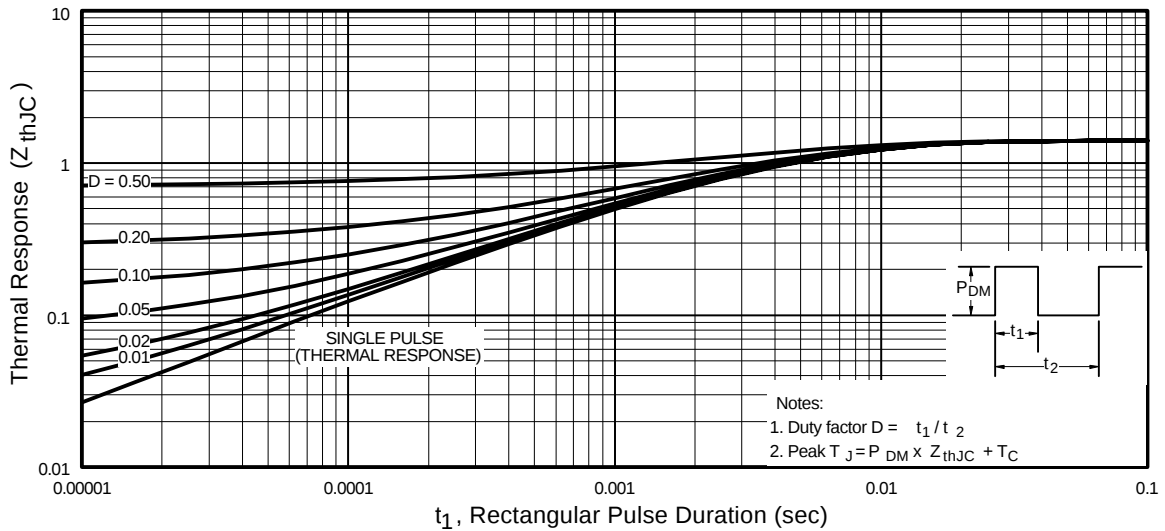


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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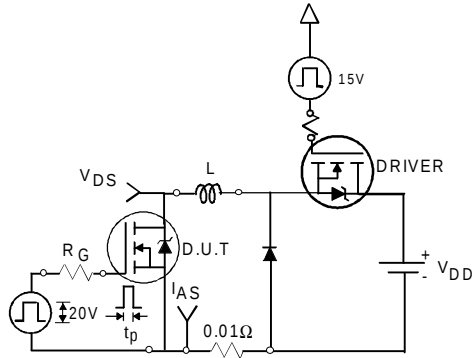


Fig 12a. Unclamped Inductive Test Circuit

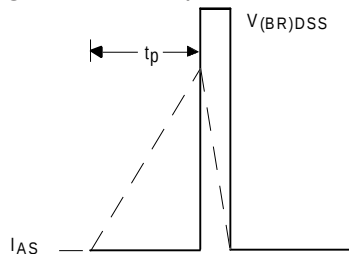


Fig 12b. Unclamped Inductive Waveforms

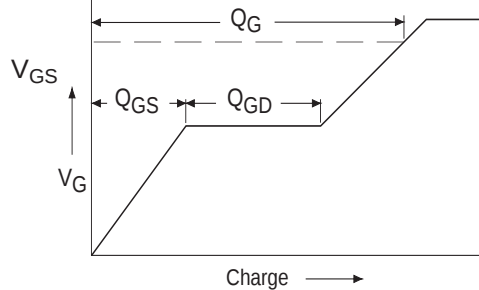


Fig 13a. Basic Gate Charge Waveform

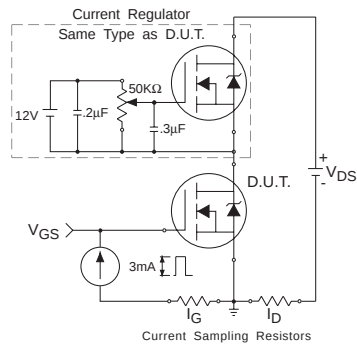


Fig 13b. Gate Charge Test Circuit

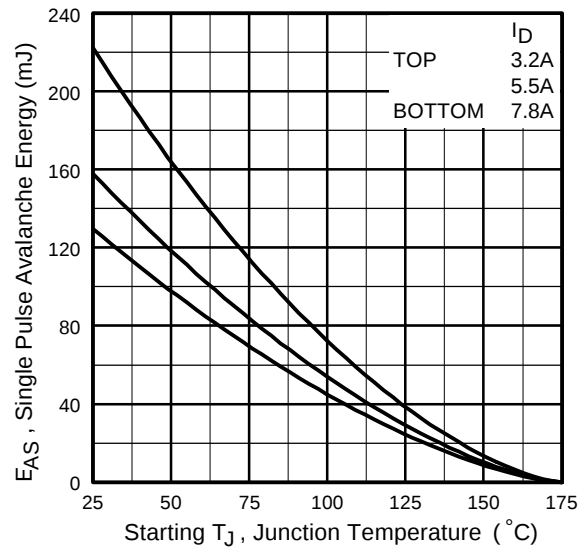


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

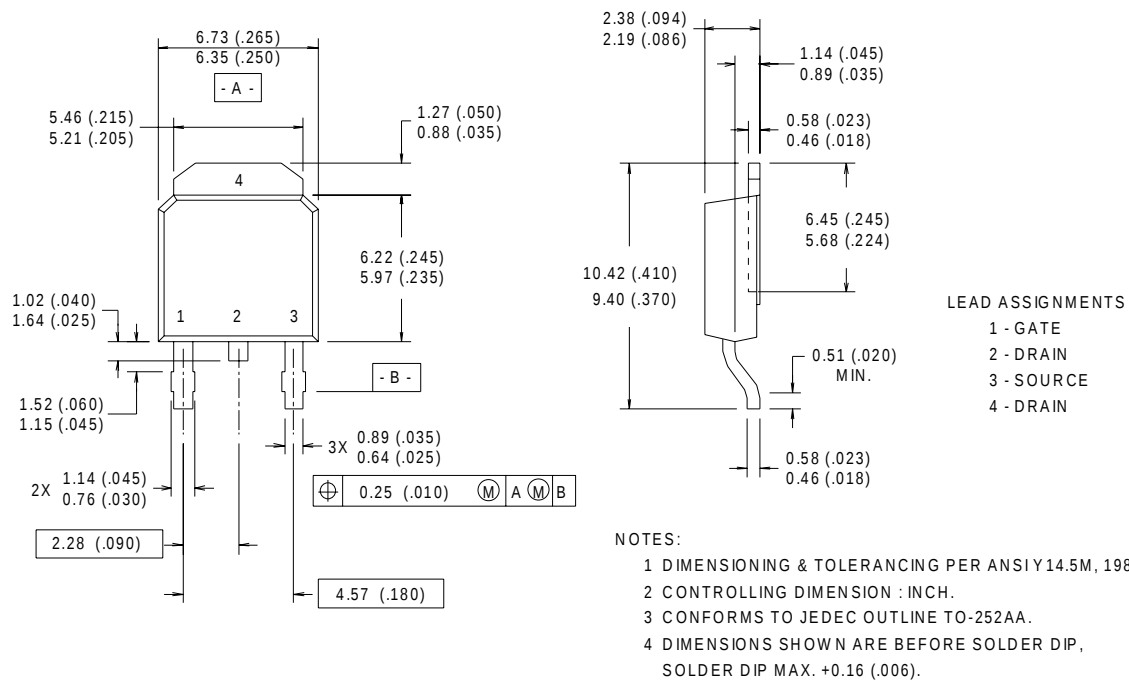
Fig 14. For N-Channel HEXFET® Power MOSFETs

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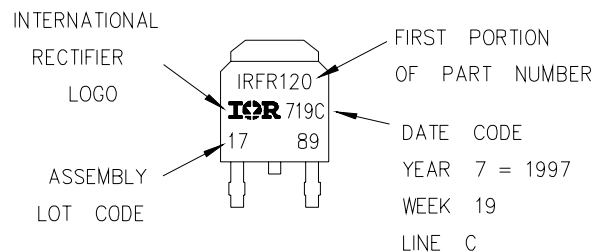
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



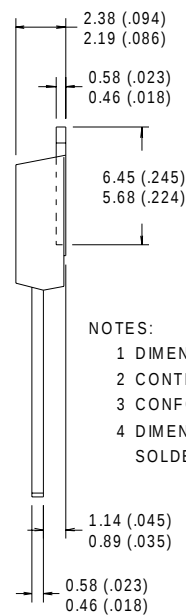
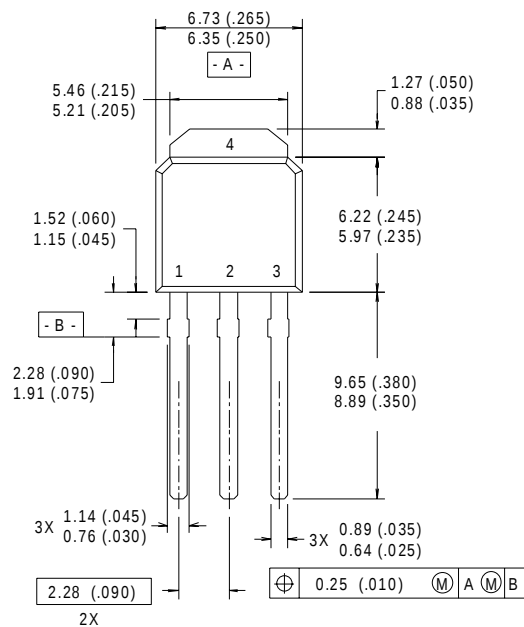
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

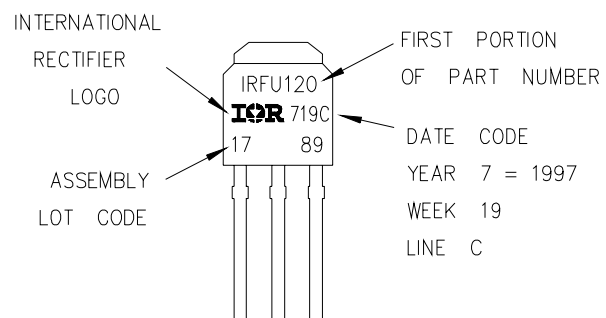
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
- 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

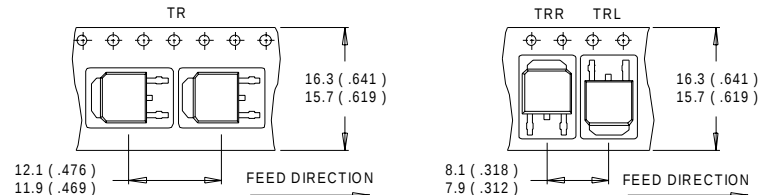


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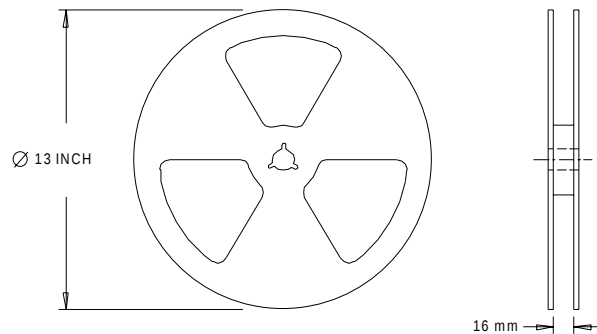
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 - ② Starting $T_J = 25^\circ\text{C}$, $L = 4.3\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 7.8\text{A}$.
 - ③ $I_{SD} \leq 7.8\text{A}$, $di/dt \leq 81\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
 - ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 - ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- * When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

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Data and specifications subject to change without notice. 2/2000

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