

## (Features)

- Low-voltage and Standard-voltage Operation
  - 1.8 ( $V_{CC} = 1.8$  to 5.5V)
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1 MHz (5.0V) and 400 KHz (1.8V Compatibility)
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Lead-free/Halogen-free Devices
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, 8-lead Ultra Thin Mini-MAP (MLP2x3), and 8-ball dBGAA2 Packages.
- Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers

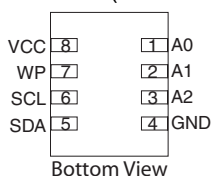
## Description

The AT24C32C/64C provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32C/64C is available in space saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, 8-lead Ultra Thin Mini-MAP (MLP2x3) and, 8-ball dBGAA2 packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 1.8V (1.8 to 5.5V) version.

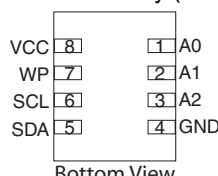
## Pin Configurations

| Pin Name | Function           |
|----------|--------------------|
| A0 - A2  | Address Inputs     |
| SDA      | Serial Data        |
| SCL      | Serial Clock Input |
| WP       | Write Protect      |

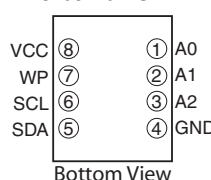
8-lead Ultra Thin Mini-MAP (MLP 2x3)



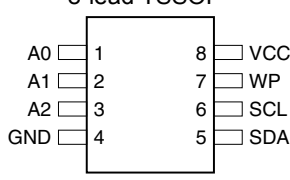
8-lead Ultra Lead Frame Land Grid Array (ULA)



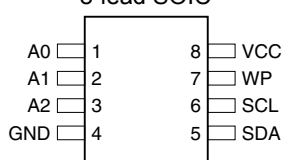
8-ball dBGAA2



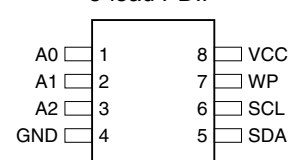
8-lead TSSOP



8-lead SOIC



8-lead PDIP



## 2-Wire Serial EEPROM

32K (4096 x 8)

64K (8192 x 8)

## AT24C32C AT24C64C

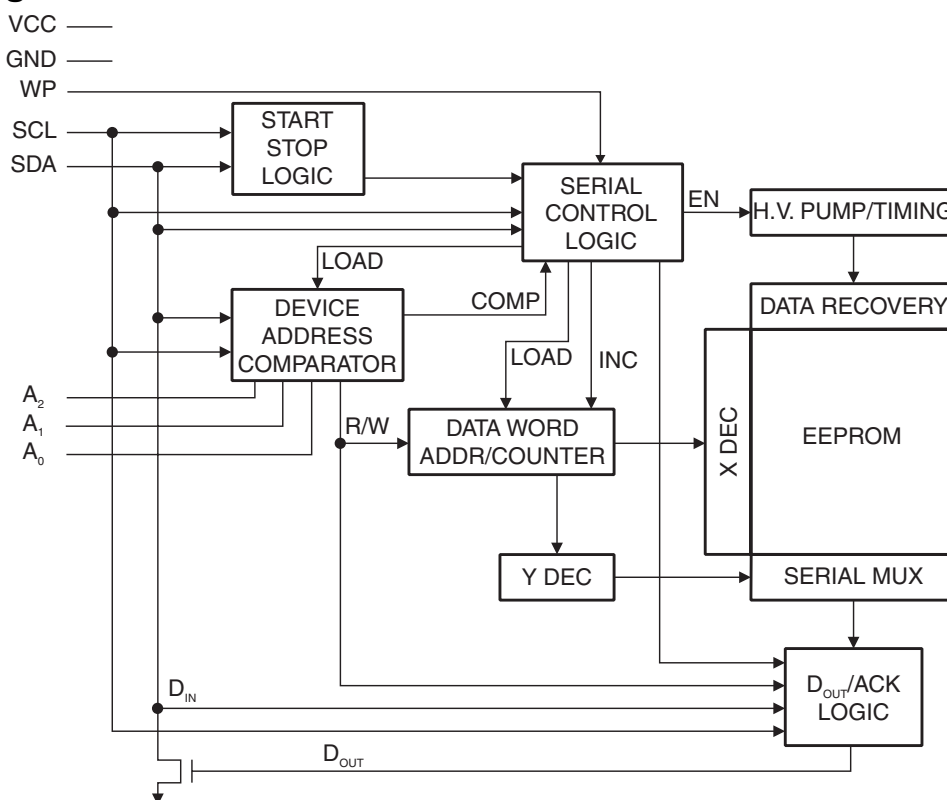


## Absolute Maximum Ratings\*

|                                                    |               |
|----------------------------------------------------|---------------|
| Operating Temperature.....                         | -55 to +125°C |
| Storage Temperature .....                          | -65 to +150°C |
| Voltage on Any Pin<br>with Respect to Ground ..... | -1.0 to +7.0V |
| Maximum Operating Voltage .....                    | 6.25V         |
| DC Output Current.....                             | 5.0 mA        |

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 1. Block Diagram



## 2. Pin Description

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

**DEVICE/ADDRESSES (A2, A1, A0):** The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with other AT24CXX devices. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board  $V_{CC}$  plane is  $<3\text{pF}$ . If coupling is  $>3\text{pF}$ , Atmel® recommends connecting the address pins to GND.

**WRITE PROTECT (WP):** The write protect input, when connected to GND, allows normal write operations. When WP is connected high to  $V_{CC}$ , all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board  $V_{CC}$  plane is  $<3\text{pF}$ . If coupling is  $>3\text{pF}$ , Atmel recommends connecting the pin to GND.

### 3. Memory Organization

**AT24C32C/64C, 32/64K SERIAL EEPROM:** The 32K/64K is internally organized as 128/256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

#### Pin Capacitance<sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +1.8\text{V}$  to  $5.5\text{V}$

| Symbol    | Test Condition                             | Max | Units | Conditions            |
|-----------|--------------------------------------------|-----|-------|-----------------------|
| $C_{I/O}$ | Input/Output Capacitance (SDA)             | 8   | pF    | $V_{I/O} = 0\text{V}$ |
| $C_{IN}$  | Input Capacitance ( $A_0, A_1, A_2, SCL$ ) | 6   | pF    | $V_{IN} = 0\text{V}$  |

Note: 1. This parameter is characterized and is not 100% tested.

#### DC Characteristics

Applicable over recommended operating range from:  $T_{AI} = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +1.8$  to  $+5.5\text{V}$  (unless otherwise noted)

| Symbol           | Parameter                                     | Test Condition                                        |                                                      | Min                   | Typ  | Max                   | Units |
|------------------|-----------------------------------------------|-------------------------------------------------------|------------------------------------------------------|-----------------------|------|-----------------------|-------|
| V <sub>CC1</sub> | Supply Voltage                                |                                                       |                                                      | 1.8                   |      | 5.5                   | V     |
| I <sub>CC1</sub> | Supply Current                                | V <sub>CC</sub> = 5.0V                                | READ at 400 kHz                                      |                       | 0.4  | 1.0                   | mA    |
| I <sub>CC2</sub> | Supply Current                                | V <sub>CC</sub> = 5.0V                                | WRITE at 400 kHz                                     |                       | 2.0  | 3.0                   | mA    |
| I <sub>SB1</sub> | Standby Current (1.8V option)                 | V <sub>CC</sub> = 1.8V                                | V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub> |                       |      | 1.0                   | μA    |
|                  |                                               | V <sub>CC</sub> = 5.5V                                |                                                      |                       |      | 6.0                   | μA    |
| I <sub>LI</sub>  | Input Leakage Current V <sub>CC</sub> = 5.0V  | V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub>  |                                                      |                       | 0.10 | 3.0                   | μA    |
| I <sub>LO</sub>  | Output Leakage Current V <sub>CC</sub> = 5.0V | V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub> |                                                      |                       | 0.05 | 3.0                   | μA    |
| V <sub>IL</sub>  | Input Low Level <sup>(1)</sup>                |                                                       |                                                      | −0.6                  |      | V <sub>CC</sub> × 0.3 | V     |
| V <sub>IH</sub>  | Input High Level <sup>(1)</sup>               |                                                       |                                                      | V <sub>CC</sub> × 0.7 |      | V <sub>CC</sub> + 0.5 | V     |
| V <sub>OL2</sub> | Output Low Level                              | V <sub>CC</sub> = 3.0V                                | I <sub>OL</sub> = 2.1 mA                             |                       |      | 0.4                   | V     |
| V <sub>OL1</sub> | Output Low Level                              | V <sub>CC</sub> = 1.8V                                | I <sub>OL</sub> = 0.15 mA                            |                       |      | 0.2                   | V     |

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.

## AC Characteristics

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $CL = 1$  TTL Gate and 100 pF (unless otherwise noted)

| Symbol                   | Parameter                                                                    | 1.8-volt  |     | 5.0-volt |      | Units         |
|--------------------------|------------------------------------------------------------------------------|-----------|-----|----------|------|---------------|
|                          |                                                                              | Min       | Max | Min      | Max  |               |
| $f_{SCL}$                | Clock Frequency, SCL                                                         |           | 400 |          | 1000 | kHz           |
| $t_{LOW}$                | Clock Pulse Width Low                                                        | 1.3       |     | 0.4      |      | $\mu\text{s}$ |
| $t_{HIGH}$               | Clock Pulse Width High                                                       | 0.6       |     | 0.4      |      | $\mu\text{s}$ |
| $t_i$                    | Noise Suppression Time <sup>(1)</sup>                                        |           | 100 |          | 50   | ns            |
| $t_{AA}$                 | Clock Low to Data Out Valid                                                  | 0.05      | 0.9 | 0.05     | 0.55 | $\mu\text{s}$ |
| $t_{BUF}$                | Time the bus must be free before a new transmission can start <sup>(1)</sup> | 1.3       |     | 0.5      |      | $\mu\text{s}$ |
| $t_{HD,STA}$             | Start Hold Time                                                              | 0.6       |     | 0.25     |      | $\mu\text{s}$ |
| $t_{SU,STA}$             | Start Set-up Time                                                            | 0.6       |     | 0.25     |      | $\mu\text{s}$ |
| $t_{HD,DAT}$             | Data In Hold Time                                                            | 0         |     | 0        |      | $\mu\text{s}$ |
| $t_{SU,DAT}$             | Data In Set-up Time                                                          | 100       |     | 100      |      | ns            |
| $t_R$                    | Inputs Rise Time <sup>(1)</sup>                                              |           | 0.3 |          | 0.3  | $\mu\text{s}$ |
| $t_F$                    | Inputs Fall Time <sup>(1)</sup>                                              |           | 300 |          | 100  | ns            |
| $t_{SU,STO}$             | Stop Set-up Time                                                             | 0.6       |     | 0.25     |      | $\mu\text{s}$ |
| $t_{DH}$                 | Data Out Hold Time                                                           | 50        |     | 50       |      | ns            |
| $t_{WR}$                 | Write Cycle Time                                                             |           | 5   |          | 5    | ms            |
| Endurance <sup>(1)</sup> | 25°C, Page Mode, 3.3V                                                        | 1,000,000 |     |          |      | Write Cycles  |

- Notes:
1. This parameter is ensured by characterization.
  2. AC measurement conditions:  
 $R_L$  (connects to  $V_{CC}$ ): 1.3 k $\Omega$  (2.5V, 5.0V), 10 k $\Omega$  (1.8V)  
 Input pulse voltages: 0.3  $V_{CC}$  to 0.7  $V_{CC}$   
 Input rise and fall times:  $\leq 50$  ns  
 Input and output timing reference voltages: 0.5  $V_{CC}$

## 4. Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

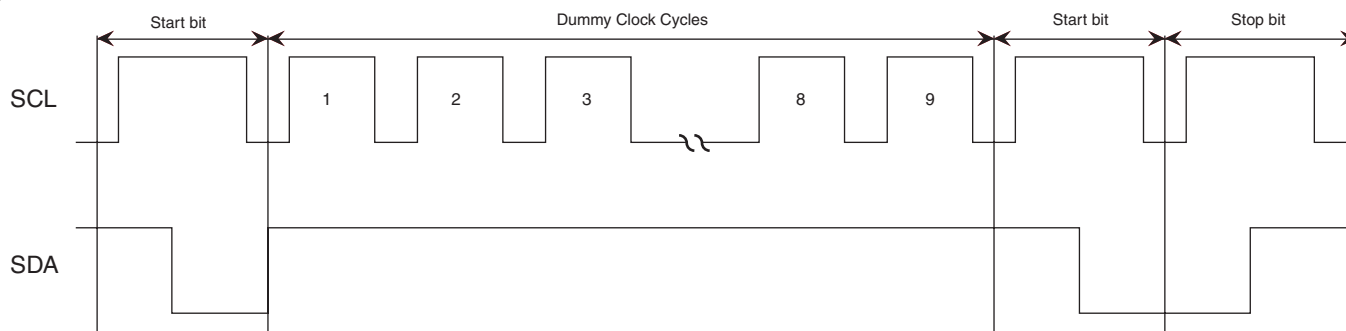
**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

**STANDBY MODE:** The AT24C32C/64C features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the Stop bit and the completion of any internal operations.

**SOFTWARE RESET:** After an interruption in protocol, power loss or system reset, and 2-wire part can be protocol reset by following these steps:

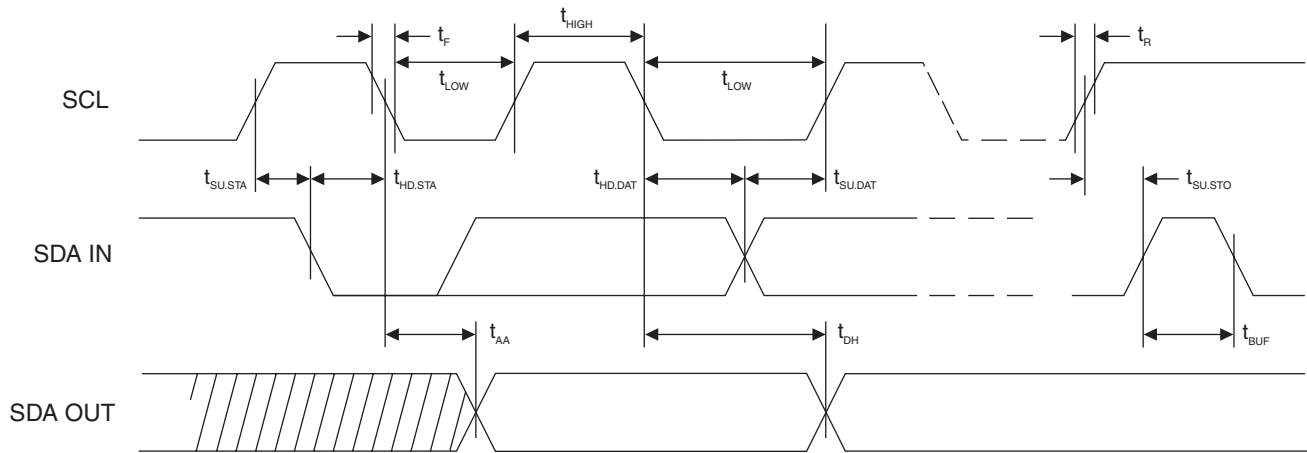
(a) Create a start bit condition, (b) clock 9 cycles, (c) create another start bit followed by stop bit condition as shown below. The device is ready for next communication after above steps have been completed.

**Figure 4-1.** Software Reset



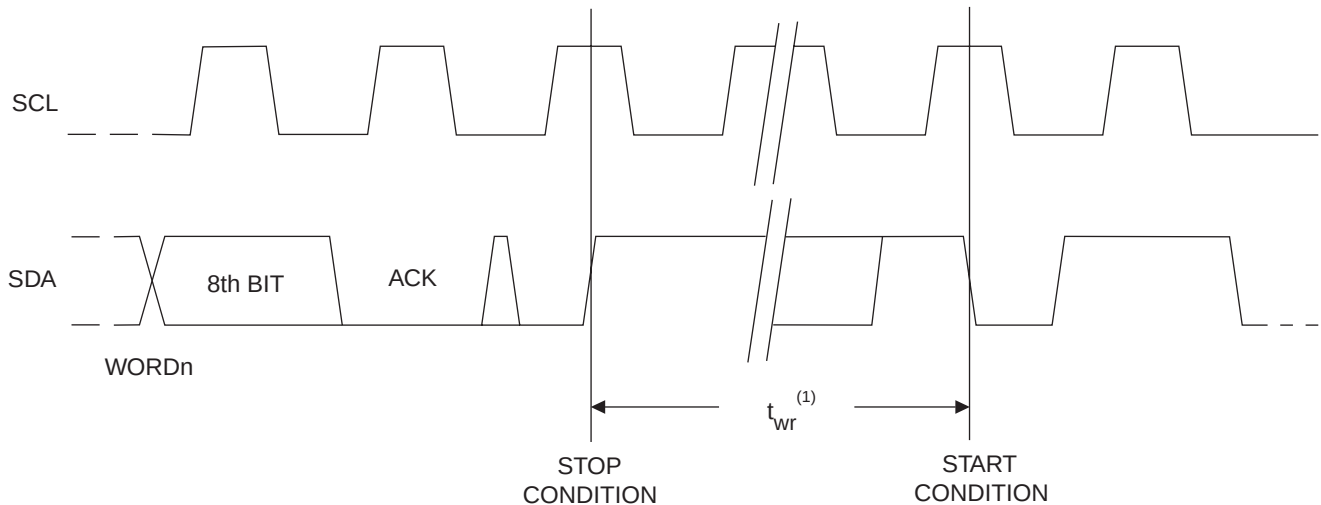
## 5. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O



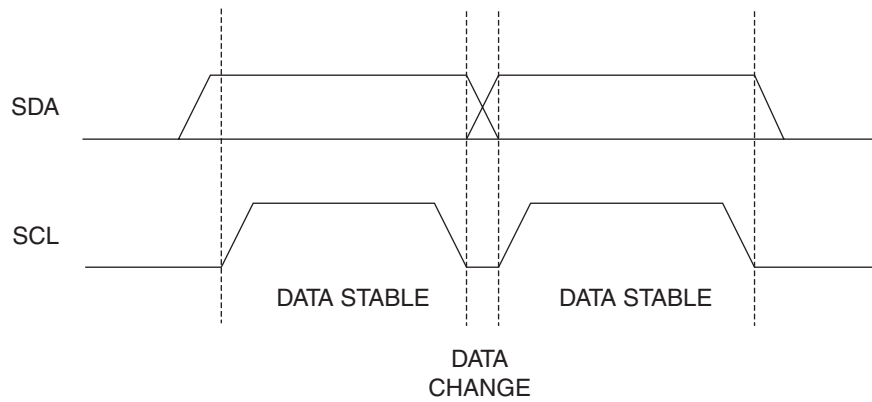
## 6. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O

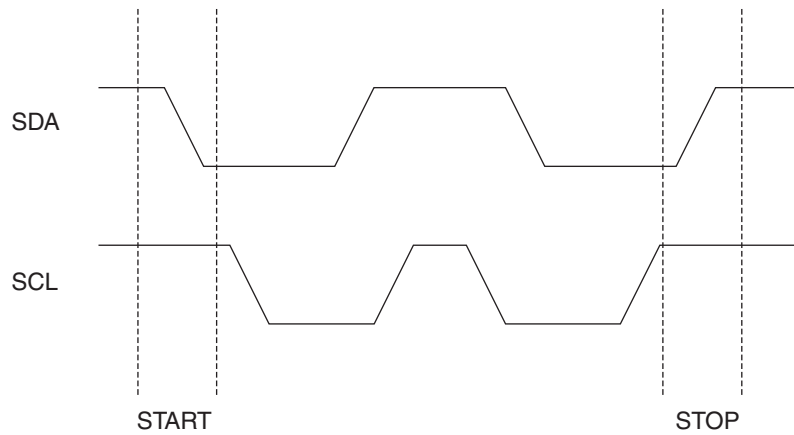


Note: 1. The write cycle time  $t_{wr}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

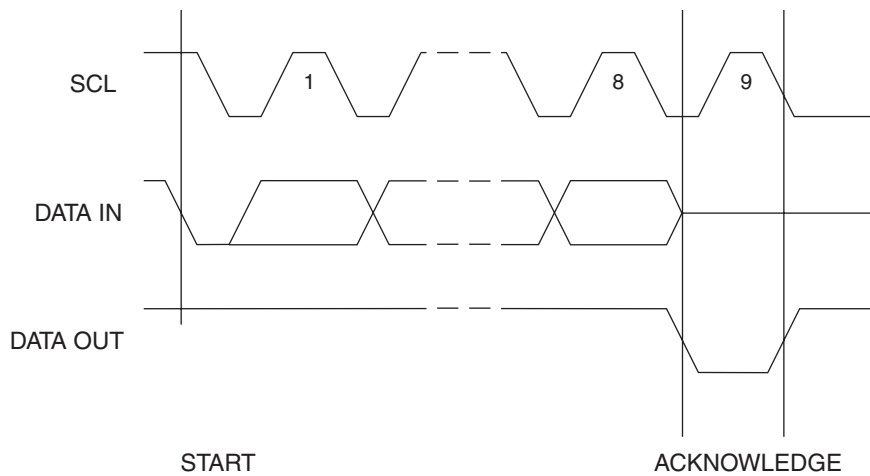
## 7. Data Validity



## 8. Start and Stop Definition



## 9. Output Acknowledge





## 10. Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see [Figure 12-1](#) on page 11). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

**DATA SECURITY:** The AT24C32C/64C has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at  $V_{CC}$ .

## 11. Write Operations

**BYTE WRITE:** A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see [Figure 12-2](#) on page 11).

**PAGE WRITE:** The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see [Figure 12-3](#) on page 11).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

**ACKNOWLEDGE POLLING:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

## 12. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

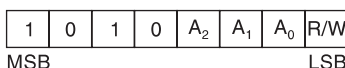
**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see [Figure 12-4](#) on page 12).

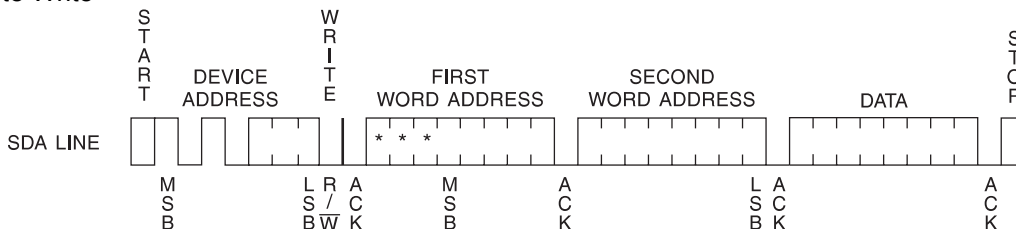
**RANDOM READ:** A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 12-5](#) on page 12).

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 12-6](#) on page 12).

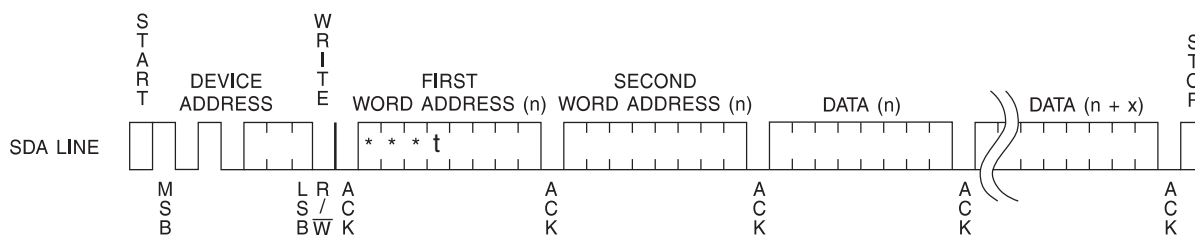
**Figure 12-1.** Device Address



**Figure 12-2.** Byte Write

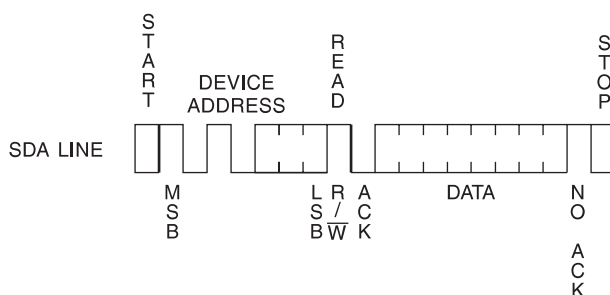


**Figure 12-3. Page Write**

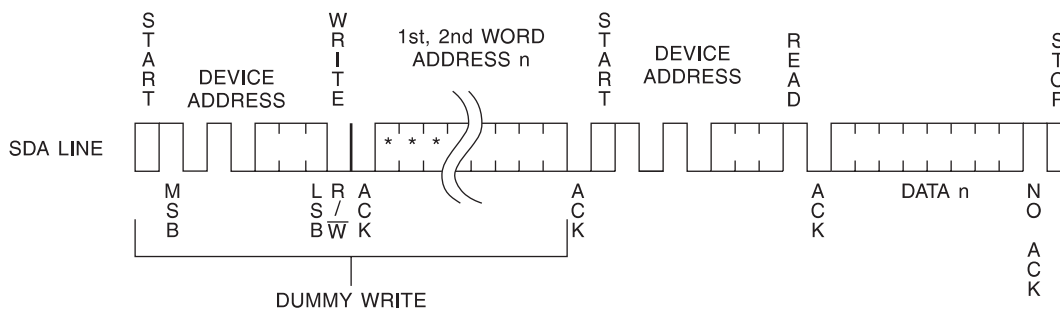


- Note:
1. \* = DON'T CARE bits
  2. t = DON'T CARE bit for AT24C32C

**Figure 12-4. Current Address Read**

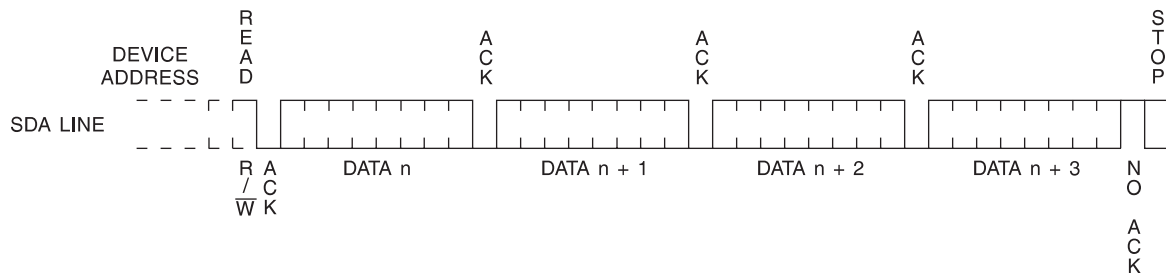


**Figure 12-5. Random Read**



- Note:
1. \* = DON'T CARE bits

**Figure 12-6. Sequential Read**



## AT24C32C Ordering Information

| Ordering Code                                       | Voltage | Package  | Operation Range                                                     |
|-----------------------------------------------------|---------|----------|---------------------------------------------------------------------|
| AT24C32C-PU (Bulk form only)                        | 1.8     | 8P3      | Lead-free/Halogen-free<br>Industrial Temperature<br>(-40°C to 85°C) |
| AT24C32CN-SH-B <sup>(1)</sup> (NiPdAu Lead Finish)  | 1.8     | 8S1      |                                                                     |
| AT24C32CN-SH-T <sup>(2)</sup> (NiPdAu Lead Finish)  | 1.8     | 8S1      |                                                                     |
| AT24C32C-TH-B <sup>(1)</sup> (NiPdAu Lead Finish)   | 1.8     | 8A2      |                                                                     |
| AT24C32C-TH-T <sup>(2)</sup> (NiPdAu Lead Finish)   | 1.8     | 8A2      |                                                                     |
| AT24C32CY6-YH-T <sup>(2)</sup> (NiPdAu Lead Finish) | 1.8     | 8Y6      |                                                                     |
| AT24C32CD3-DH-T <sup>(2)</sup> (NiPdAu Lead Finish) | 1.8     | 8D3      |                                                                     |
| AT24C32CU2-UU-T <sup>(2)</sup>                      | 1.8     | 8U2-1    |                                                                     |
| AT24C32C-W-11 <sup>(3)</sup>                        | 1.8     | Die Sale | Industrial Temperature<br>(-40°C to 85°C)                           |

- Notes:
1. “-B” denotes Bulk.
  2. “-T” denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP and dBG2 = 5K per reel.
  3. Available in waffle pack, tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

| Package Type |                                                                                                        |
|--------------|--------------------------------------------------------------------------------------------------------|
| 8Y6          | 8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Mini-MAP, Dual no Lead Package (DFN), (MLP 2x3) |
| 8P3          | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)                                                |
| 8S1          | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)                                      |
| 8A2          | 8-lead, 4.4 mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)                                |
| 8U2-1        | 8-ball, die Ball Grid Array Package (dBG2)                                                             |
| 8D3          | 8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)                                 |
| Options      |                                                                                                        |
| -1.8         | Low Voltage (1.8V to 5.5V)                                                                             |

## AT24C64C Ordering Information

| Ordering Code                                       | Voltage | Package  | Operation Range                                                     |
|-----------------------------------------------------|---------|----------|---------------------------------------------------------------------|
| AT24C64C-PU (Bulk form only)                        | 1.8     | 8P3      | Lead-free/Halogen-free<br>Industrial Temperature<br>(-40°C to 85°C) |
| AT24C64CN-SH-B <sup>(1)</sup> (NiPdAu Lead Finish)  | 1.8     | 8S1      |                                                                     |
| AT24C64CN-SH-T <sup>(2)</sup> (NiPdAu Lead Finish)  | 1.8     | 8S1      |                                                                     |
| AT24C64C-TH-B <sup>(1)</sup> (NiPdAu Lead Finish)   | 1.8     | 8A2      |                                                                     |
| AT24C64C-TH-T <sup>(2)</sup> (NiPdAu Lead Finish)   | 1.8     | 8A2      |                                                                     |
| AT24C64CY6-YH-T <sup>(2)</sup> (NiPdAu Lead Finish) | 1.8     | 8Y6      |                                                                     |
| AT24C64CD3-DH-T <sup>(2)</sup> (NiPdAu Lead Finish) | 1.8     | 8D3      |                                                                     |
| AT24C64CU2-UU-T <sup>(2)</sup>                      | 1.8     | 8U2-1    |                                                                     |
| AT24C64C-W-11 <sup>(3)</sup>                        | 1.8     | Die Sale | Industrial Temperature<br>(-40°C to 85°C)                           |

- Notes:
1. "-B" denotes Bulk.
  2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP and dBGA2 = 5K per reel.
  3. Available in waffle pack, tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

| Package Type |                                                                                                        |
|--------------|--------------------------------------------------------------------------------------------------------|
| 8Y6          | 8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Mini-MAP, Dual no Lead Package (DFN), (MLP 2x3) |
| 8P3          | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)                                                |
| 8S1          | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)                                      |
| 8A2          | 8-lead, 4.4 mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)                                |
| 8U2-1        | 8-ball, die Ball Grid Array Package (dBGA2)                                                            |
| 8D3          | 8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)                                 |
| Options      |                                                                                                        |
| -1.8         | Low Voltage (1.8V to 5.5V)                                                                             |

## 13. Part Marking Scheme

### 13.1 8-PDIP

| TOP MARK                        | Seal Year<br>  Seal Week | Y = SEAL YEAR                               | WW = SEAL WEEK |
|---------------------------------|--------------------------|---------------------------------------------|----------------|
|                                 |                          | 6: 2006 0: 2010                             | 02 = Week 2    |
|                                 |                          | 7: 2007 1: 2011                             | 04 = Week 4    |
|                                 |                          | 8: 2008 2: 2012                             | :: : :::: :    |
|                                 |                          | 9: 2009 3: 2013                             | :: : :::: ::   |
|                                 |                          |                                             | 50 = Week 50   |
|                                 |                          |                                             | 52 = Week 52   |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
| A T M L U Y W W                 |                          |                                             |                |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
| 3 2 C 1                         |                          |                                             |                |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
| * Lot Number                    |                          | Lot Number to Use ALL Characters in Marking |                |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
|                                 |                          |                                             |                |
| Pin 1 Indicator (Dot)           |                          | <b>BOTTOM MARK</b>                          | No Bottom Mark |

### 13.2 8-SOIC

| TOP MARK                        | Seal Year<br>  Seal Week | Y = SEAL YEAR                               | WW = SEAL WEEK |
|---------------------------------|--------------------------|---------------------------------------------|----------------|
|                                 |                          | 6: 2006 0: 2010                             | 02 = Week 2    |
|                                 |                          | 7: 2007 1: 2011                             | 04 = Week 4    |
|                                 |                          | 8: 2008 2: 2012                             | :: : :::: :    |
|                                 |                          | 9: 2009 3: 2013                             | :: : :::: ::   |
|                                 |                          |                                             | 50 = Week 50   |
|                                 |                          |                                             | 52 = Week 52   |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
| A T M L H Y W W                 |                          |                                             |                |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
| 3 2 C 1                         |                          |                                             |                |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
| * Lot Number                    |                          | Lot Number to Use ALL Characters in Marking |                |
| --- --- --- --- --- --- --- --- |                          |                                             |                |
|                                 |                          | <b>BOTTOM MARK</b>                          | No Bottom Mark |
| Pin 1 Indicator (Dot)           |                          |                                             |                |

## 13.3 8-TSSOP

### TOP MARK

```

Pin 1 Indicator (Dot)
|
|---|---|---|---|
*   H   Y   W   W
|---|---|---|---|
3   2   C       1
|---|---|---|---|

```

Y = SEAL YEAR

|         |         |
|---------|---------|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

WW = SEAL WEEK

|              |
|--------------|
| 02 = Week 2  |
| 04 = Week 4  |
| :: : :::: :  |
| :: : :::: :: |
| 50 = Week 50 |
| 52 = Week 52 |

### BOTTOM MARK

```

|---|---|---|---|---|---|
P   H
|---|---|---|---|---|---|
A   A   A   A   A   A   A
|---|---|---|---|---|---|
<- Pin 1 Indicator

```

## 13.4 8-Ultra Thin Mini MAP

### TOP MARK

```

|---|---|---|
3   2   C
|---|---|---|
H   1
|---|---|---|
Y   X   X
|---|---|---|
*
|
Pin 1 Indicator (Dot)

```

Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH  
NSEB TRACE CODE LOG BOOK.  
(e.g. XX = AA, AB, AC, ...AX, AY, AZ)

Y = SEAL YEAR

|         |         |
|---------|---------|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |



## 13.5 8-ULA

### TOP MARK

```

|---|---|---|
  2   B C
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
Pin 1 Indicator (Dot)

```

Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH  
NSEB TRACE CODE LOG BOOK.  
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = BUILD YEAR

6: 2006

7: 2007

8: 2008

Etc...

## 14. Part Marking Scheme

### 14.1 8-PDIP

#### TOP MARK

Seal Year  
| Seal Week  
| | |  
|---|---|---|---|---|---|---|---|  
A T M L U Y W W  
|---|---|---|---|---|---|---|---|  
6 4 C 1  
|---|---|---|---|---|---|---|---|  
\* Lot Number  
|---|---|---|---|---|---|---|---|  
|  
Pin 1 Indicator (Dot)

#### Y = SEAL YEAR

6: 2006 0: 2010  
7: 2007 1: 2011  
8: 2008 2: 2012  
9: 2009 3: 2013

#### WW = SEAL WEEK

02 = Week 2  
04 = Week 4  
:: : :::: :  
:: : :::: ::  
50 = Week 50  
52 = Week 52

Lot Number to Use ALL Characters in Marking

#### BOTTOM MARK

No Bottom Mark

### 14.2 8-SOIC

#### TOP MARK

Seal Year  
| Seal Week  
| | |  
|---|---|---|---|---|---|---|---|  
A T M L H Y W W  
|---|---|---|---|---|---|---|---|  
6 4 C 1  
|---|---|---|---|---|---|---|---|  
\* Lot Number  
|---|---|---|---|---|---|---|---|  
|  
Pin 1 Indicator (Dot)

#### Y = SEAL YEAR

6: 2006 0: 2010  
7: 2007 1: 2011  
8: 2008 2: 2012  
9: 2009 3: 2013

#### WW = SEAL WEEK

02 = Week 2  
04 = Week 4  
:: : :::: :  
:: : :::: ::  
50 = Week 50  
52 = Week 52

Lot Number to Use ALL Characters in Marking

#### BOTTOM MARK

No Bottom Mark

## 14.3 8-TSSOP

### TOP MARK

```

Pin 1 Indicator (Dot)
|
|---|---|---|---|
*   H   Y   W   W
|---|---|---|---|
6   4   C       1
|---|---|---|---|

```

Y = SEAL YEAR

|         |         |
|---------|---------|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

WW = SEAL WEEK

|              |
|--------------|
| 02 = Week 2  |
| 04 = Week 4  |
| :: : :::: :  |
| :: : :::: :: |
| 50 = Week 50 |
| 52 = Week 52 |

### BOTTOM MARK

```

|---|---|---|---|---|---|
P   H
|---|---|---|---|---|---|
A   A   A   A   A   A   A
|---|---|---|---|---|---|
<- Pin 1 Indicator

```

## 14.4 8-Ultra Thin Mini MAP

### TOP MARK

```

|---|---|---|
6   4   C
|---|---|---|
H   1
|---|---|---|
Y   X   X
|---|---|---|
*
|
Pin 1 Indicator (Dot)

```

Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH  
NSEB TRACE CODE LOG BOOK.  
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = SEAL YEAR

|         |         |
|---------|---------|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

## 14.5 8-ULA

### TOP MARK

```

|---|---|---|
  2   C  C
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
Pin 1 Indicator (Dot)

```

Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH  
NSEB TRACE CODE LOG BOOK.

(e.g. XX = AA, AB, AC, ...AX, AY, AZ)

Y = BUILD YEAR

6: 2006

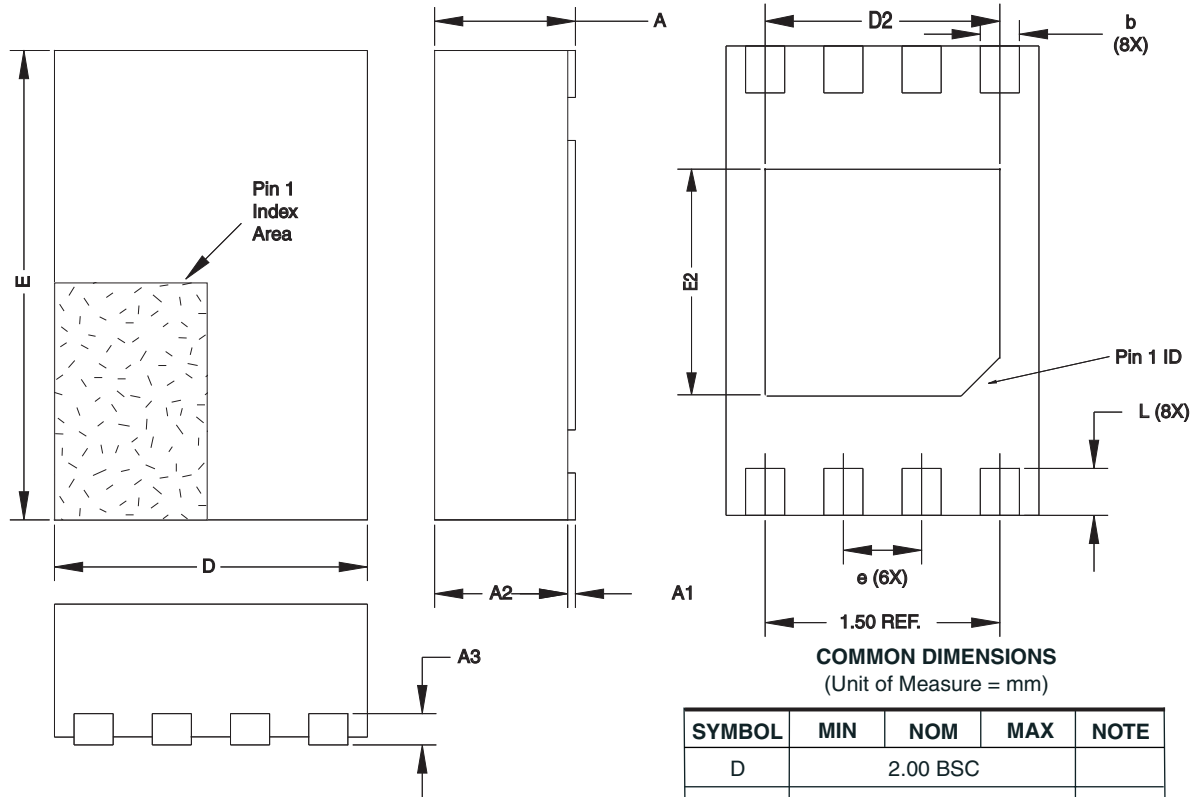
7: 2007

8: 2008

Etc...

## 15. Packaging Information

### 8Y6 - MLP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN  | NOM      | MAX  | NOTE |
|--------|------|----------|------|------|
| D      |      | 2.00 BSC |      |      |
| E      |      | 3.00 BSC |      |      |
| D2     | 1.40 | 1.50     | 1.60 |      |
| E2     | -    | -        | 1.40 |      |
| A      | -    | -        | 0.60 |      |
| A1     | 0.0  | 0.02     | 0.05 |      |
| A2     | -    | -        | 0.55 |      |
| A3     |      | 0.20 REF |      |      |
| L      | 0.20 | 0.30     | 0.40 |      |
| e      |      | 0.50 BSC |      |      |
| b      | 0.20 | 0.25     | 0.30 | 2    |

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
  2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
  3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

10/16/07



2325 Orchard Parkway  
San Jose, CA 95131

#### TITLE

**8Y6**, 8-lead 2.0 x 3.0 mm Body, 0.50 mm Pitch, Ultra Thin Mini-Map,  
Dual No Lead Package (DFN) ,(MLP 2x3)

#### DRAWING NO.

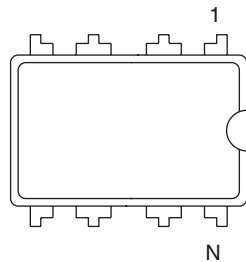
8Y6

#### REV.

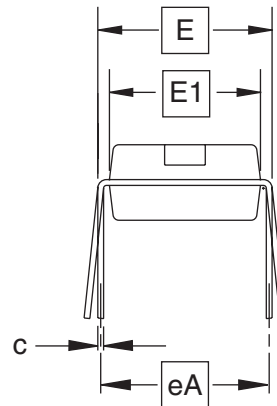
D



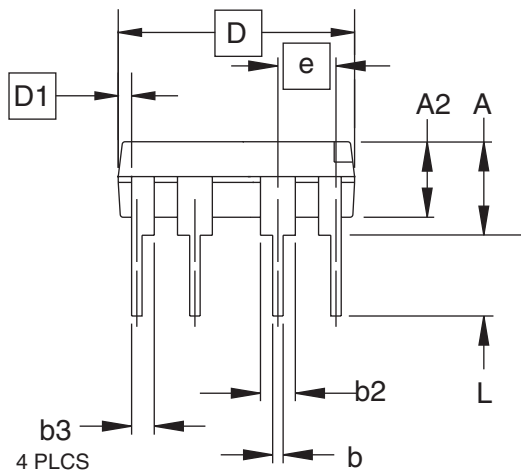
## 8P3 – PDIP



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = inches)

| SYMBOL | MIN       | NOM   | MAX   | NOTE |
|--------|-----------|-------|-------|------|
| A      |           |       | 0.210 | 2    |
| A2     | 0.115     | 0.130 | 0.195 |      |
| b      | 0.014     | 0.018 | 0.022 | 5    |
| b2     | 0.045     | 0.060 | 0.070 | 6    |
| b3     | 0.030     | 0.039 | 0.045 | 6    |
| c      | 0.008     | 0.010 | 0.014 |      |
| D      | 0.355     | 0.365 | 0.400 | 3    |
| D1     | 0.005     |       |       | 3    |
| E      | 0.300     | 0.310 | 0.325 | 4    |
| E1     | 0.240     | 0.250 | 0.280 | 3    |
| e      | 0.100 BSC |       |       |      |
| eA     | 0.300 BSC |       |       | 4    |
| L      | 0.115     | 0.130 | 0.150 | 2    |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
  2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
  3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
  4. E and eA measured with the leads constrained to be perpendicular to datum.
  5. Pointed or rounded lead tips are preferred to ease insertion.
  6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual  
In-line Package (PDIP)

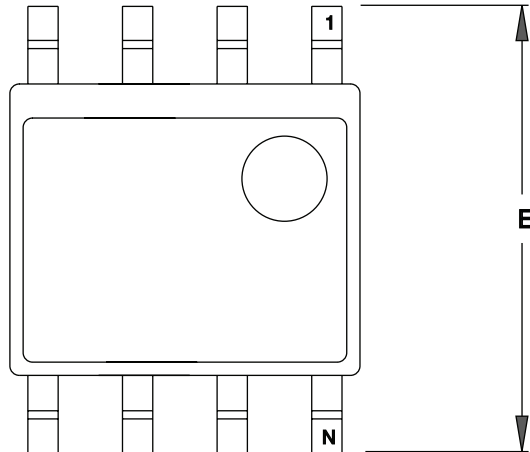
**DRAWING NO.**

8P3

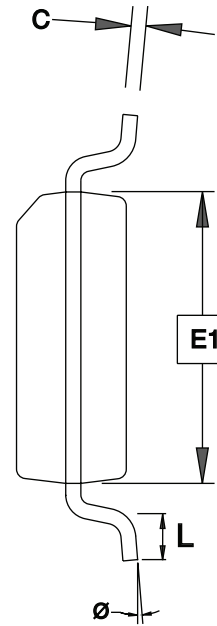
**REV.**

B

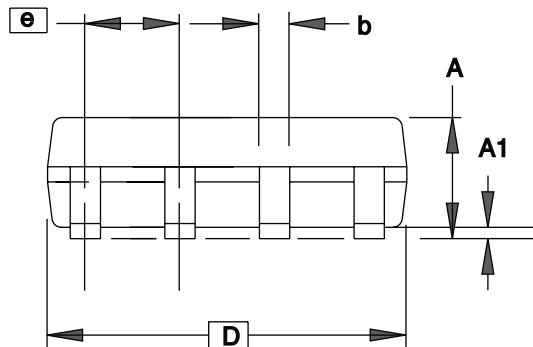
# 8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM | MAX  | NOTE |
|--------|----------|-----|------|------|
| A      | 1.35     | –   | 1.75 |      |
| A1     | 0.10     | –   | 0.25 |      |
| b      | 0.31     | –   | 0.51 |      |
| C      | 0.17     | –   | 0.25 |      |
| D      | 4.80     | –   | 5.05 |      |
| E1     | 3.81     | –   | 3.99 |      |
| E      | 5.79     | –   | 6.20 |      |
| e      | 1.27 BSC |     |      |      |
| L      | 0.40     | –   | 1.27 |      |
| θ      | 0°       | –   | 8°   |      |

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

3/17/05



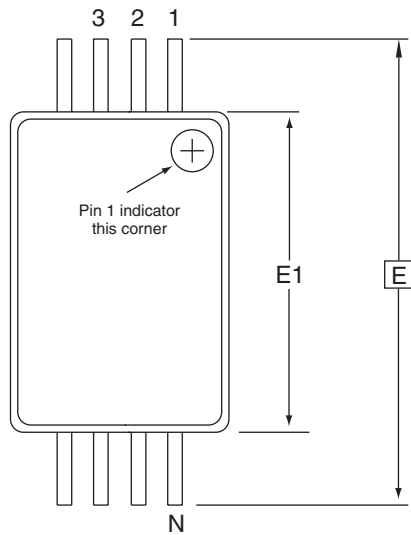
1150 E. Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906

**TITLE**  
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing  
Small Outline (JEDEC SOIC)

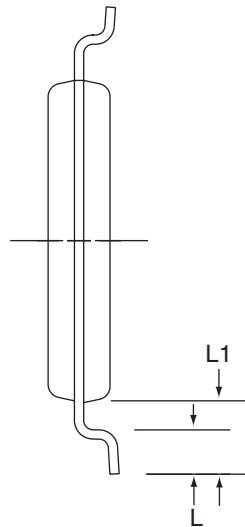
**DRAWING NO.**  
8S1

**REV.**  
C

## 8A2 – TSSOP



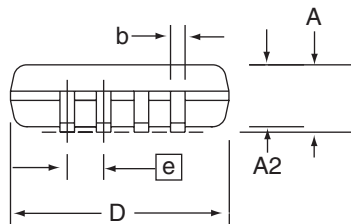
Top View



End View

### COMMON DIMENSIONS (Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE |
|--------|----------|------|------|------|
| D      | 2.90     | 3.00 | 3.10 | 2, 5 |
| E      | 6.40 BSC |      |      |      |
| E1     | 4.30     | 4.40 | 4.50 | 3, 5 |
| A      | –        | –    | 1.20 |      |
| A2     | 0.80     | 1.00 | 1.05 |      |
| b      | 0.19     | –    | 0.30 | 4    |
| e      | 0.65 BSC |      |      |      |
| L      | 0.45     | 0.60 | 0.75 |      |
| L1     | 1.00 REF |      |      |      |



Side View

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02



2325 Orchard Parkway  
San Jose, CA 95131

#### TITLE

**8A2**, 8-lead, 4.4 mm Body, Plastic  
Thin Shrink Small Outline Package (TSSOP)

#### DRAWING NO.

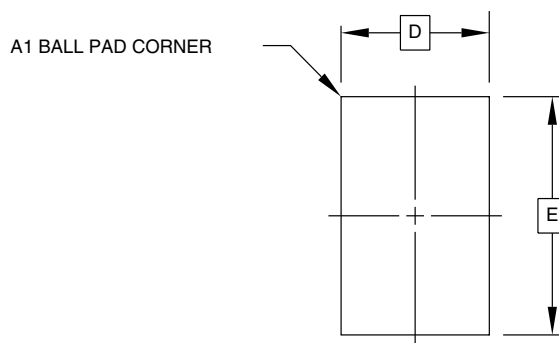
8A2

#### REV.

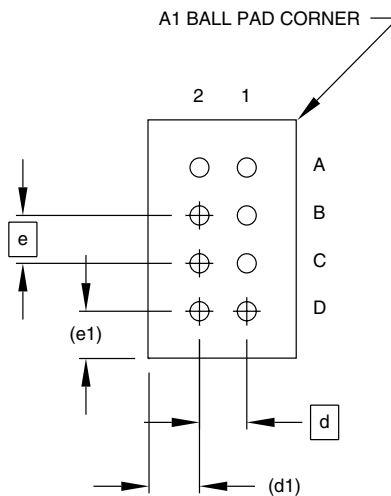
B



## 8U2-1 - dBGA2

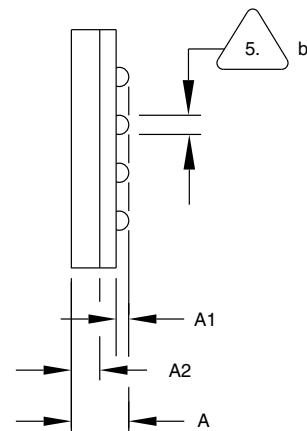


TOP VIEW



BOTTOM VIEW

8 SOLDER BALLS



SIDE VIEW

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE |
|--------|----------|------|------|------|
| A      | 0.81     | 0.91 | 1.00 |      |
| A1     | 0.15     | 0.20 | 0.25 |      |
| A2     | 0.40     | 0.45 | 0.50 |      |
| b      | 0.25     | 0.30 | 0.35 |      |
| D      | 2.35 BSC |      |      |      |
| E      | 3.73 BSC |      |      |      |
| e      | 0.75 BSC |      |      |      |
| e1     | 0.74 REF |      |      |      |
| d      | 0.75 BSC |      |      |      |
| d1     | 0.80 REF |      |      |      |

5. Dimension 'b' is measured at the maximum solder ball diameter.

This drawing is for general information only.

6/17/03



1150 E. Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906

### TITLE

8U2-1, 8-ball, 2.35 x 3.73 mm Body, 0.75 mm pitch,  
Small Die Ball Grid Array Package (dBGA2)

### DRAWING NO.

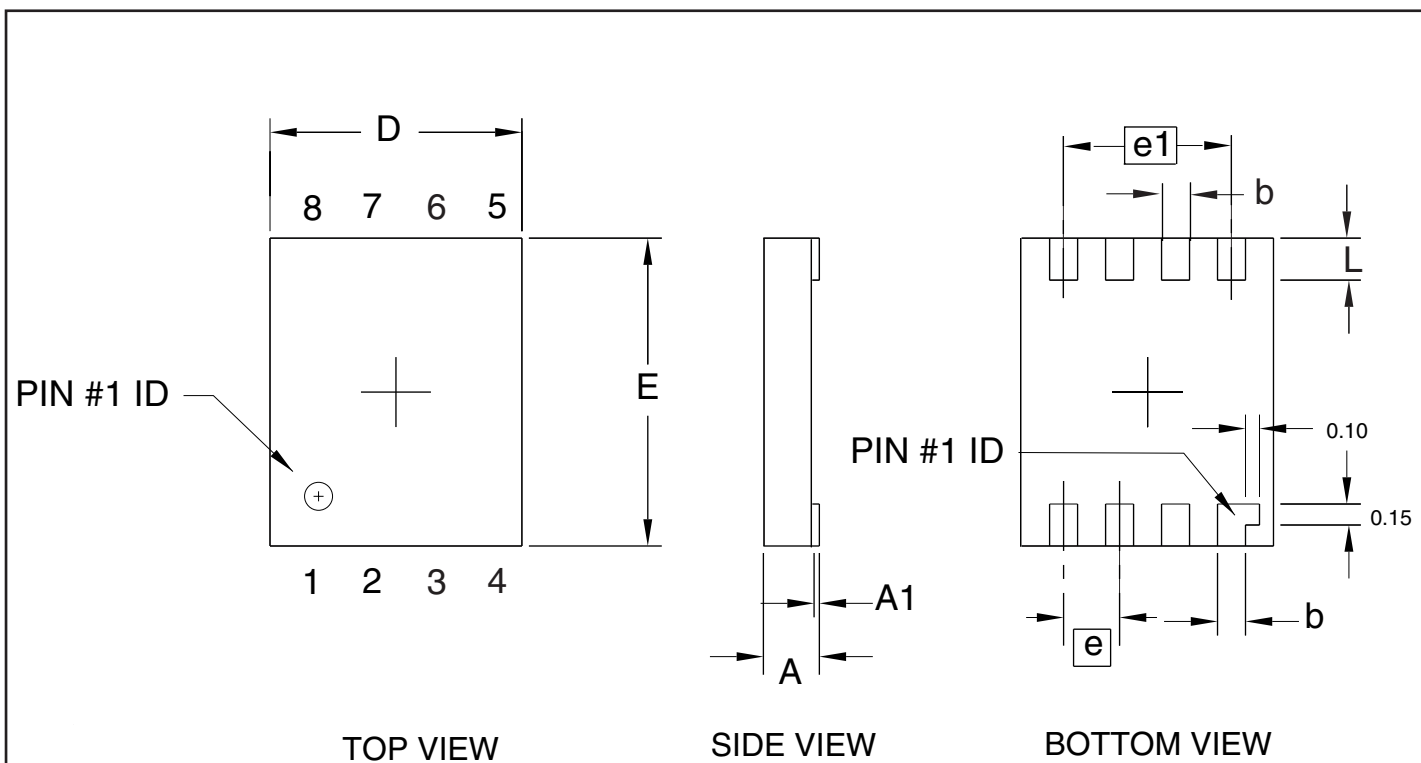
PO8U2-1

### REV.

A



## 8D3 - ULA



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN  | NOM      | MAX  | NOTE |
|--------|------|----------|------|------|
| A      | —    | —        | 0.40 |      |
| A1     | 0.00 | —        | 0.05 |      |
| D      | 1.70 | 1.80     | 1.90 |      |
| E      | 2.10 | 2.20     | 2.30 |      |
| b      | 0.15 | 0.20     | 0.25 |      |
| e      |      | 0.40 TYP |      |      |
| e1     |      | 1.20 REF |      |      |
| L      | 0.25 | 0.30     | 0.35 |      |

11/15/05



1150 E. Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906

### TITLE

**8D3**, 8-lead (1.80 x 2.20 mm Body) Ultra Leadframe  
Land Grid Array (ULLGA) D3

### DRAWING NO.

8D3

### REV.

0

## Revision History

| Doc. Rev. | Date   | Comments                                                                                                                 |
|-----------|--------|--------------------------------------------------------------------------------------------------------------------------|
| 5298A     | 1/2008 | AT24C32C/64C product with date code 2008 work week 14 (814) or later supports 5Vcc operation<br>Initial document release |



## Headquarters

---

**Atmel Corporation**  
2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## International

---

**Atmel Asia**  
Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

**Atmel Europe**  
Le Krebs  
8, Rue Jean-Pierre Timbaud  
BP 309  
78054 Saint-Quentin-en-  
Yvelines Cedex  
France  
Tel: (33) 1-30-60-70-00  
Fax: (33) 1-30-60-71-11

**Atmel Japan**  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Product Contact

---

**Web Site**  
[www.atmel.com](http://www.atmel.com)

**Technical Support**  
[s\\_eeeprom@atmel.com](mailto:s_eeeprom@atmel.com)

**Sales Contact**  
[www.atmel.com/contacts](http://www.atmel.com/contacts)

**Literature Requests**  
[www.atmel.com/literature](http://www.atmel.com/literature)

---

**Disclaimer:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

©2008 Atmel Corporation. **All rights reserved.** Atmel®, logo and combinations thereof, and others, are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.