P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.02 @ V_{GS} = –10 V	–8.0
	0.035 @ V_{GS} = –4.5 V	–6.0

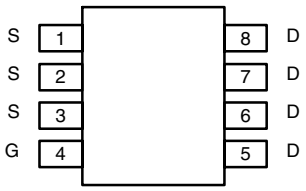
FEATURES

- Lead (Pb)-Free Version is RoHS Compliant

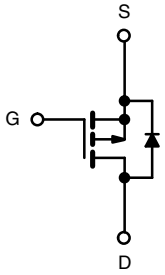
Pb-free Available

RoHS COMPLIANT

SO-8



Top View



P-Channel MOSFET

Ordering Information: Si4435DY-T1–REV A
Si4435DY-T1–A–E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25° UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	–8.0	A
	T_A = 70°C		–6.4	
Pulsed Drain Current		I_{DM}	–50	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

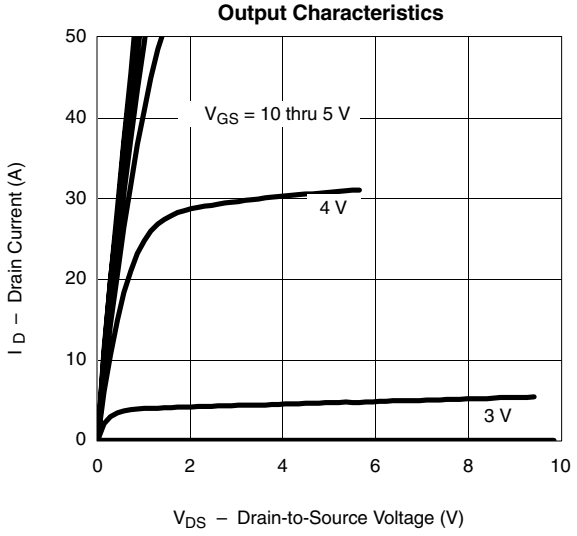
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 μA	–1.0	–2.0	–3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
		V_{DS} = –30 V, V_{GS} = 0 V, T_J = 70°C			–5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ –5 V, V_{GS} = –10 V	–40			A
		V_{DS} ≤ –5 V, V_{GS} = –4.5 V	–10			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –8.0 A		0.015	0.02	Ω
		V_{GS} = –4.5 V, I_D = –5.0 A		0.022	0.035	
Forward Transconductance[b]	g_{fs}	V_{DS} = –15 V, I_D = –8.0 A		20		S
Diode Forward Voltage[b]	V_{SD}	I_S = –2.1 A, V_{GS} = 0 V		–0.75	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = –15 V, V_{GS} = –10 V, I_D = –4.6 A		47	60	nC
Gate-Source Charge	Q_{gs}			9.5		
Gate-Drain Charge	Q_{gd}			8		
Gate Resistance	R_G			2.75	4.1	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –15 V, R_L = 15 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω		16	30	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			75	120	
Fall Time	t_f			31	80	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –2.1 A, di/dt = 100 A/μs		40	80	

Notes
a. Guaranteed by design, not subject to production testing. Values shown are for Product Revision A.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

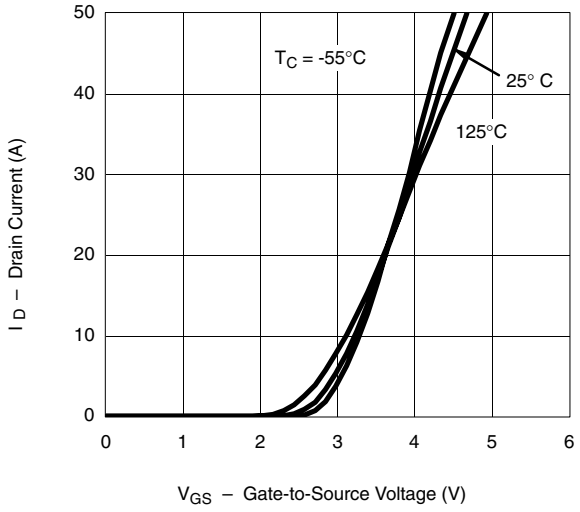
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS, PRODUCT REVISION A (25°C UNLESS NOTED)

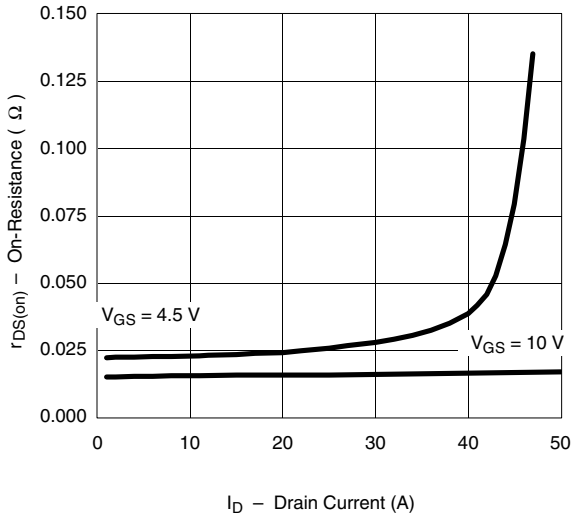
Output Characteristics



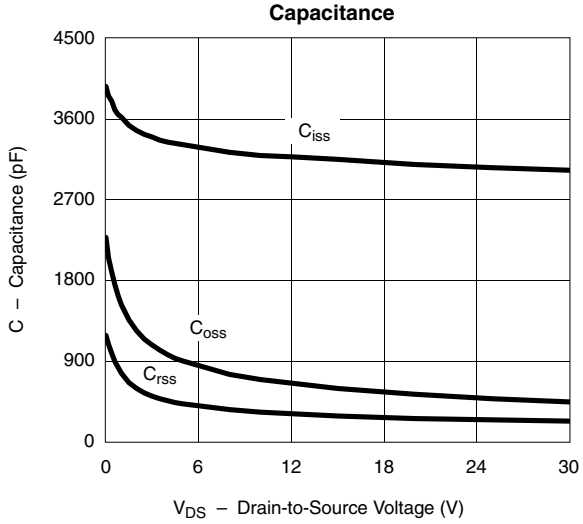
Transfer Characteristics



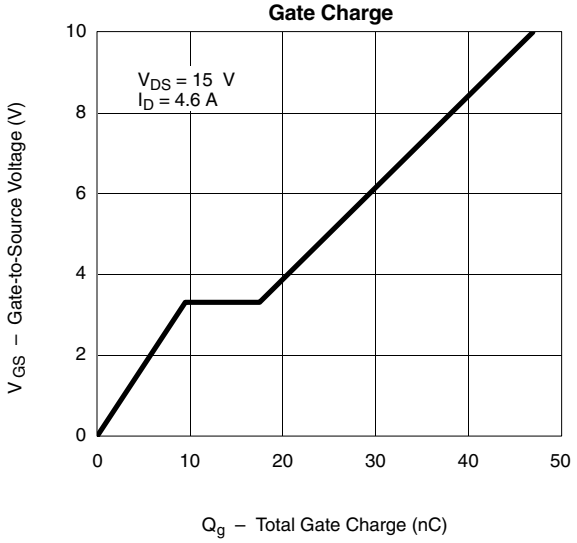
On-Resistance vs. Drain Current



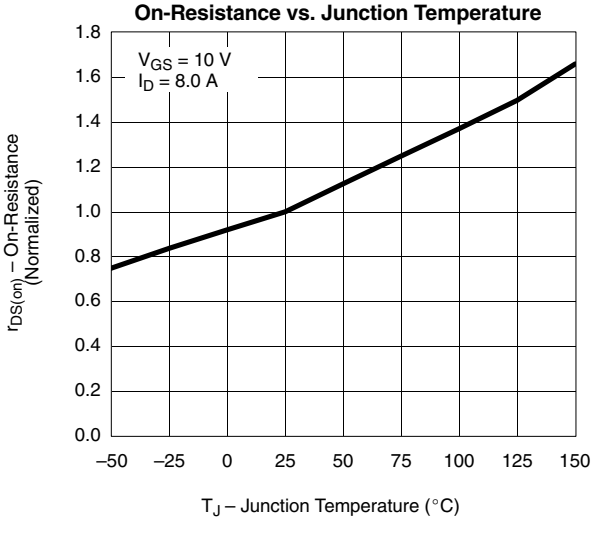
Capacitance



Gate Charge

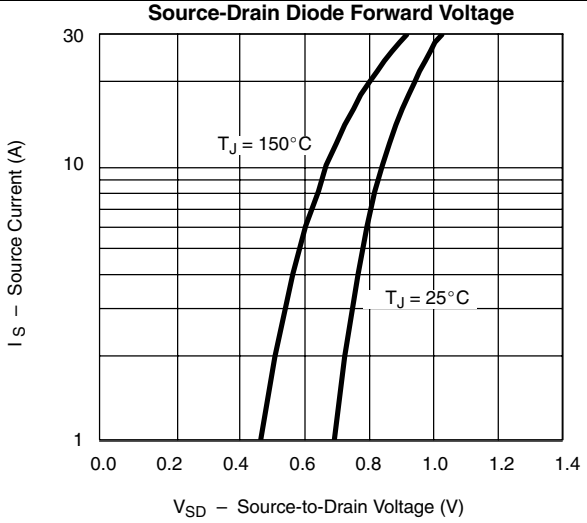


On-Resistance vs. Junction Temperature

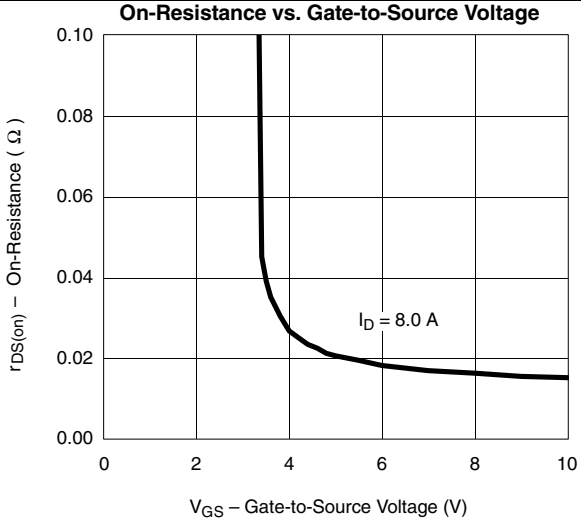


TYPICAL CHARACTERISTICS, PRODUCT REVISION A (25°C UNLESS NOTED)

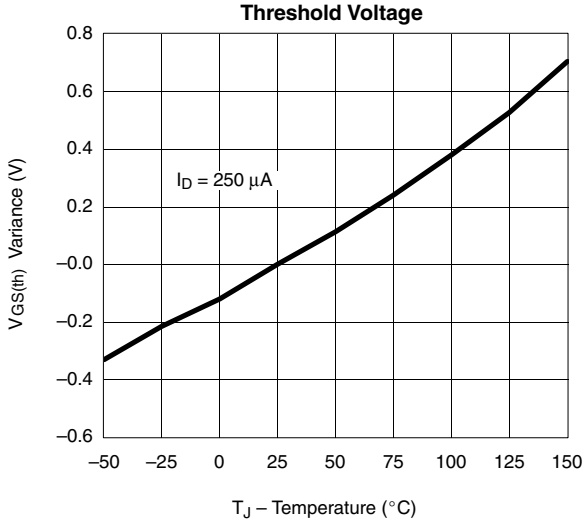
Source-Drain Diode Forward Voltage



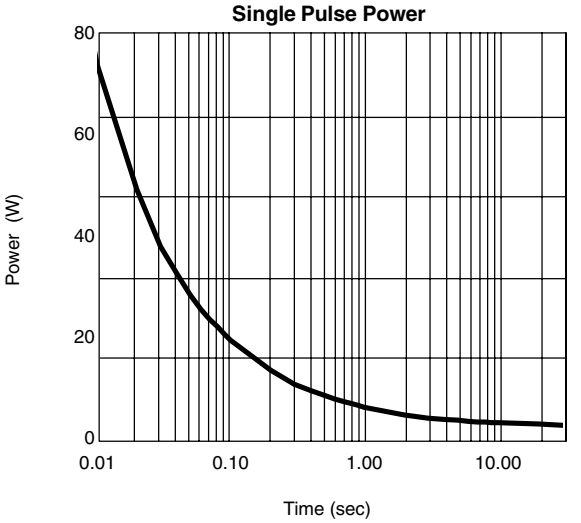
On-Resistance vs. Gate-to-Source Voltage



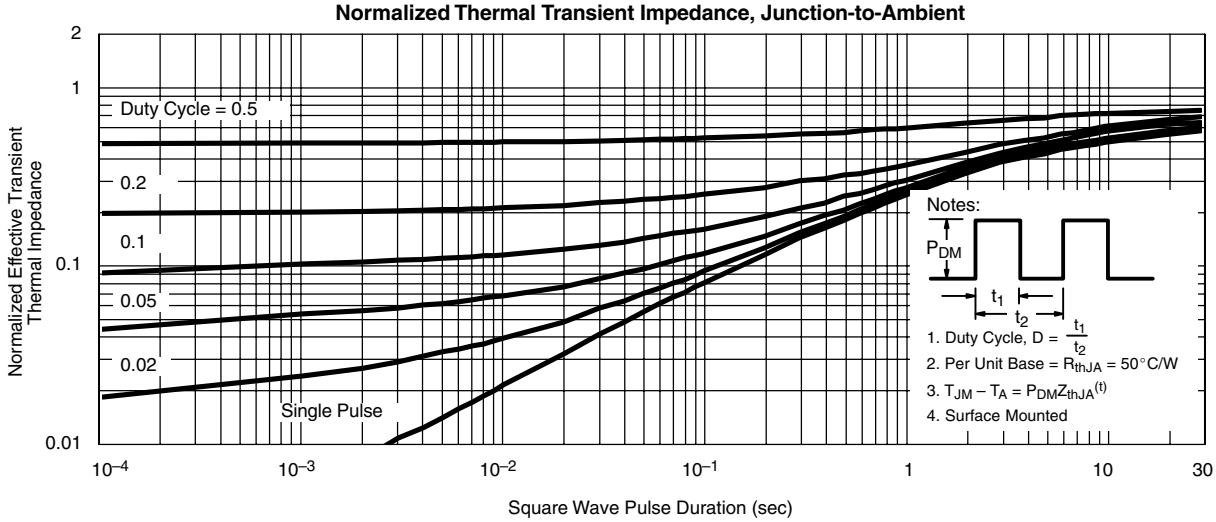
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



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