3500A/1400V
PHASE CONTROL THYRISTOR

Features

Center amplifying gate
Metal case with ceramic insulator
Low on-state and switching losses

Application

Large power converter
DC and AC switches
Active & Passive inverter

$I_{T(AV)}$	3500 A
V_{DRM}/V_{RRM}	1400 V
I_{TSM}	51 KA
I^2T	13005 KA^2S

Symb.		parameter	Test Conditions	$T_{J(℃)}$	Value	Unit
Current Ratings	$I_{T(AV)}$	Average on-state current	180° half sine wave 50Hz Double side cooled Ths=75°C	125	3500	A
	$I_{T(AV)}$	Average on-state current	180° half sine wave 50Hz Double side cooled Ths=55°C	125	3790	A
	I_{TSM}	Surge on-state current	10ms half sine wave VR=0.6VRRM	125	51	KA
	I^2t	I^2T for fusing coordination		125	13005	KA^2S
Characteristics	V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM} & V_{RRM} tp=10ms V_{DSM} & V_{RSM}= V_{DRM}&V_{RRM}+100V	125	1400	V
	I_{DRM} I_{RRM}	Repetitive peak current	V_{DM}= V_{DRM} V_{RM}= V_{RRM}	125	Max.200	mA
	V_{TO}	Threshold voltage		125	Max.0.84	V
	V_{TM}	Threshold voltage	I_{TM}=5000A, F=40KN	25	Max.1.8	V
	r_T	On-state slop resistance		125	Max.0.09	mΩ
	I_H	Holding current	V_A=12V, I_A=1A	25	20-300	mA
Dynamic Parameters	dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%VDRM	125	Max.1000	V/μs
	di/dt	Critical rate of rise of on-state current	VDM= 67%VDRM to 6000A, Gate pulse tr ≤0.5μs IGM=1.5A	125	Max.250	A/μs
	Q_{rr}	Reverse Recovery charge	I_{TM}=2000A,tp=2000μs,V_R=50 V di/dt=-20A/μs	125	2500	μc
Gate Parameters	I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	40-300	mA
	V_{GT}	Gate trigger voltage		25	0.8-3.0	V
	V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	Min.0.3	V

Thermal &Mechanical Date

Symb.	parameter	Test Conditions	$T_{J(℃)}$	Value	Unit
$R_{th(j-c)}$	Thermal resistance Junction to case	At 180^0 sine wave, double side cooled Clamping force 40KN		Max.0.01	℃/W
F_m	Mounting force			35-47	KN
T_{stg}	Stored temperature			-40-140	℃
W_t	Weight			1100	g

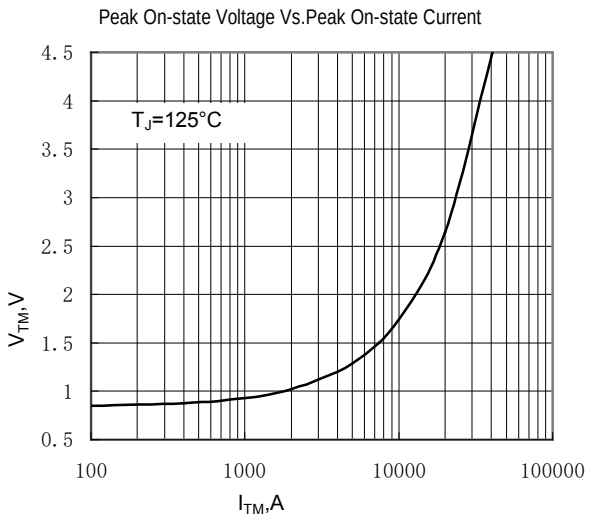

Fig.1

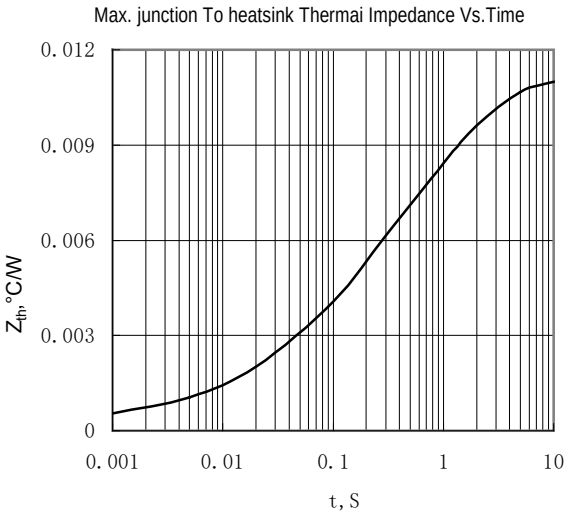

Fig.2

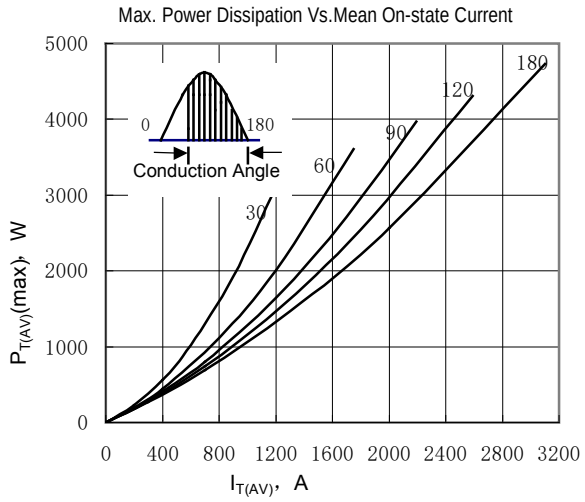

Fig.3

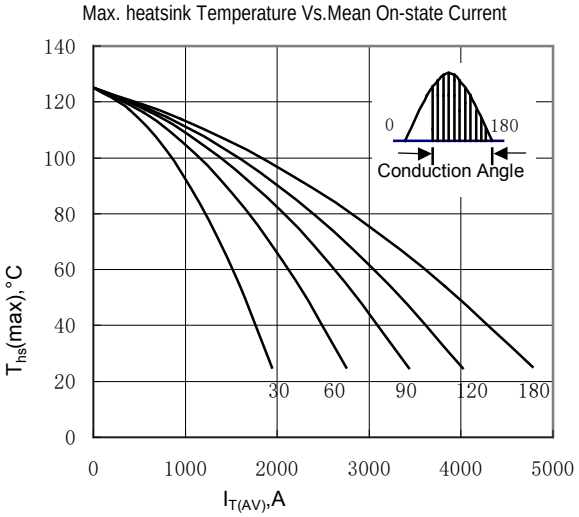

Fig.4

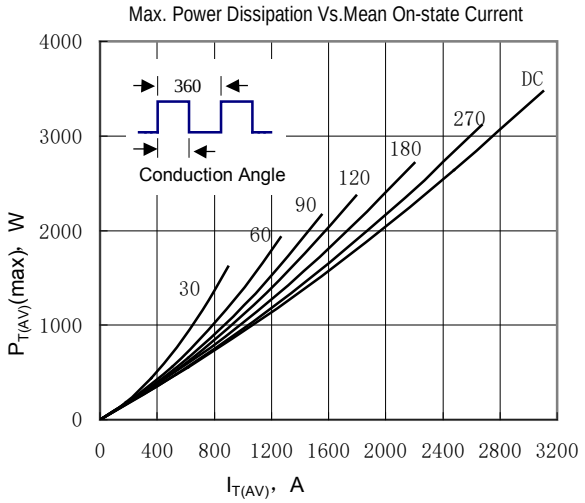

Fig.5

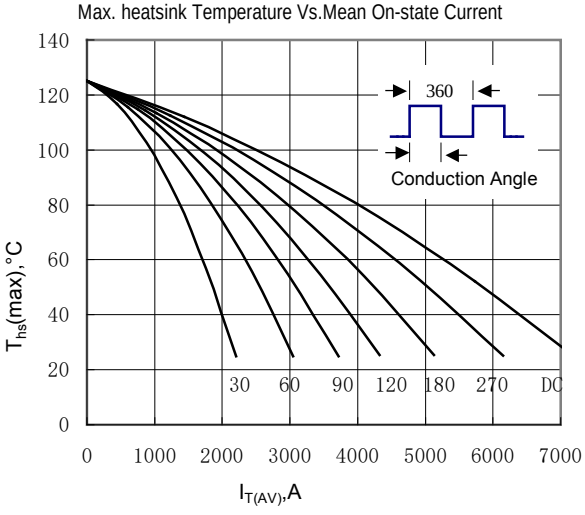

Fig.6

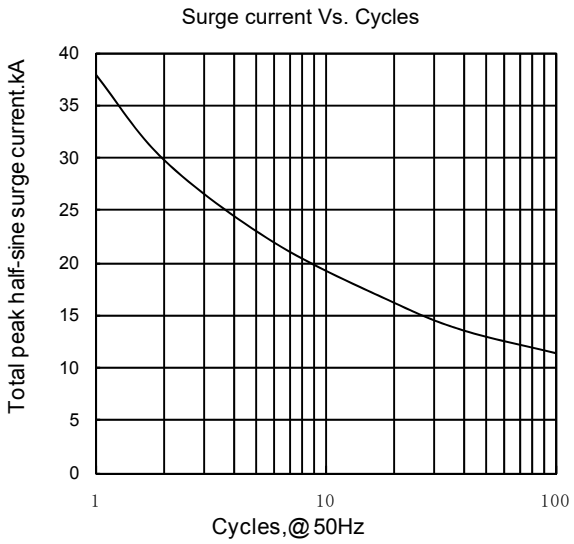

Fig7

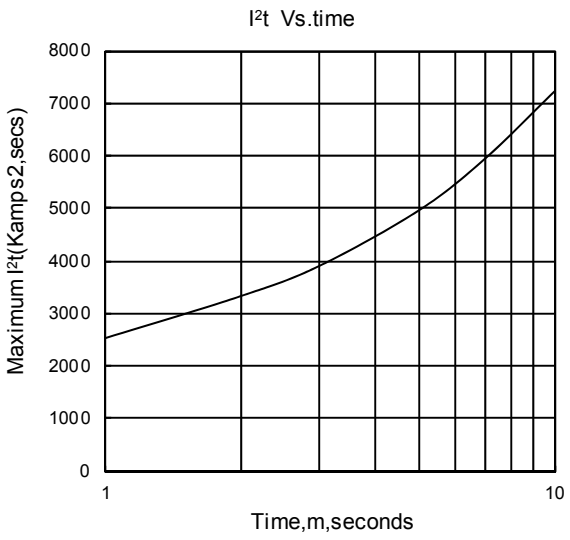

Fig8

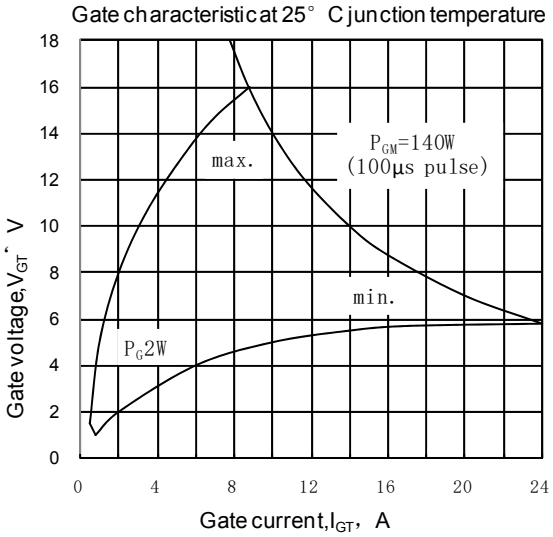

Fig9

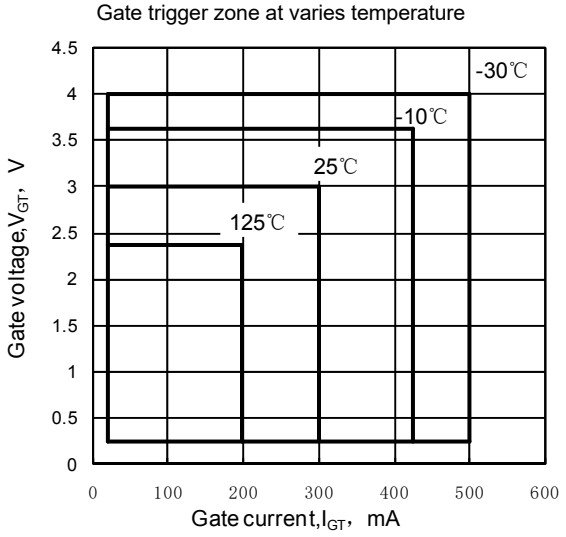

Fig10

Outline: