

HEF4020B

14-stage binary counter

Rev. 04 — 4 December 2008

Product data sheet

1. General description

The HEF4020B is a 14-stage binary counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0, and Q3 to Q13). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. A feature of the device is its high speed (typ. 35 MHz at $V_{DD} = 15$ V).

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input. It is also suitable for use over the full industrial (-40 °C to $+85$ °C) temperature range.

2. Features

- High speed operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range -40 °C to $+85$ °C
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Applications

- Industrial

4. Ordering information

Table 1. Ordering information

All types operate from -40 °C to $+85$ °C.

Type number	Package		
	Name	Description	Version
HEF4020BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4020BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

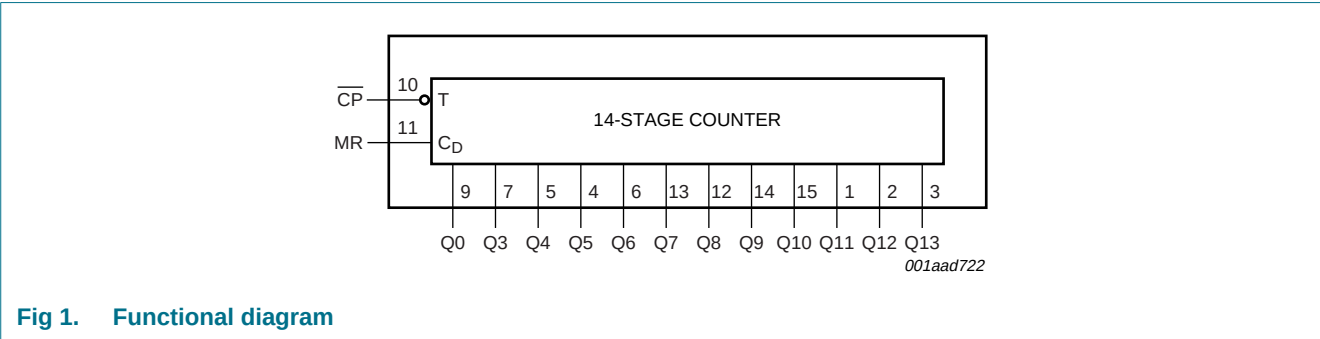


Fig 1. Functional diagram

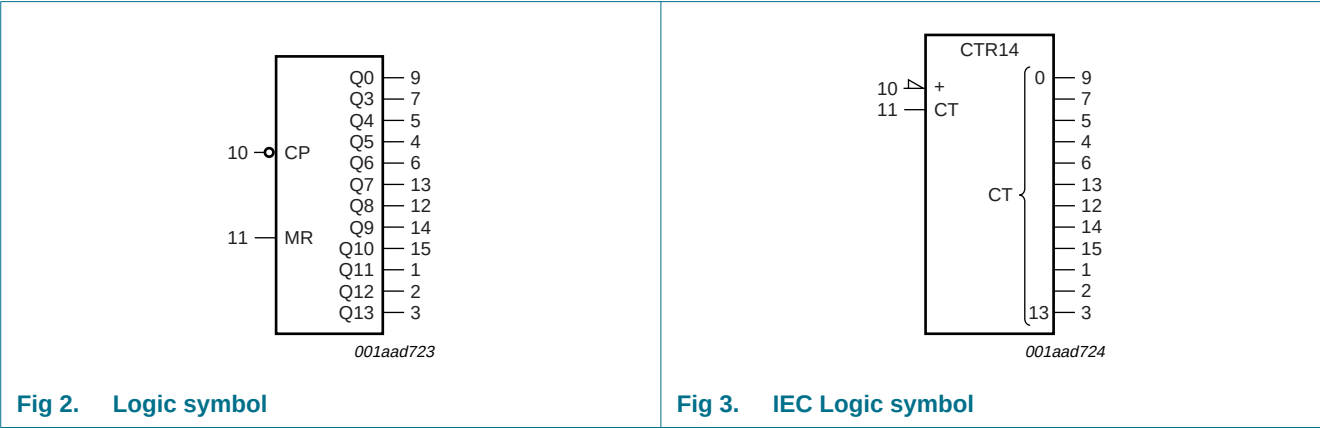


Fig 2. Logic symbol

Fig 3. IEC Logic symbol

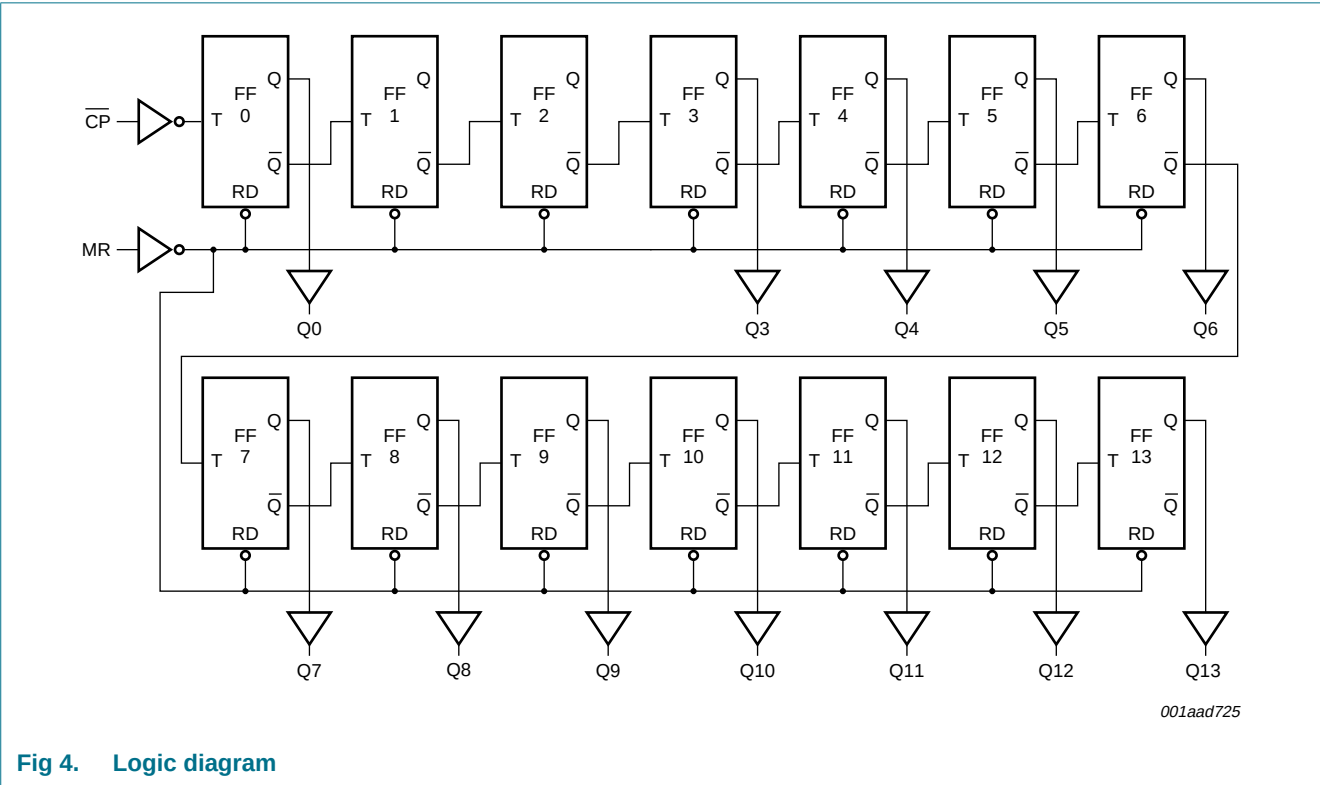


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

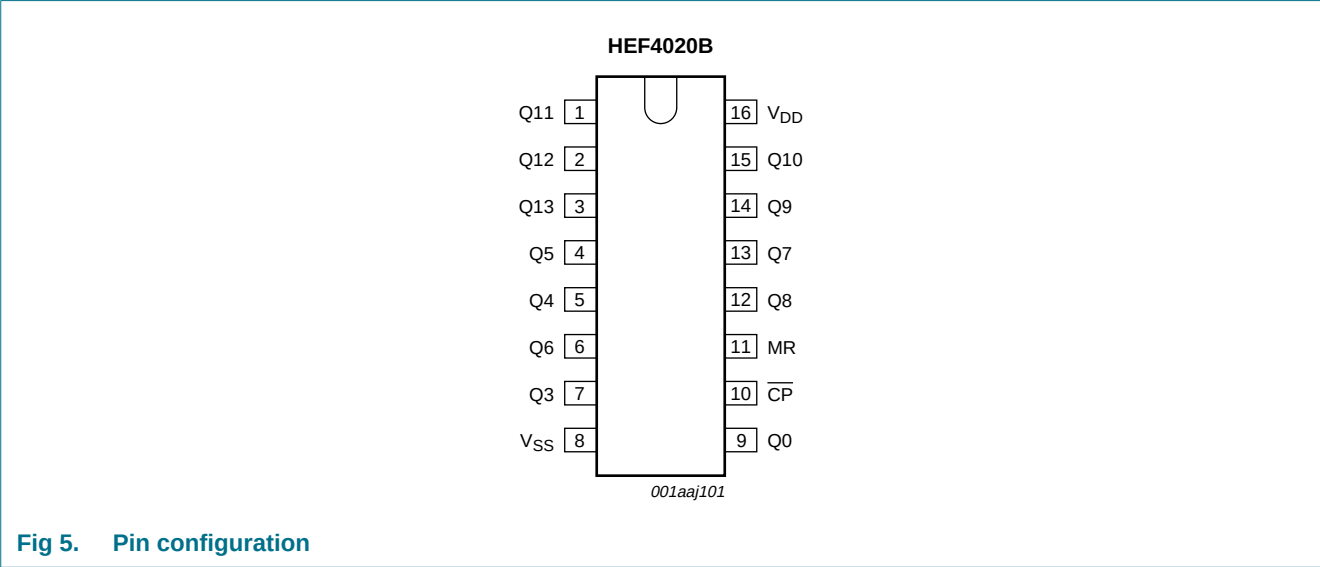


Fig 5. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q3 to Q13	7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	parallel output (Q3 to Q13)
V _{SS}	8	ground supply voltage
Q0	9	parallel output
CP	10	clock input (HIGH-to-LOW edge triggered)
MR	11	master reset input (active HIGH)
V _{DD}	16	supply voltage

7. Functional description

Table 3. Functional table^[1]

Input		Output
CP	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

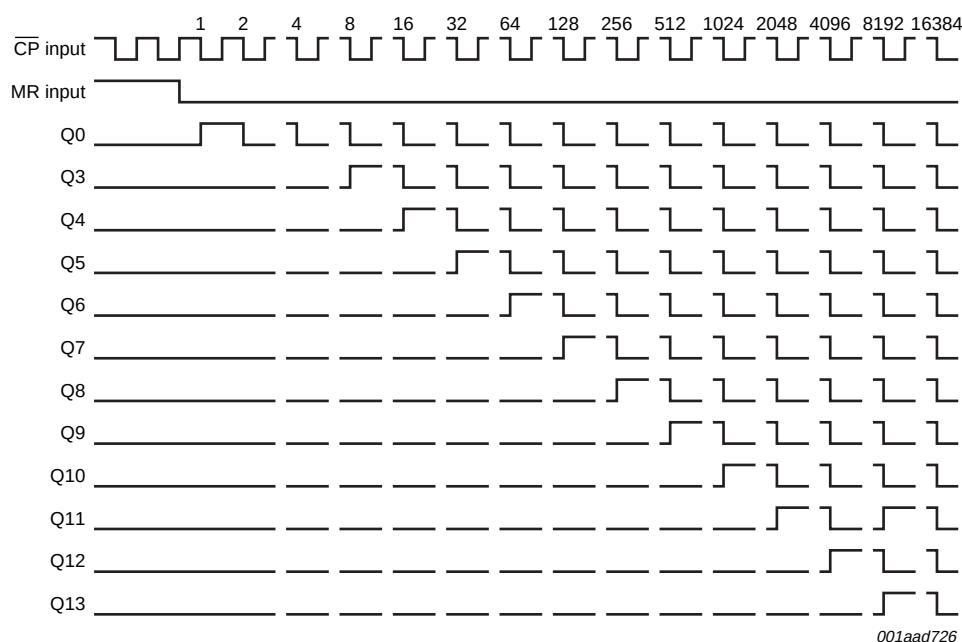


Fig 6. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < 0.5 \text{ V}$ or $V_I > V_{DD} + 0.5 \text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < 0.5 \text{ V}$ or $V_O > V_{DD} + 0.5 \text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} -40 \text{ °C to } +85 \text{ °C}$			
		DIP16 package	[1] -	750	mW
		SO16 package	[2] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	ns/V
		$V_{DD} = 10\text{ V}$	-	-	0.5	ns/V
		$V_{DD} = 15\text{ V}$	-	-	0.08	ns/V

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		$V_O = 4.6\text{ V}$	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		$V_O = 9.5\text{ V}$	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		$V_O = 13.5\text{ V}$	15 V	-3.6	-	-3.0	-	-2.4	-	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 8](#).

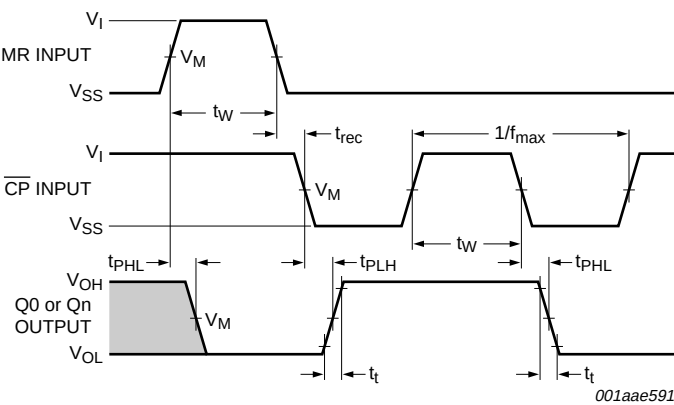
Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP to Q0; see Figure 7	5 V	$78\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	105	210	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	45	90	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	30	65	ns
		Qn to Qn + 1	5 V	$53\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	80	160	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	30	60	ns
			15 V	$12\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	20	40	ns
		MR to Qn; see Figure 7	5 V	$153\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	180	360	ns
			10 V	$79\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	90	180	ns
			15 V	$62\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	70	140	ns
t_{PLH}	LOW to HIGH propagation delay	CP to Q0; see Figure 7	5 V	$78\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	105	210	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	50	95	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	35	70	ns
		Qn to Qn + 1	5 V	$43\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	70	140	ns
			10 V	$14\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	25	50	ns
			15 V	$12\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	20	40	ns
t_t	transition time	see Figure 7	5 V	$10\text{ ns} + (1.00\text{ ns/pF}) C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF}) C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF}) C_L$	-	20	40	ns
t_w	pulse width	CP = HIGH; minimum width; see Figure 7	5 V		50	25	-	ns
			10 V		25	15	-	ns
			15 V		20	10	-	ns
		MR = HIGH; minimum width; see Figure 7	5 V		130	65	-	ns
			10 V		95	50	-	ns
			15 V		90	45	-	ns
t_{rec}	recovery time	MR input; see Figure 7	5 V		115	60	-	ns
			10 V		65	35	-	ns
			15 V		55	25	-	ns
f_{max}	maximum frequency	see Figure 7	5 V		5	10	-	MHz
			10 V		13	25	-	MHz
			15 V		18	35	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D
 P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 2800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 8200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.

12. Waveforms

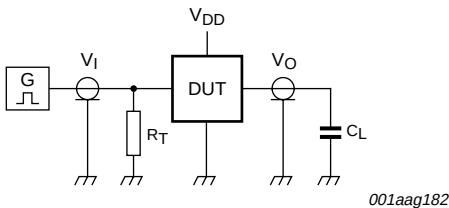


Measurement points are given in [Table 9](#).

Fig 7. Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).
 Definitions for test circuit:
 DUT = Device Under Test.
 C_L = load capacitance including jig and probe capacitance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 8. Test circuit

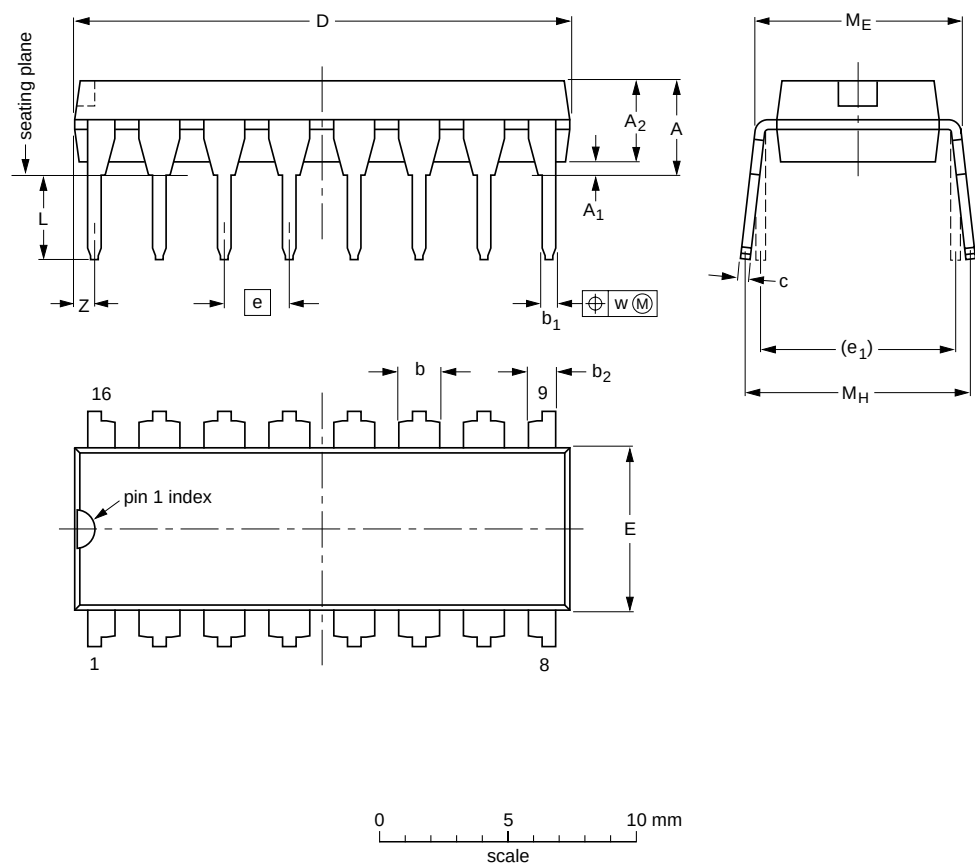
Table 10. Test data

Supply voltage	Input		Load
V _{DD}	V _I	t _r , t _f	C _L
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

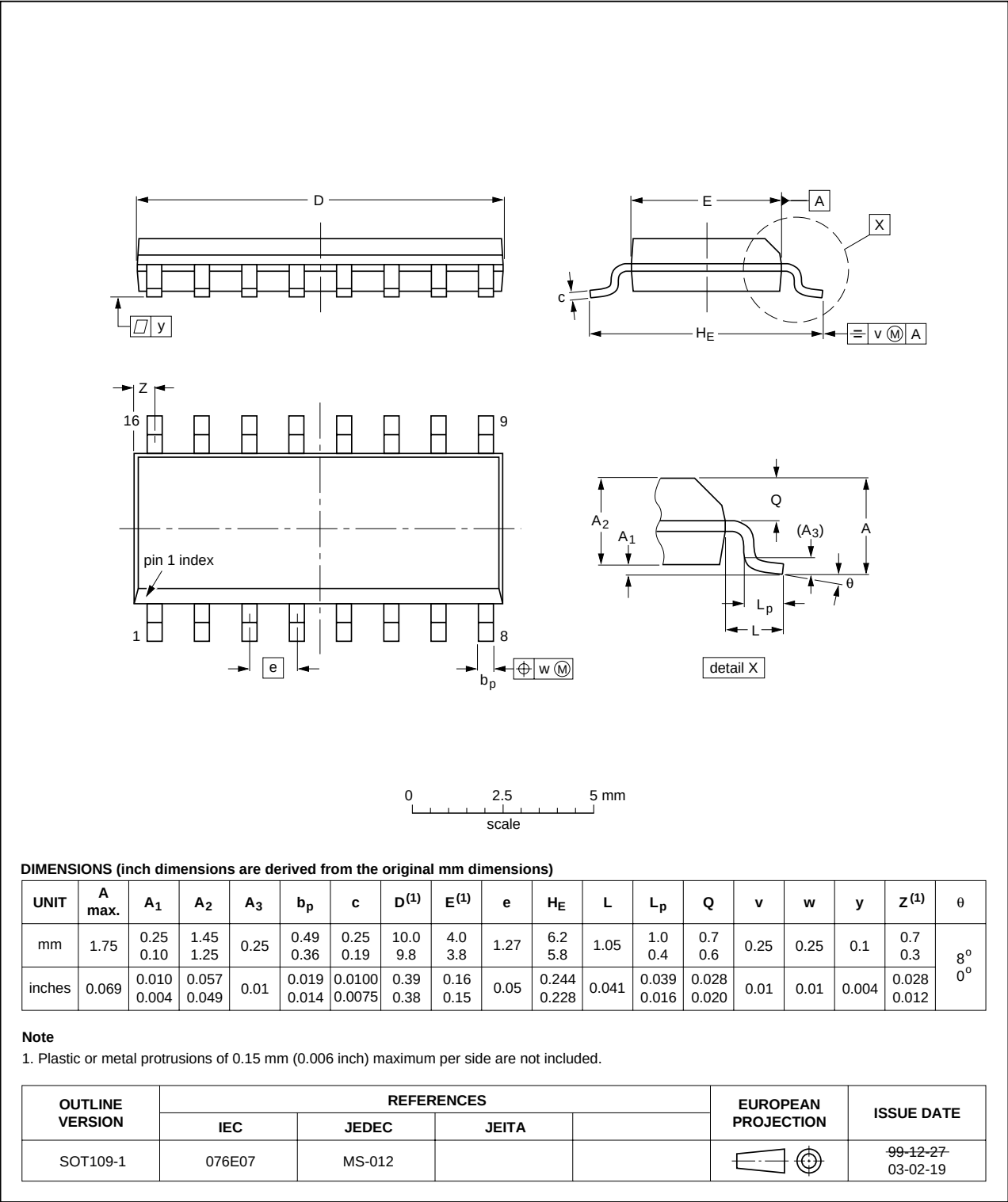


Fig 10. Package outline SOT109-1 (SO16)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4020B_4	20081204	Product data sheet	-	HEF4020B_CNV_3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Parallel output pins renamed Q0 to Q13 throughout. - Temperature statement added to Section 1 "General description". Section 2 "Features" added. Table 1 "Ordering information" restructured. - Package version SOT38-1 changed to SOT38-4 in Section 4, and Figure 9. Package SOT74 removed from Section 4. Figure 1 "Functional diagram", Figure 4 "Logic diagram", Figure 5 "Pin configuration", Figure 7 "Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency" and Figure 6 "Timing diagram" changed for pin name changes. Figure 2 "Logic symbol" and Figure 3 "IEC Logic symbol" added. Table 2 "Pin description" edited for pin name changes. Section 7 "Functional description" added. Section 8 "Limiting values" and Section 10 "Static characteristics" added, taken from the HE4000B Family Specifications data sheet. t_{RMR}, t_{WCPH} and t_{WMRH} changed to t_{rec} and t_W for Table 7 "Dynamic characteristics" and Figure 7 "Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency". 50 % replaced by V_M for Figure 7 "Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency". Table 9 "Measurement points", Figure 8 "Test circuit" and Table 10 "Test data" added.			
HEF4020B_CNV_3	19950101	Product specification	-	HEF4020B_CNV_2
HEF4020B_CNV_2	19950101	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1 General description 1

2 Features 1

3 Applications 1

4 Ordering information 1

5 Functional diagram 2

6 Pinning information 3

6.1 Pinning 3

6.2 Pin description 3

7 Functional description 3

8 Limiting values 4

9 Recommended operating conditions 5

10 Static characteristics 5

11 Dynamic characteristics 6

12 Waveforms 7

13 Package outline 9

14 Abbreviations 11

15 Revision history 11

16 Legal information 12

16.1 Data sheet status 12

16.2 Definitions 12

16.3 Disclaimers 12

16.4 Trademarks 12

17 Contact information 12

18 Contents 13



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.