



N-Channel 30 V (D-S) MOSFET

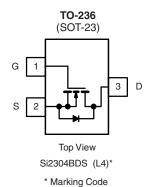
PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
30	0.070 at V _{GS} = 10 V	3.2	2.6			
	0.105 at V _{GS} = 4.5 V	2.6	2.0			

FEATURES

- Halogen-free According to IEC 61249-2-21
- TrenchFET® Power MOSFET
- 100 % R_q Tested
- Compliant to RoHS Directive 2002/95/EC



HALOGEN FREE



Ordering Information: Si2304BDS-T1-E3 (Lead (Pb)-free)

Si2304BDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter	Symbol	5 s	Steady State	Unit		
Drain-Source Voltage	V _{DS}	30		V		
Gate-Source Voltage	V _{GS}	± 20				
Continuous Drain Current /T 150 °C\a.b	T _A = 25 °C	I _D	3.2	2.6		
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 70 °C		2.5	2.1	_	
Pulsed Drain Current	I _{DM}	10		Α		
Continuous Source Current (Diode Conduction) ^{a, b}	I _S	0.9	0.62			
Mariana Barra Birata at and h	T _A = 25 °C	P _D	1.08	0.75	W	
Maximum Power Dissipation ^{a, b}	T _A = 70 °C	T D	0.69	0.48] **	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maniana baratian ta Ambianta	t ≤ 5 s	- R _{thJA}	90	115	°C/W	
Maximum Junction-to-Ambient ^a	Steady State		130	166		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	60	75		

Notes:

- a. Surface mounted on FR4 board, $t \le 5 \text{ s.}$
- b. Pulse width limited by maximum junction temperature.
- c. Surface mounted on FR4 board.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

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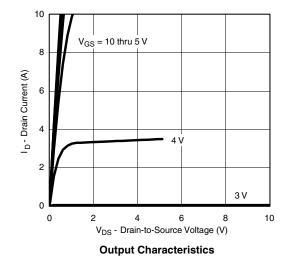


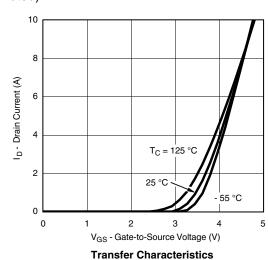
SPECIFICATIONS (T _A = 25 °C, unless otherwise noted)							
			Limits				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.5		3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V _{DS} = 30 V, V _{GS} = 0 V			0.5		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
		$V_{DS} = 30 \text{ V}, V_{GS} = 1 \text{ V}, T_{J} = 25 ^{\circ}\text{C}$			1		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 4.5 \text{ V}, V_{GS} = 10 \text{ V}$	6			Α	
		$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		0.055	0.070		
Drain-Source On-Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$		0.080	0.105	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 4.5 \text{ V}, I_{D} = 2.5 \text{ A}$		6		S	
Diode Forward Voltage	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V		0.8	1.2	V	
Dynamic							
Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 2.5 \text{ A}$		2.6	4		
Total Gate Charge	Q _{gt}			4.6	7	~ C	
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 2.5 \text{ A}$		0.8		nC	
Gate-Drain Charge	Q_{gd}			1.15			
Gate Resistance	R _g	f = 1 MHz	0.6	3	6	Ω	
Input Capacitance	C _{iss}			225			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		50		pF	
Reverse Transfer Capacitance	C _{rss}			28			
Switching							
Turn-On Delay Time	t _{d(on)}			7.5	12		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		12.5	20	no	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		19	30	ns	
Fall Time	t _f			15	25		

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

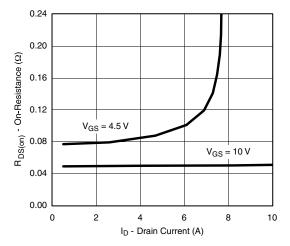




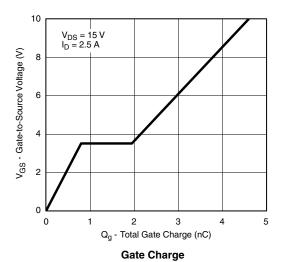
a. Pulse test: PW \leq 300 μ s, duty cycle \leq 2 %.



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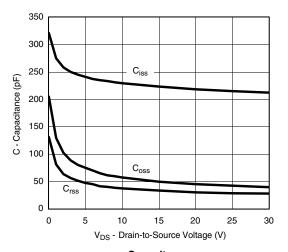


On-Resistance vs. Drain Current

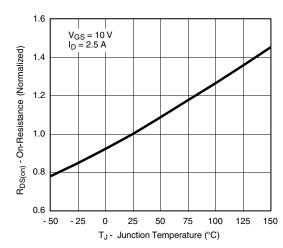


10 T_J = 150 °C Is - Source Current (A) T_J = 25 °C 0.1 0.01 0.001 0.8 0.0 1.2 V_{SD} - Source-to-Drain Voltage (V)

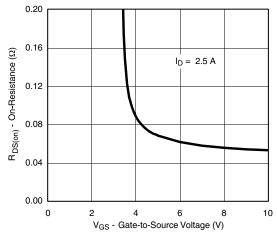
Source-Drain Diode Forward Voltage



Capacitance



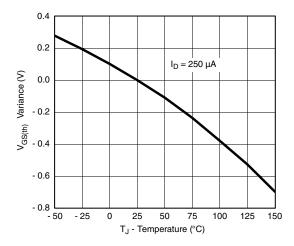
On-Resistance vs. Junction Temperature

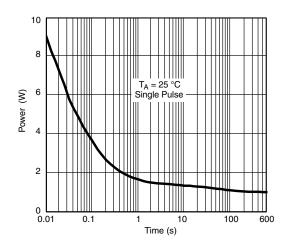


On-Resistance vs. Gate-to-Source Voltage

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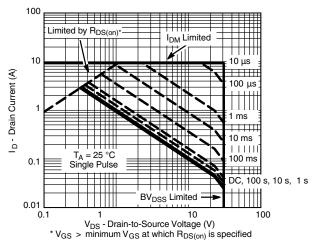
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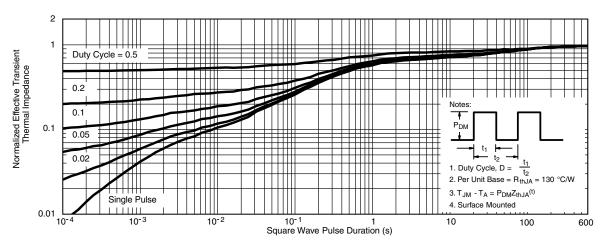


Threshold Voltage

Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72503

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SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES			
	Min	Max	Min	Max		
Α	0.89	1.12	0.035	0.044		
A ₁	0.01	0.10	0.0004	0.004		
A ₂	0.88	1.02	0.0346	0.040		
b	0.35	0.50	0.014	0.020		
С	0.085	0.18	0.003	0.007		
D	2.80	3.04	0.110	0.120		
E	2.10	2.64	0.083	0.104		
E ₁	1.20	1.40	0.047	0.055		
е	0.95 BSC		0.0374 Ref			
e ₁	1.90 BSC		0.074	0.0748 Ref		
L	0.40	0.60	0.016	0.024		
L ₁	0.64 Ref		0.025			
S	0.50 Ref		0.020) Ref		
q	3°	8°	3°	8°		
FCN: S-03946-Rev K 09-	lul-01	•				

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

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RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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