TEST REPORT
IEEE 1547
IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems

Report Number..... :	240801086GZU-001
Date of issue ..... :	03 Sep., 2024
Total number of pages	46 pages
Name of Testing Laboratory preparing the Report .....:	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch Room101/301/401/102/202/302/402/502/602/702/802, No. 7-2, Caipin Road, Huangpu District, Guangzhou, Guangdong, China
Applicant's name.....:	Huawei Technologies Co., Ltd.
Address .....:	Administration Building, Headquarters of Huawei Technologies Co., Ltd., Bantian, Longgang District, Shenzhen, 518129, P.R.C
Test specification:	
Standard ..... :	IEEE 1547: 2003, IEEE 1547a:2014 & IEEE 1547.1: 2005+ A1: 2015
Test procedure..... :	Type approval
Condition of the item tested :	Prototype
Non-standard test method……..:	N/A
Test Report Form No.....:	IEEE1547_a
Test Report Form(s) Originator.....:	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch
Master TRF .....:	Dated 2021-04

General disclaimer:

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The authenticity of this Test Report and its contents can be verified by contacting the NCB, responsible for this Test Report.

Test item description..... : Solar Inverter

Trade Mark..... : HUAWEI

Manufacturer ..... : Same as applicant

Model/Type reference..... : SUN2000-50K-MGL0, SUN2000-50K-MGL0-BR, SUN2000-75K-MGL0-BR, SUN2000-80K-MGL0

Ratings..... :

Model	SUN2000-50K-MGL0	SUN2000-50K-MGL0-BR
Max. Input voltage	750Vdc	
MPPT voltage range	160 ~ 750Vdc	
Max. input current	48Adc*7	
Max. Isc	66Adc*7	
Rated output power	50kW	50kW
Max. Output Apparent power	55kVA	55kVA
Nominal output voltage	3/N/PE 127/220 Vac	
Nominal output current	131.3Aac	131.3Aac
Max. output current	144.4Aac	144.4Aac
Nominal output frequency	60Hz	
Power factor range	0.8(Leading) ~ 0.8(Lagging)	
Ingress protection	IP66	
Operation ambient temperature	-25℃ to +60℃	
Software version	SUN2000MG_V600R023C10	
Model	SUN2000-75K-MGL0-BR	SUN2000-80K-MGL0
Max. Input voltage	750Vdc	
MPPT voltage range	160 ~ 750Vdc	
Max. input current	48Adc*7	
Max. Isc	66Adc*7	
Rated output power	75kW	80kW
Max. Output Apparent power	75kVA	88kVA
Nominal output voltage	3/N/PE 127/220Vac	

Nominal output current	196.9Aac	210.0Aac
Max. output current	196.9Aac	231.0Aac
Nominal output frequency	60Hz	
Power factor range	0.8(Leading) ~ 0.8(Lagging)	
Ingress protection	IP66	
Operation ambient temperature	-25℃ to +60℃	
Software version	SUN2000MG_V600R023C10	

Responsible Testing Laboratory (as applicable), testing procedure and testing location(s):			
☒	**Testing Laboratory:**	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch	
Testing location/ address ..... :		Room101/301/401/102/202/302/402/502/602/702/802, No. 7-2, Caipin Road, Huangpu District, Guangzhou, Guangdong, China	
☐	**Associated CB Testing Laboratory:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name, function, signature) ..... :		Luther Qiu Engineer	Luther Qiu
Approved by (name, function, signature) .. :		Jason Fu Supervisor	Jason Fu
☐	**Testing procedure: CTF Stage 1:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name, function, signature) ..... :		N/A	
Approved by (name, function, signature) .. :		N/A	
☐	**Testing procedure: CTF Stage 2:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name + signature)..... :		N/A	
Witnessed by (name, function, signature) . :		N/A	
Approved by (name, function, signature) .. :		N/A	
☐	**Testing procedure: CTF Stage 3:**	N/A	
☐	**Testing procedure: CTF Stage 4:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name, function, signature) ..... :		N/A	
Witnessed by (name, function, signature) . :		N/A	
Approved by (name, function, signature) .. :		N/A	
Supervised by (name, function, signature) :		N/A	

List of Attachments (including a total number of pages in each attachment): **N/A**	
Summary of testing:	
Tests performed (name of test and test clause): All applicable tests	**Testing location:** Intertek Testing Services Shenzhen Ltd. Guangzhou Branch Room101/301/401/102/202/302/402/502/602/702/802, No. 7-2, Caipin Road, Huangpu District, Guangzhou, Guangdong, China
Summary of compliance with National Differences (List of countries addressed): N/A ☒ **The product fulfils the requirements of** IEEE 1547: 2003 & IEEE 1547.1: 2005+ A1: 2015	

Copy of marking plate:

The artwork below may be only a draft. The use of certification marks on a product must be authorized by the respective NCBs that own these marks.

Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation.

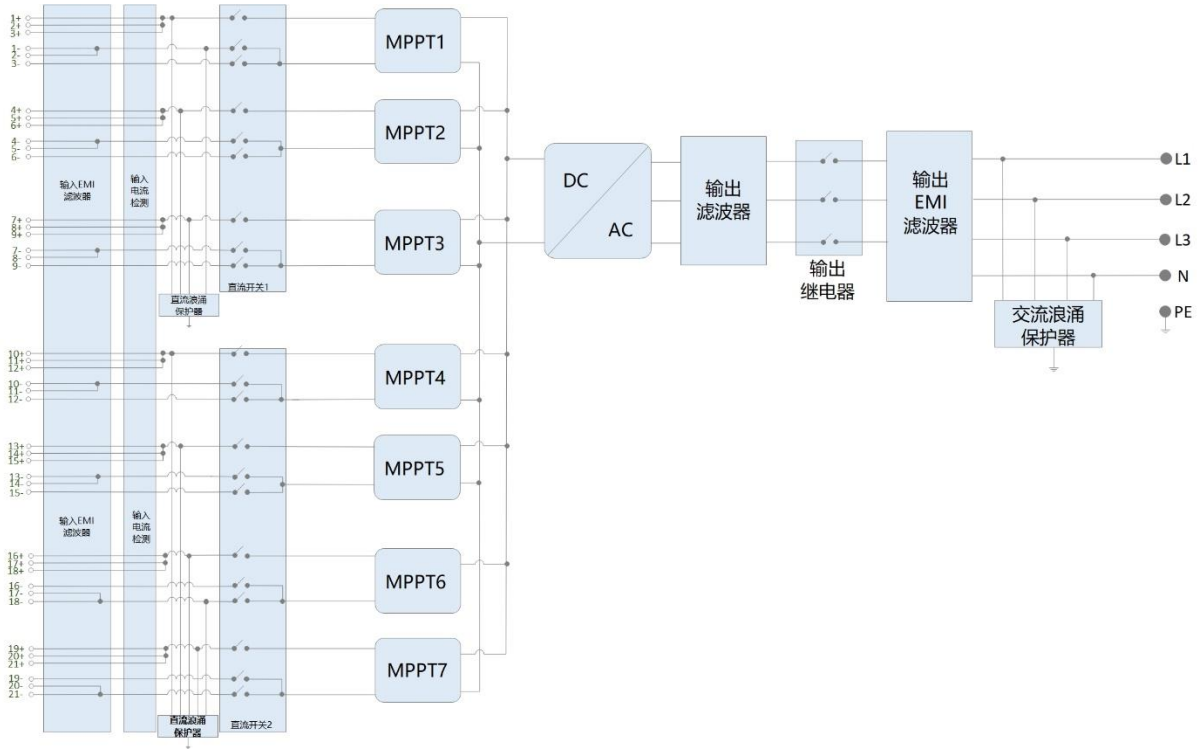
Test item particulars..... :	
Equipment mobility ..... :	☐ movable ☐ hand-held ☐ stationary ☒ fixed ☐ transportable ☐ for building-in
Connection to the mains..... :	☐ pluggable equipment ☐ direct plug-in ☒ permanent connection ☐ for building-in
Environmental category..... :	☒ outdoor ☐ indoor unconditional ☐ indoor conditional
Over voltage category Mains ..... :	☐ OVC I ☐ OVC II ☒ OVC III ☐ OVC IV
Over voltage category DC ..... :	☐ OVC I ☒ OVC II ☐ OVC III ☐ OVC IV
Mains supply tolerance (%)..... :	-90 / +110 %
Tested for power systems ..... :	TN systems
IT testing, phase-phase voltage (V)..... :	- - -
Class of equipment..... :	☒ Class I ☐ Class II ☐ Class III ☐ Not classified
Mass of equipment (kg) ..... :	Approx. 98kg
Pollution degree..... :	Outside PD3; Inside PD2
IP protection class..... :	IP 66
..... :	
Possible test case verdicts:	
- test case does not apply to the test object..... :	N/A
- test object does meet the requirement..... :	P (Pass)
- test object was not evaluated for the requirement ..... :	N/E
- test object does not meet the requirement..... :	F (Fail)
Testing..... :	
Date of receipt of test item ..... :	01 Aug 2024
Date (s) of performance of tests..... :	02 Aug 2024 ~ 02 Sep 2024

General remarks:	
"(See Enclosure #)" refers to additional information appended to the report. "(See appended table)" refers to a table appended to the report. **Throughout this report a ☐ comma / ☒ point is used as the decimal separator.**	
Manufacturer's Declaration per sub-clause 4.2.5 of IECEE 02:	
The application for obtaining a CB Test Certificate includes more than one factory location and a declaration from the Manufacturer stating that the sample(s) submitted for evaluation is (are) representative of the products from each factory has been provided ..... :	☐ **Yes** ☒ **Not applicable**
When differences exist; they shall be identified in the General product information section.	
Name and address of factory (ies) ..... :	Dongguan Luxshare Smart-Link Electronic Technology Co., Ltd. Building 2, No.313, Qingxi North Ring Road, Qingxi Town, Dongguan City, Guangdong Province, P.R. China.

General product information:

The Solar Inverter is a three-phase type (without isolating transformer inside) which converts direct current optimized by photovoltaic DC conditioner to alternating current, and they are intended to be connected in parallel with the public grid via an external isolated transformer depend on the rated output voltage of inverter. The winding ratio is adapted according to the voltage level of inverter output and connection point at public grid. They are intended for professional incorporation into PV system, and they are assessed on a component test basis.

The topology diagram as following:



Model difference:

All models of the same series have identical mechanical and electrical construction except some parameter of the software architecture to control the max output power.

SUN2000-50K-MGL0 and SUN2000-50K-MGL0-BR are differentiated between sales territories.

The product was tested on:

The Software version: SUN2000MG_V600R023C10

The Hardware version: SUN2000MG V600R023C10

Other than special notes, the model of SUN2000-80K-MGL0 is type tested.

The reference impedance: Z_source = 1,05 + j 0,32 ohm, I_SC = 210 A

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Clause	Requirement – Test	Result – Remark	Verdict

4.1	**General requirements**		**P**
4.1.1	Voltage regulation		P
	Coordination with and approval of, the area EPS and DR operators, shall be required for the DR to actively participate to regulate the voltage by changes of real and reactive power. The DR shall not cause the Area EPS service voltage at other Local EPSs to go outside the requirements of ANSI C84.1-2011 1995, Range A.	This unit is local electric power system (Local EPS). The unit is complied with specified ANSI C84.1.	P
4.1.2	Integration with Area EPS grounding		N/A
	The grounding scheme of the DR interconnection shall not cause overvoltages that exceed the rating of the equipment connected to the Area EPS and shall not disrupt the coordination of the ground fault protection on the Area EPS.	No DR interconnection.	N/A
4.1.3	Synchronization		P
	The DR unit shall parallel with the Area EPS without causing a voltage fluctuation at the PCC greater than ±5% of the prevailing voltage level of the Area EPS at the PCC,and meet the flicker requirements of 4.3.2.		P
4.1.4	Distributed resources on distribution secondary grid and spot networks		N/A
4.1.4.1	Distribution secondary grid networks		N/A
	This topic is under consideration for future revisions of this standard.		N/A
4.1.4.2	Distribution secondary spot networks		N/A
	Network protectors shall not be used to separate, switch, serve as breaker failure backup or in any manner isolate a network or network primary feeder to which DR is connected from the remainder of the Area EPS,unless the protectors are rated and t ested per applicable standards for such an application.	The unit does not included reclosing of any network protectors installed on the spot network.	N/A
	Any DR installation connected to a spot network shall not cause operation or prevent reclosing of any network protectors installed on the spot network. This coordination shall be accomplished without requiring any changes to prevailing network protector clearing time practices of the Area EPS.		N/A
	Connection of the DR to the Area EPS is only permitted if the Area EPS network bus is already energized by more than 50% of the installed network protectors.		N/A
	The DR output shall not cause any cycling of network protectors.		N/A
	The network equipment loading and fault interrupting capacity shall not be exceeded with the addition of DR.		N/A
	DR installations on a spot network, using an automatic transfer scheme in which load is transferred between the DR and the EPS in a		N/A

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	momentary make-before-break operation, shall meet all the requirements of this clause regardless of the duration of paralleling.		
4.1.5	Inadvertent energization of the Area EPS		P
	The DR shall not energize the Area EPS when the Area EPS is de-energized.		P
4.1.6	Monitoring provisions		N/A
	Each DR unit of 250 kVA or more or DR aggregate of 250 kVA or more at a single PCC shall have provisions for monitoring its connection status, real power output, reactive power output, and voltage at the point of DR connection.	This unit output is less than 250kVA.	N/A
4.1.7	Isolation device		N/A
	When required by the Area EPS operating practices, a readily accessible, lockable, visible-break isolation device shall be located between the Area EPS and the DR unit.		N/A
4.1.8	Interconnect integrity		P
4.1.8.1	Protection from electromagnetic interference		P
	The interconnection system shall have the capability to withstand electromagnetic interference (EMI) environments in accordance with IEEE Std C37.90.2-1995. The influence of EMI shall not result in a change in state or misoperation of the interconnection system.	The interconnection system have the capability to withstand electromagnetic interference (EMI).	P
4.1.8.2	Surge withstand performance		P
	The interconnection system shall have the capability to withstand voltage and current surges in accordance with the environments defined in IEEE Std C62.41.2-2002 or IEEE Std C37.90.1-2002 as applicable.		P
4.1.8.3	Paralleling device		P
	The interconnection system paralleling-device shall be capable of withstanding 220% of the interconnection system rated voltage.		P
4.2	**Response to Area EPS abnormal conditions**		**P**
	Abnormal conditions can arise on the Area EPS that require a response from the connected DR. This response contributes to the safety of utility maintenance personnel and the general public, as well as the avoidance of damage to connected equipment, including the DR. All voltage and frequency parameters specified in these subclauses shall be met at the PCC, unless otherwise stated.	Response contributed to the safety of utility maintenance personnel and the general public as well as the avoidance of damage to connected equipment.	P
4.2.1	Area EPS faults		P
	The DR unit shall cease to energize the Area EPS for faults on the Area EPS circuit to which it is connected.	The unit ceased to energize the Area EPS.	P
4.2.2	Area EPS reclosing coordination		P
	The DR shall cease to energize the Area EPS circuit to		P

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	which it is connected prior to reclosure by the Area EPS.		
4.2.3	Voltage		P
	When any voltage is in a range given in Table 1, the DR shall cease to energize the Area EPS within the clearing time as indicated. Under mutual agreement between the EPS and DR operators, other static or dynamic voltage and clearing time trip settings shall be permitted. Clearing time is the time between the start of the abnormal condition and the DR ceasing to energize the Area EPS. For DR less than or equal to 30 kW 300 W in peak capacity, the voltage set points and clearing times shall be either fixed or field adjustable. For DR greater than 30 kW 300 W, the voltage set points and clearing times shall be field adjustable.	The protection functions of the interconnection system detected the effective of fundamental frequency value of each phase to phase voltage.	P
	The voltages shall be detected at either the PCC or the point of DR connection when any of the following conditions exist:		P
	a) The aggregate capacity of DR systems connected to a single PCC is less than or equal to 30 kW,		N/A
	b) The interconnection equipment is certified to pass a non-islanding test for the system to which it is to be connected,		P
	c) The aggregate DR capacity is less than 50% of the total Local EPS minimum annual integrated electrical demand for a 15 minute time period, and export of real or reactive power by the DR to the Area EPS is not permitted.		P
	Table 1—Interconnection system default response to abnormal voltages **Default settings[a]** **Voltage range (% of base voltage[b]) / Clearing time (s) / Clearing time: adjustable up to and including (s)** V < 45 / 0.16 / 0.16 45 ≤ V < 60 / 1 / 11 60 ≤ V < 88 / 2 / 21 110 < V < 120 / 1 / 13 V ≥ 120 / 0.16 / 0.16 [a] Under mutual agreement between the EPS and DR operators, other static or dynamic voltage and clearing time trip settings shall be permitted [b] Base voltages are the nominal system voltages stated in ANSI C84.1-2011, Table 1.		P
4.2.4	Frequency		P
	When the system frequency is in a range given in Table 2, the DR shall cease to energize the Area EPS within the a pre-set clearing time as indicated. Under mutual agreement between the EPS and DR operators, other static or dynamic frequency and clearing time trip settings shall be permitted. Clearing time is the time between the start of the abnormal condition and the DR ceasing to energize the Area	Complied with Table 2.	P

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	EPS.		
	The frequency and time set points in Table 2 shall be field adjustable. Adjustable under-frequency (UF) and over-frequency (OF) trip settings shall be coordinated with the Area EPS operatortions. DR settings for frequency response shall be coordinated with load shedding schemes of the Area EPS.		P
	As mutually agreed upon by the Area EPS and DR operators, DR shall be permitted to provide modulated power output as a function of frequency in coordination with functions UF1,UF2, OF1, and OF2. Operating parameters shall be specified when this function is provided.		N/A
	Table 2—Interconnection system default response to abnormal frequencies Default settings / Ranges of adjustability Function | Frequency (Hz) | Clearing time (s) | Frequency (Hz) | Clearing time (s) adjustable up to and including UF1 | < 57 | 0.16 | 56 – 60 | 10 UF2 | < 59.5 | 2 | 56 – 60 | 300 OF1 | > 60.5 | 2 | 60 – 64 | 300 OF2 | > 62 | 0.16 | 60 – 64 | 10		P
4.2.5	Loss of synchronism		N/A
	Loss of synchronism protection is not required except as necessary to meet 4.3.2.		N/A
4.2.6	Reconnection to Area EPS		P
	After an Area EPS disturbance, no DR reconnection shall take place until the Area EPS voltage is within Range B of ANSI C84.1-1995,Table 1, and frequency range of 59.3 Hz to 60.5Hz.		P
	The DR interconnection system shall include an adjustable delay (or a fixed delay of five minutes)that may delay reconnection for up to five minutes after the Area EPS steady-state oltage and frequency are restored to the ranges identified above.		P
4.3	**Power quality**		**P**
4.3.1	Limitation of dc injection		P
	The DR and its interconnection system shall not inject dc current greater than 0.5% of the full rated output current at the point of DR connection.		P
4.3.2	Limitation of flicker induced by the DR		P
	The DR shall not create objectionable flicker for other customers on the Area EPS		P
4.3.3	Harmonics		P
	When the DR is serving balanced linear loads, harmonic current injection into the Area EPS at the PCC shall not exceed the limits stated below in Table 3. The harmonic current injections shall be exclusive of any harmonic currents due to harmonic voltage distortion present in the Area	Complied with specified Table 3.	P

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	EPS without the DR connected.		
	Table 3—Maximum harmonic current distortion in percent of current (I)[a] **Individual harmonic order h (odd harmonics)[b]** / **h < 11** / **11 ≤ h < 17** / **17 ≤ h < 23** / **23 ≤ h < 35** / **35 ≤ h** / **Total demand distortion (TDD)** Percent (%) / 4.0 / 2.0 / 1.5 / 0.6 / 0.3 / 5.0 [a] I = the greater of the Local EPS maximum load current integrated demand (15 or 30 minutes) without the DR unit, or the DR unit rated current capacity (transformed to the PCC when a transformer exists between the DR unit and the PCC). [b] Even harmonics are limited to 25% of the odd harmonic limits above.		P
4.4	Islanding		P
4.4.1	Unintentional islanding		P
	For an unintentional island in which the DR Energizes a portion of the Area EPS through the PCC, the DR interconnection system shall detect the island and cease to energize the Area EPS within two seconds of the formation of an island	DR interconnection system detected the island and cease to energize the Area EPS with two seconds.	P
4.4.2	Intentional islanding		N/A
	This topic is under consideration for future revisions of this standard.		N/A
5	**Interconnection test specifications and requirements**		**P**
	This clause provides the test requirements to demonstrate that the interconnection system meets the requirements of Clause 4. The applicable tests from this clause are required for all interconnection systems. The results of these tests shall be formally documented.		P
	The stated test specifications and requirements are universally needed for interconnection of DR including synchronous machines, induction machines, or static power inverters/converters, and will be sufficient for most installations.		P
5.1	**Design test**		**P**
	This design test shall be performed as applicable to the specific interconnection system technology. The test shall be performed on a representative sample, either in the factory, at a testing laboratory, or on equipment in the field.		P
	This test applies to a packaged interconnection system using embedded components or to an interconnection system that uses an assembly of discrete components.	Considered.	P
	The design test shall be conducted on the same sample in the sequence of Table 4.	The design test was conducted according to Table 4.	P

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Clause	Requirement – Test	Result – Remark	Verdict

	Table 4—Sequence for conducting design test **Required order** / **Design test clause and title** 1 — 5.1.1 Response to abnormal voltage and frequency 2 — 5.1.2 Synchronization 3 — 5.1.3 Interconnect integrity test **Suggested order** 4 — 5.1.1 Response to abnormal voltage and frequency 5 — 5.1.2 Synchronization 6 — 5.1.4 Unintentional islanding 7 — 5.1.5 Limitation of dc injection 8 — 5.1.6 Harmonics		P
5.1.1	Response to abnormal voltage and frequency		P
	This test shall demonstrate that the DR ceases to energize the Area EPS when the voltage or frequency exceeds the limits as specified in 4.2.3 and 4.2.4. Interconnection systems provided with field adjustable set points shall also be tested at the minimum, midpoint, and maximum of the adjustable set point ranges. These tests shall be conducted using either the simulated utility or secondary injection method.		P
5.1.2	Synchronization		N/A
	Test results conforming to requirements of A, B, or C below are accepted as indicating compliance with the requirements of 4.1.3. The appropriate conditions to be met for specific interconnection system technology follow.		N/A
A.	Synchronous interconnection to an EPS, or an energized local EPS to an energized Area EPS		N/A
	This test shall demonstrate that at the moment of the paralleling-device closure, all three parameters in Table 5 are within the stated ranges. This test shall also demonstrate that if any of the parameters are outside of the ranges stated in the table, the paralleling-device shall not close.		N/A
B.	Induction interconnection		N/A
	Self-excited induction generators shall be tested as per A in 5.1.2.		N/A
	This test shall determine the maximum start-up (in-rush) current drawn by the unit. The results shall be used, along with Area EPS impedance information for the proposed location, to estimate the starting voltage		N/A

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Table 5—Synchronization parameter limits for synchronous interconnection to an EPS, or an energized local EPS to an energized Area EPS

Aggregate rating of DR units (kVA)	Frequency difference (Δf, Hz)	Voltage difference (ΔV, %)	Phase angle difference (ΔΦ, °)
0 – 500	0.3	10	20
> 500 – 1 500	0.2	5	15
> 1 500 – 10 000	0.1	3	10

drop and verify that the unit shall not exceed the synchronization requirements in 4.1.3 and the flicker requirements in 4.3.2.

C	Inverter interconnection		P
	An inverter-based interconnection system that produces fundamental voltage before the paralleling device is closed shall be tested according to the procedure for synchronous interconnection as stated in A of 5.1.2.		P
	All other inverter-based interconnection systems shall be tested to determine the maximum start-up current. The results shall be used, along with Area EPS impedance for the proposed location, to estimate the starting voltage magnitude change and verify that the unit shall meet the synchronization requirements in 4.1.3 and the flicker requirements in 4.3.2.		N/A
5.1.3	Interconnect integrity test		P
5.1.3.1	Protection from EMI		P
	The interconnection system shall be tested in accordance with IEEE Std C37.90.2-1995 to confirm that the results are in compliance with 4.1.8.1. The influence of EMI shall not result in a change in state or mis-operation of the interconnection system.		P
5.1.3.2	Surge withstand performance		P
	The interconnection system shall be tested for the requirement in 4.1.8.2 in all normal operating modes in accordance with IEEE Std C62.45-2002 for equipment rated less than 1000 V to confirm that the surge withstand capability is met by using the selected test level(s) from IEEE Std C62.41.2-2002. Interconnection system equipment rated greater than 1000 V shall be tested in accordance with manufacturer or system integrator designated applicable standards. For interconnection system equipment signal and control circuits, use IEEE Std C37.90.1-2002. The results		P
5.1.3.3	Paralleling device		P
	A dielectric test across the open-circuited paralleling device shall be conducted to confirm compliance with the requirements of 4.1.8.3.		P
5.1.4	Unintentional Islanding		P
	A test or field verification shall be conducted to confirm that 4.4.1 is met regardless of the selected method of detecting isolation.		P

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5.1.5	Limitation of dc injection		P
	Inverter based DR shall be tested to confirm that the DR does not inject dc current greater than prescribed limits that are listed in 4.3.1.		P
5.1.6	Harmonics		P
	The intent of the harmonics interconnection test is to assess that under a controlled set of conditions the DR unit meets the harmonic limits specified in 4.3.3.		P
	The DR shall be operated in parallel with a predominantly inductive voltage source with a short circuit current capacity ISC of not less than 20 times the DR rated output current at fundamental frequency. The voltage and frequency output of the voltage source shall correspond to the rated voltage and frequency of the DR. The unloaded voltage waveform produced by the Area EPS or simulated utility voltage source shall have a total harmonic distortion (THD) less than 2.5%.		P
	The DR shall be operated at an output test load current, IL, of 33%, 66%, and at a level as close to 100% of rated output current as practical. Use total rated-current distortion (TRD) in place of TDD. TRD is the total rms value of the sum of the current harmonics created by the DR unit operating into a linear balanced load divided by the greater of the test load current (IL) demand or the rated current capacity of the DR unit (Irated). The individual harmonic distortion and TRD of the DR output current shall be measured for the first 40 harmonics. The harmonic current injections shall be exclusive of any harmonic currents due to harmonic voltage distortion present in the Area EPS without the DR connected. The test results shall not exceed the values in 4.3.3, Table 3.	The unit has operated at an output test load 33%, 66% and at a level as close to100%	P
	As an alternative, a synchronous generator DR shall be tested to meet the requirements of 4.3.3; either after installation or while powering a balanced resistive load and isolated from any other sources. The voltage harmonics while powering a resistive load at 100% of the machine kVA rating shall not exceed the levels in Table 6. Voltage harmonics shall be measured line to line for 3-phase/3 wire systems, and line to neutral for 3-phase/4-wire systems.		N/A
	Table 6—Maximum harmonic voltage distortion in percent of rated voltage for synchronous machines Individual harmonic order: h < 11 | 11 ≤ h < 17 | 17 ≤ h < 23 | 23 ≤ h < 35 | 35 ≤ h | Total harmonic distortion Percent (%): 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0		N/A
5.2	**Production tests**		N/A

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	Each interconnection system shall be subjected to requirements of 5.1.1 and 5.1.2. Interconnection systems with adjustable set points shall be tested at a single set of set points as specified by the manufacturer. This test may be conducted as a factory test or may be performed as part of a commissioning test (see 5.4)**.**	Considered by the manufacturer during production	N/A
5.3	**Interconnection installation evaluation**		**N/A**
5.3.1	Grounding integration with Area EPS		N/A
	A system design verification shall be made to ensure that the requirements of 4.1.2 have been met.		N/A
5.3.2	Isolation device		N/A
	A system design verification shall be made to ensure that the requirements of 4.1.7 have been met.		N/A
5.3.3	Monitoring provisions		N/A
	A system design verification shall be made to ensure that the provisions for monitoring are in accordance with 4.1.6.		N/A
5.3.4	Area EPS faults		N/A
	A system design verification shall be made to ensure that the requirements of 4.2.1 have been met.		N/A
5.3.5	Area EPS reclosing coordination		N/A
	A system design verification shall be made to verify the interconnection system is coordinated with the Area EPS reclosing practices in accordance with 4.2.2.		N/A
5.4	**Commissioning tests**		N/A
	All commissioning tests shall be performed based on written test procedures.19 The following visual inspections shall be performed.		N/A
	— A visual inspection shall be made to ensure that the grounding coordination requirement of 4.1.2 has been implemented. — A visual inspection shall be made to confirm the presence of the isolation device if required by 4.1.7.		N/A
	Initial commissioning tests shall be performed on the installed DR and interconnection system equipment prior to the initial parallel operation of the DR. The following tests are required:		N/A
	— Operability test on the isolation device — Unintentional-islanding functionality as specified in 5.4.1 — Cease to energize functionality as specified in 5.4.2 — Any tests of 5.1 that have not been previously performed on a representative sample and formally documented		N/A

IEEE1547			
Clause	Requirement – Test	Result – Remark	Verdict

	— Any tests of 5.2 that have not been previously performed		
	The applicable tests of 5.1 shall be repeated when:		N/A
	— Functional software or firmware changes have been made on the interconnection system — Any hardware component of the interconnection system has been modified in the field, or, replaced or repaired with parts different from the tested configuration.	Manufactuer has control and procedure to verify changes software or firmware.	N/A
	Sublauses 5.4.1 and 5.4.2, and the applicable tests of 5.2 shall be repeated if:		N/A
	— Protection settings have been changed after factory testing. — Protection functions have been adjusted after the initial commissioning process.		N/A
5.4.1	Unintentional islanding functionality test		N/A
5.4.1.1	Reverse-power or minimum power test		N/A
	A reverse-power or minimum power function, if used to meet the requirements of 4.4.1, shall be tested using injection techniques or by adjusting the DR output and local loads to verify that the reverse power or minimum power function is met.		N/A
5.4.1.2	Non-islanding functionality test		N/A
	For non-islanding interconnection systems, 5.4.2 satisfies this requirement.		N/A
5.4.1.3	Other unintentional islanding functionality tests		N/A
	If tests in 5.4.1.1 and 5.4.1.2 are not applicable to the interconnection system, the interconnection system shall be tested in accordance with procedures provided by the manufacturer or system integrator.		N/A
5.4.2	Cease to energize functionality test		N/A
	Check the cease to energize functionality by operating a load interrupting device and verify the equipment ceases to energize its output terminals and does not restart/reconnect for the required time delay. The test shall be performed on each phase individually. This test verifies conformance to the cease to energize requirement of 4.1.4, 4.2.1, 4.2.2, 4.2.3, 4.2.4, and 4.4.1.		N/A
5.5	**Periodic interconnection tests**		**N/A**
	All interconnection-related protective functions and associated batteries shall be periodically tested at intervals specified by the manufacturer, system integrator, or the authority who has jurisdiction over the DR interconnection. Periodic test reports or a log for inspection shall be maintained.		N/A

Testing Result

4.1.8	Interconnect integrity	P

Performance Criterion:

A - operate as intended during and after the test
B - operate as intended after the test
C - loss/error of function

Required Criterion: B

☑ For IEEE Std C62.41.2 ™ -2002

Test Port	Applied Voltage (kV)	Repetition Frequency (kHz)	Result
A.C. Power supply line	±4kV	2.5k	A

☑ For IEEE Std C37.90.1 ™ -2002

Test Port	Applied Voltage (kV)	Repetition Frequency (kHz)	Result
D.C. Power supply line	±4kV	2.5k	A
External signal and control circuits	±4kV	2.5k	A

Performance Criterion:

A - operate as intended during and after the test
B - operate as intended after the test
C - loss/error of function

Required Criterion: B

Test Port	Applied Voltage (kV)	Result
A.C. Power supply line	Line to line ±6kV	A
A.C. Power supply line	line to earth ±6kV	A

Testing Result

5.2	Test for response to abnormal voltage conditions (25℃)					P
Testing item	Tripping voltage/ Clearing time setting	Measured Tripping voltage/ Clearing time				
		Phase	1	2	3	4	5
Voltage - under (V≤45%)	45%Un/ 0.16s	L1-N	57.13V/ 0.135s	57.14V/ 0.143s	57.15V/ 0.148s	57.14V/ 0.146s	57.15V/ 0.129s
		L2-N	56.53V/ 0.128s	56.82V/ 0.126s	56.75V/ 0.131s	56.75V/ 0.139s	56.88V/ 0.133s
		L3-N	56.49V/ 0.136s	56.48V/ 0.138s	56.49V/ 0.132s	56.50V/ 0.139s	56.69V/ 0.147s
		L1L2L3-N	57.11V/ 0.140s	57.10V/ 0.139s	57.12V/ 0.145s	57.12V/ 0.129s	57.13V/ 0.129s
Voltage - under (45%≤V<60%)	45%Un/ 1s	L1-N	57.14V/ 0.978s	57.10V/ 0.984s	57.13V/ 0.972s	57.15V/ 0.983s	57.13V/ 0.977s
		L2-N	56.54V/ 0.980s	56.53V/ 0.982s	56.52V/ 0.977s	56.53V/ 0.990s	56.53V/ 0.988s
		L3-N	56.28V/ 0.988s	56.09V/ 0.980s	56.10V/ 0.983s	56.30V/ 0.971s	56.30V/ 0.974s
		L1L2L3-N	57.12V/ 0.982s	57.11V/ 0.985s	57.12V/ 0.985s	57.12V/ 0.987s	57.12V/ 0.988s
	50%Un/ 6s	L1-N	63.51V/ 5.964s	63.52V/ 5.984s	63.51V/ 5.980s	63.54V/ 5.973s	63.52V/ 5.977s
		L2-N	62.97V/ 5.978s	62.95V/ 5.981s	62.95V/ 5.985s	62.96V/ 5.986s	62.96V/ 5.980s
		L3-N	62.71V/ 5.982s	62.72V/ 5.973s	62.55V/ 5.983s	62.82V/ 5.975s	62.65V/ 5.986s
		L1L2L3-N	63.59V/ 5.974s	63.52V/ 5.969s	63.59V/ 5.981s	63.51V/ 5.984s	63.53V/ 5.973s
	59%Un/ 11s	L1-N	74.94V/ 10.971s	74.94V/ 10.986s	74.94V/ 10.976s	74.93V/ 10.983s	74.94V/ 10.968s
		L2-N	74.57V/ 10.980s	74.57V/ 10.969s	74.58V/ 10.975s	74.63V/ 10.981s	74.57V/ 10.974s
		L3-N	74.11V/ 10.974s	74.13V/ 10.978s	74.11V/ 10.967s	74.11V/ 10.977s	74.12V/ 10.975s
		L1L2L3-N	74.95V/ 10.970s	74.93V/ 10.970s	74.93V/ 10.976s	74.99V/ 10.980s	75.00V/ 10.980s
Voltage - under (60%≤V<88%)	60%Un/ 2s	L1-N	76.05V/ 1.986s	76.07V/ 1.979s	76.03V/ 1.975s	76.03V/ 1.966s	76.05V/ 1.978s
		L2-N	75.86V/ 1.985s	75.86V/ 1.976s	75.87V/ 1.976s	75.87V/ 1.978s	75.87V/ 1.980s
		L3-N	75.74V/ 1.981s	75.72V/ 1.971s	75.62V/ 1.979s	75.62V/ 1.979s	75.61V/ 1.983s
		L1L2L3-N	76.09V/ 1.986s	76.03V/ 1.986s	76.02V/ 1.973s	76.03V/ 1.973s	76.04V/ 1.972s
	74%Un/ 11.5s	L1-N	93.76V/ 11.467s	93.78V/ 11.479s	93.56V/ 11.475s	93.56V/ 11.465s	93.75V/ 11.479s
		L2-N	93.79V/ 11.471s	93.79V/ 11.471s	93.80V/ 11.474s	93.81V/ 11.483s	93.79V/ 11.476s
		L3-N	93.53V/ 11.469s	93.60V/ 11.477s	93.53V/ 11.478s	93.53V/ 11.483s	93.54V/ 11.480s

Testing Result

		L1L2L3-N	93.55V/ 11.473s	93.74V/ 11.479s	93.62V/ 11.469s	93.55V/ 11.486s	93.55V/ 11.486s
	87%Un/ 21s	L1-N	110.09V/ 20.975s	110.11V/ 20.973s	110.07V/ 20.968s	110.05V/ 20.962s	110.07V/ 20.974s
		L2-N	109.50V/ 20.969s	109.69V/ 20.987s	109.71V/ 20.982s	109.70V/ 20.972s	109.50V/ 20.969s
		L3-N	109.46V/ 20.985s	109.33V/ 20.966s	109.31V/ 20.970s	109.44V/ 20.982s	109.46V/ 20.977s
		L1L2L3-N	110.25V/ 20.981s	110.25V/ 20.985s	110.32V/ 20.972s	110.31V/ 20.977s	110.26V/ 20.980s
Voltage – over (110%<V<120 %)	111%Un/ 1s	L1-N	140.96V/ 0.985s	140.95V/ 0.974s	140.95V/ 0.983s	140.96V/ 0.967s	140.95V/ 0.973s
		L2-N	141.23V/ 0.969s	141.24V/ 0.971s	141.22V/ 0.978s	141.26V/ 0.984s	141.23V/ 0.967s
		L3-N	141.38V/ 0.969s	141.58V/ 0.974s	141.57V/ 0.966s	141.56V/ 0.979s	141.57V/ 0.978s
		L1L2L3-N	140.76V/ 0.984s	140.83V/ 0.971s	140.62V/ 0.978s	140.56V/ 0.983s	140.63V/ 0.968s
	115%Un/ 7s	L1-N	146.06V/ 6.981s	146.05V/ 6.978s	146.06V/ 6.974s	146.06V/ 6.976s	146.06V/ 6.971s
		L2-N	146.75V/ 6.965s	146.74V/ 6.974s	146.73V/ 6.986s	146.73V/ 6.977s	146.74V/ 6.985s
		L3-N	147.08V/ 6.981s	147.07V/ 6.970s	147.06V/ 6.976s	147.08V/ 6.962s	147.07V/ 6.963s
		L1L2L3-N	145.86V/ 6.980s	145.94V/ 6.978s	145.89V/ 6.976s	145.86V/ 6.969s	145.86V/ 6.989s
	119%Un/ 13s	L1-N	151.43V/ 12.972s	151.36V/ 12.974s	151.35V/ 12.966s	151.36V/ 12.963s	151.35V/ 12.975s
		L2-N	151.84V/ 12.980s	151.83V/ 12.968s	151.84V/ 12.984s	151.84V/ 12.977s	151.85V/ 12.978s
		L3-N	152.17V/ 12.976s	152.18V/ 12.983s	152.17V/ 12.974s	152.17V/ 12.986s	152.18V/ 12.977s
		L1L2L3-N	150.96V/ 12.976s	150.97V/ 12.981s	150.96V/ 12.969s	150.99V/ 12.984s	150.96V/ 12.976s
Voltage – over (≥120%)	120%Un/ 0.16s	L1-N	152.45V/ 0.131s	152.45V/ 0.124s	152.12V/ 0.137s	152.47V/ 0.133s	152.45V/ 0.132s
		L2-N	153.05V/ 0.145s	153.04V/ 0.141s	153.04V/ 0.144s	153.03V/ 0.141s	153.05V/ 0.138s
		L3-N	152.97V/ 0.138s	152.98V/ 0.134s	152.96V/ 0.139s	152.97V/ 0.147s	152.97V/ 0.137s
		L1L2L3-N	152.47V/ 0.148s	151.94V/ 0.146s	152.46V/ 0.135s	152.49V/ 0.128s	152.45V/ 0.131s

Testing Result

5.2	Test for response to abnormal voltage conditions (-25℃)					P
Testing item	Tripping voltage/ Clearing time setting	Measured Tripping voltage/ Clearing time				
		Phase	1	2	3	4	5
Voltage - under (V≤45%)	45%Un/ 0.16s	L1-N	57.13V/ 0.136s	57.13V/ 0.140s	57.14V/ 0.146s	57.14V/ 0.137s	57.12V/ 0.126s
		L2-N	57.15V/ 0.132s	56.76V/ 0.139s	57.15V/ 0.145s	57.15V/ 0.144s	57.15V/ 0.137s
		L3-N	56.77V/ 0.128s	56.53V/ 0.135s	56.73V/ 0.142s	56.74V/ 0.139s	56.69V/ 0.139s
		L1L2L3-N	56.51V/ 0.141s	56.50V/ 0.133s	56.49V/ 0.145s	56.59V/ 0.132s	56.62V/ 0.141s
Voltage - under (45%≤V<60%)	45%Un/ 1s	L1-N	57.14V/ 0.965s	57.21V/ 0.976s	57.19V/ 0.970s	57.20V/ 0.983s	57.13V/ 0.966s
		L2-N	56.42V/ 0.975s	56.30V/ 0.973s	56.42V/ 0.981s	56.29V/ 0.968s	56.29V/ 0.976s
		L3-N	56.95V/ 0.986s	56.94V/ 0.979s	57.07V/ 0.990s	56.97V/ 0.981s	56.93V/ 0.978s
		L1L2L3-N	57.12V/ 0.975s	57.11V/ 0.978s	57.12V/ 0.981s	57.12V/ 0.979s	57.12V/ 0.978s
	50%Un/ 6s	L1-N	63.33V/ 5.973s	63.39V/ 5.971s	63.33V/ 5.964s	63.34V/ 5.981s	63.32V/ 5.970s
		L2-N	62.97V/ 5.971s	63.33V/ 5.977s	63.40V/ 5.989s	62.96V/ 5.974s	63.33V/ 5.984s
		L3-N	63.32V/ 5.981s	63.39V/ 5.984s	63.32V/ 5.980s	63.33V/ 5.975s	63.36V/ 5.989s
		L1L2L3-N	63.39V/ 5.984s	63.33V/ 5.983s	63.32V/ 5.976s	63.39V/ 5.977s	63.23V/ 5.981s
	59%Un/ 11s	L1-N	74.73V/ 10.977s	74.79V/ 10.983s	74.72V/ 10.970s	74.79V/ 10.977s	74.80V/ 10.975s
		L2-N	74.80V/ 10.975s	74.76V/ 10.980s	74.77V/ 10.966s	74.74V/ 10.981s	74.97V/ 10.981s
		L3-N	74.93V/ 10.984s	74.73V/ 10.975s	74.80V/ 10.975s	74.72V/ 10.983s	74.72V/ 10.981s
		L1L2L3-N	74.95V/ 10.979s	74.90V/ 10.981s	74.83V/ 10.978s	74.80V/ 10.985s	74.90V/ 10.983s
Voltage - under (60%≤V<88%)	60%Un/ 2s	L1-N	76.03V/ 1.981s	76.10V/ 1.978s	76.03V/ 1.979s	76.03V/ 1.976s	76.05V/ 1.975s
		L2-N	76.05V/ 1.972s	76.06V/ 1.972s	76.11V/ 1.984s	75.97V/ 1.984s	76.07V/ 1.977s
		L3-N	76.24V/ 1.970s	76.32V/ 1.981s	75.78V/ 1.973s	75.89V/ 1.977s	75.90V/ 1.975s
		L1L2L3-N	76.04V/ 1.986s	76.05V/ 1.981s	76.03V/ 1.975s	76.03V/ 1.973s	76.04V/ 1.972s
	74%Un/ 11.5s	L1-N	93.75V/ 11.469s	93.81V/ 11.470s	93.56V/ 11.471s	93.75V/ 11.477s	93.74V/ 11.471s
		L2-N	93.80V/ 11.482s	93.73V/ 11.474s	93.74V/ 11.476s	93.83V/ 11.484s	93.83V/ 11.488s
		L3-N	93.73V/ 11.471s	93.74V/ 11.481s	93.73V/ 11.471s	93.83V/ 11.489s	93.74V/ 11.485s

Testing Result

		L1L2L3-N	93.79V/ 11.474s	93.76V/ 11.475s	93.72V/ 11.487s	93.81V/ 11.485s	93.80V/ 11.474s
	87%Un/ 21s	L1-N	110.25V/ 20.976s	110.32V/ 20.973s	110.26V/ 20.969s	110.27V/ 20.977s	110.33V/ 20.974s
		L2-N	110.30V/ 20.966s	110.31V/ 20.982s	110.25V/ 20.987s	110.33V/ 20.983s	110.23V/ 20.975s
		L3-N	110.46V/ 20.987s	110.33V/ 20.970s	110.28V/ 20.974s	110.31V/ 20.965s	110.36V/ 20.979s
		L1L2L3-N	110.25V/ 20.965s	110.26V/ 20.967s	110.31V/ 20.982s	110.31V/ 20.977s	110.26V/ 20.970s
Voltage – over (110%<V<120 %)	111%Un/ 1s	L1-N	140.96V/ 0.969s	140.95V/ 0.982s	140.95V/ 0.971s	140.96V/ 0.969s	140.95V/ 0.968s
		L2-N	141.23V/ 0.977s	141.24V/ 0.975s	141.22V/ 0.971s	141.26V/ 0.968s	141.23V/ 0.967s
		L3-N	141.38V/ 0.976s	141.58V/ 0.972s	141.57V/ 0.984s	141.56V/ 0.980s	141.57V/ 0.967s
		L1L2L3-N	140.76V/ 0.973s	140.83V/ 0.969s	140.62V/ 0.974s	140.56V/ 0.973s	140.63V/ 0.971s
	115%Un/ 7s	L1-N	146.06V/ 6.982s	146.05V/ 6.982s	146.06V/ 6.979s	146.06V/ 6.974s	146.06V/ 6.977s
		L2-N	146.75V/ 6.973s	146.74V/ 6.985s	146.73V/ 6.985s	146.73V/ 6.974s	146.74V/ 6.979s
		L3-N	147.08V/ 6.978s	147.07V/ 6.972s	147.06V/ 6.980s	147.08V/ 6.984s	147.07V/ 6.972s
		L1L2L3-N	145.86V/ 6.978s	145.94V/ 6.968s	145.89V/ 6.989s	145.86V/ 6.980s	145.86V/ 6.983s
	119%Un/ 13s	L1-N	151.43V/ 12.972s	151.36V/ 12.979s	151.35V/ 12.979s	151.36V/ 12.984s	151.35V/ 12.982s
		L2-N	151.84V/ 12.981s	151.83V/ 12.979s	151.84V/ 12.970s	151.84V/ 12.973s	151.85V/ 12.975s
		L3-N	152.17V/ 12.980s	152.18V/ 12.980s	152.17V/ 12.971s	152.17V/ 12.969s	152.18V/ 12.979s
		L1L2L3-N	150.96V/ 12.976s	150.97V/ 12.984s	150.96V/ 12.984s	150.99V/ 12.998s	150.96V/ 12.972s
Voltage – over (≥120%)	120%Un/ 0.16s	L1-N	152.45V/ 0.137s	152.45V/ 0.128s	152.12V/ 0.134s	152.47V/ 0.124s	152.45V/ 0.145s
		L2-N	153.05V/ 0.142s	153.04V/ 0.139s	153.04V/ 0.146s	153.03V/ 0.138s	153.05V/ 0.133s
		L3-N	152.97V/ 0.136s	152.98V/ 0.136s	152.96V/ 0.134s	152.97V/ 0.124s	152.97V/ 0.133s
		L1L2L3-N	152.47V/ 0.143s	151.94V/ 0.137s	152.46V/ 0.126s	152.49V/ 0.141s	152.45V/ 0.139s

Testing Result

5.2	Test for response to abnormal voltage conditions (60℃)					P
Testing item	Tripping voltage/ Clearing time setting	Measured Tripping voltage/ Clearing time				
		Phase	1	2	3	4	5
Voltage - under (V≤45%)	45%Un/ 0.16s	L1-N	56.93V/ 0.136s	56.91V/ 0.141s	56.89V/ 0.145s	56.93V/ 0.136s	56.94V/ 0.139s
		L2-N	56.35V/ 0.142s	56.33V/ 0.141s	56.71V/ 0.131s	56.74V/ 0.137s	56.74V/ 0.129s
		L3-N	56.50V/ 0.138s	56.48V/ 0.139s	56.49V/ 0.146s	56.29V/ 0.140s	56.30V/ 0.128s
		L1L2L3-N	56.93V/ 0.137s	56.99V/ 0.141s	56.93V/ 0.148s	56.99V/ 0.147s	57.00V/ 0.129s
Voltage - under (45%≤V<60%)	45%Un/ 1s	L1-N	56.98V/ 0.969s	56.91V/ 0.975s	56.91V/ 0.973s	56.93V/ 0.973s	56.94V/ 0.979s
		L2-N	56.34V/ 0.986s	56.43V/ 0.981s	56.33V/ 0.985s	56.34V/ 0.975s	56.33V/ 0.971s
		L3-N	56.30V/ 0.982s	56.27V/ 0.974s	56.28V/ 0.979s	56.31V/ 0.978s	56.31V/ 0.973s
		L1L2L3-N	56.92V/ 0.984s	57.00V/ 0.984s	56.93V/ 0.988s	56.99V/ 0.976s	56.93V/ 0.982s
	50%Un/ 6s	L1-N	63.33V/ 5.974s	63.38V/ 5.979s	63.34V/ 5.971s	63.34V/ 5.975s	63.34V/ 5.978s
		L2-N	62.75V/ 5.978s	62.74V/ 5.977s	62.74V/ 5.978s	62.75V/ 5.977s	63.76V/ 5.976s
		L3-N	62.70V/ 5.984s	62.70V/ 5.974s	62.71V/ 5.986s	62.70V/ 5.974s	62.68V/ 5.969s
		L1L2L3-N	63.32V/ 5.978s	63.39V/ 5.974s	63.34V/ 5.974s	63.40V/ 5.983s	63.34V/ 5.972s
	59%Un/ 11s	L1-N	74.73V/ 10.979s	74.79V/ 10.979s	74.73V/ 10.987s	74.72V/ 10.974s	74.78V/ 10.979s
		L2-N	74.72V/ 10.984s	74.73V/ 10.986s	74.80V/ 10.979s	74.73V/ 10.979s	74.72V/ 10.986s
		L3-N	74.76V/ 10.974s	74.81V/ 10.981s	74.76V/ 10.976s	74.73V/ 10.982s	74.79V/ 10.984s
		L1L2L3-N	74.72V/ 10.970s	74.90V/ 10.975s	74.60V/ 10.972s	74.62V/ 10.977s	74.54V/ 10.981s
Voltage - under (60%≤V<88%)	60%Un/ 2s	L1-N	76.04V/ 1.981s	76.10V/ 1.973s	76.04V/ 1.978s	76.02V/ 1.986s	76.09V/ 1.979s
		L2-N	76.02V/ 1.967s	76.03V/ 1.976s	76.09V/ 1.989s	76.03V/ 1.972s	76.03V/ 1.980s
		L3-N	76.09V/ 1.984s	76.03V/ 1.980s	76.04V/ 1.985s	76.10V/ 1.968s	76.03V/ 1.980s
		L1L2L3-N	76.04V/ 1.979s	76.04V/ 1.984s	76.04V/ 1.974s	76.14V/ 1.973s	76.04V/ 1.972s
	74%Un/ 11.5s	L1-N	93.39V/ 11.469s	93.40V/ 11.478s	93.34V/ 11.484s	93.33V/ 11.472s	93.50V/ 11.474s
		L2-N	93.74V/ 11.476s	93.34V/ 11.471s	93.40V/ 11.486s	93.33V/ 11.481s	93.34V/ 11.474s
		L3-N	93.40V/ 11.475s	93.34V/ 11.488s	93.33V/ 11.475s	93.40V/ 11.475s	93.34V/ 11.474s

Testing Result

		L1L2L3-N	93.78V/ 11.471s	93.77V/ 11.470s	93.74V/ 11.474s	93.38V/ 11.471s	93.80V/ 11.474s
	87%Un/ 21s	L1-N	110.24V/ 20.970s	110.35V/ 20.981s	110.27V/ 20.971s	110.43V/ 20.962s	110.25V/ 20.983s
		L2-N	110.31V/ 20.979s	110.35V/ 20.976s	110.31V/ 20.968s	110.25V/ 20.982s	110.26V/ 20.976s
		L3-N	110.24V/ 20.986s	110.29V/ 20.964s	110.35V/ 20.976s	110.24V/ 20.973s	110.25V/ 20.978s
		L1L2L3-N	110.24V/ 20.974s	110.30V/ 20.979s	110.24V/ 20.982s	110.31V/ 20.978s	110.30V/ 20.981s
Voltage – over (110%<V<120 %)	111%Un/ 1s	L1-N	140.76V/ 0.969s	140.75V/ 0.974s	140.82V/ 0.965s	140.86V/ 0.964s	140.83V/ 0.972s
		L2-N	140.75V/ 0.964s	140.76V/ 0.973s	140.71V/ 0.970s	140.81V/ 0.977s	140.79V/ 0.970s
		L3-N	141.14V/ 0.983s	141.18V/ 0.969s	141.15V/ 0.972s	141.15V/ 0.970s	141.15V/ 0.970s
		L1L2L3-N	141.23V/ 0.979s	141.25V/ 0.969s	141.22V/ 0.974s	141.22V/ 0.963s	141.27V/ 0.978s
	115%Un/ 7s	L1-N	145.86V/ 6.977s	145.92V/ 6.978s	145.86V/ 6.980s	145.87V/ 6.976s	145.93V/ 6.978s
		L2-N	145.88V/ 6.978s	145.91V/ 6.978s	145.94V/ 6.971s	145.90V/ 6.968s	145.92V/ 6.978s
		L3-N	145.87V/ 6.970s	145.92V/ 6.978s	145.96V/ 6.978s	145.88V/ 6.981s	145.87V/ 6.972s
		L1L2L3-N	145.95V/ 6.980s	145.94V/ 6.974s	145.92V/ 6.978s	145.88V/ 6.970s	145.96V/ 6.976s
	119%Un/ 13s	L1-N	151.04V/ 12.984s	151.06V/ 12.976s	151.03V/ 12.961s	150.97V/ 12.979s	151.06V/ 12.969s
		L2-N	150.97V/ 12.974s	150.96V/ 12.978s	151.01V/ 12.985s	150.95V/ 12.967s	150.96V/ 12.984s
		L3-N	151.02V/ 12.969s	150.98V/ 12.976s	150.97V/ 12.986s	151.05V/ 12.977s	151.18V/ 12.981s
		L1L2L3-N	150.97V/ 12.982s	150.99V/ 12.983s	151.06V/ 12.966s	150.99V/ 12.970s	150.95V/ 12.972s
Voltage – over (≥120%)	120%Un/ 0.16s	L1-N	152.46V/ 0.136s	152.52V/ 0.135s	152.46V/ 0.131s	151.96V/ 0.138s	152.02V/ 0.144s
		L2-N	152.97V/ 0.141s	152.84V/ 0.142s	152.74V/ 0.142s	152.83V/ 0.131s	152.75V/ 0.129s
		L3-N	152.01V/ 0.140s	152.95V/ 0.136s	152.01V/ 0.134s	152.96V/ 0.139s	152.95V/ 0.139s
		L1L2L3-N	152.97V/ 0.126s	151.95V/ 0.141s	152.94V/ 0.134s	152.04V/ 0.141s	152.06V/ 0.140s

Testing Result

5.3	Response to abnormal frequency conditions (25℃)					P
Testing item	Tripping frequency/ Clearing time setting	Measured Tripping frequency/ Clearing time				
		1	2	3	4	5
Frequency - under UF1	56.00Hz/ 2s	55.990Hz/ 1.987s	55.990Hz/ 1.986s	56.000Hz/ 1.988s	55.990Hz/ 1.979s	56.000Hz/ 1.978s
Frequency - under UF1	58.00Hz/ 151s	57.990Hz/ 150.980s	57.990Hz/ 150.990s	57.990Hz/ 150.980s	57.990Hz/ 150.990s	57.990Hz/ 150.990s
Frequency - under UF1	59.50Hz/ 300s	59.490Hz/ 299.980s	59.490Hz/ 299.980s	59.490Hz/ 299.980s	59.489Hz/ 299.970s	59.490Hz/ 299.970s
Frequency - under UF2	56.00Hz/ 0.16s	55.990Hz/ 0.141s	55.990Hz/ 0.141s	55.990Hz/ 0.134s	55.990Hz/ 0.138s	55.990Hz/ 0.143s
Frequency - under UF2	58.00Hz/ 5s	57.990Hz/ 4.975s	57.990Hz/ 4.970s	57.990Hz/ 4.974s	57.990Hz/ 4.974s	57.990Hz/ 4.986s
Frequency - under UF2	59.50Hz/ 10s	59.499Hz/ 9.978s	59.500Hz/ 9.976s	59.499Hz/ 9.982s	59.500Hz/ 9.966s	59.500Hz/ 9.964s
Frequency - over OF1	60.50Hz/ 2s	60.500Hz/ 1.973s	60.500Hz/ 1.976s	60.500Hz/ 1.972s	60.500Hz/ 1.967s	60.500Hz/ 1.984s
Frequency - over OF1	62.00Hz/ 151s	62.010Hz/ 150.970s	62.010Hz/ 150.980s	62.010Hz/ 150.980s	62.010Hz/ 150.970s	62.010Hz/ 150.980s
Frequency - over OF1	64.00Hz/ 300s	64.009Hz/ 299.970s	64.010Hz/ 299.970s	64.010Hz/ 299.980s	64.010Hz/ 299.980s	64.010Hz/ 299.970s
Frequency - over OF2	60.50Hz/ 0.16s	60.510Hz/ 0.134s	60.510Hz/ 0.131s	60.510Hz/ 0.124s	60.510Hz/ 0.129s	60.510Hz/ 0.133s
Frequency - over OF2	62.00Hz/ 5s	62.010Hz/ 4.981s	62.010Hz/ 4.966s	62.010Hz/ 4.971s	62.010Hz/ 4.983s	62.010Hz/ 4.973s
Frequency - over OF2	64.00Hz/ 10s	64.010Hz/ 9.972s	64.010Hz/ 9.970s	64.010Hz/ 9.975s	64.010Hz/ 9.984s	64.010Hz/ 9.997s

Testing Result

5.3	Response to abnormal frequency conditions (-25℃)	P

Testing item	Tripping frequency/ Clearing time setting	Measured Tripping frequency/ Clearing time				
		1	2	3	4	5
Frequency - under UF1	56.00Hz/ 2s	55.990Hz/ 1.985s	55.990Hz/ 1.983s	55.990Hz/ 1.970s	55.990Hz/ 1.975s	55.990Hz/ 1.984s
Frequency - under UF1	58.00Hz/ 151s	57.990Hz/ 150.970s	57.990Hz/ 150.980s	57.990Hz/ 150.980s	57.990Hz/ 150.980s	57.990Hz/ 150.970s
Frequency - under UF1	59.50Hz/ 300s	59.490Hz/ 299.980s	59.490Hz/ 299.980s	59.490Hz/ 299.980s	59.490Hz/ 299.970s	59.490Hz/ 299.970s
Frequency - under UF2	56.00Hz/ 0.16s	55.990Hz/ 0.143s	55.990Hz/ 0.147s	55.990Hz/ 0.143s	55.990Hz/ 0.138s	55.990Hz/ 0.134s
Frequency - under UF2	58.00Hz/ 5s	57.990Hz/ 4.976s	57.990Hz/ 4.979s	57.990Hz/ 4.976s	57.990Hz/ 4.975s	57.900Hz/ 4.977s
Frequency - under UF2	59.50Hz/ 10s	59.490Hz/ 9.967s	59.490Hz/ 9.971s	59.490Hz/ 9.975s	59.490Hz/ 9.981s	59.490Hz/ 9.964s
Frequency - over OF1	60.50Hz/ 2s	60.500Hz/ 1.975s	60.500Hz/ 1.977s	60.500Hz/ 1.966s	60.500Hz/ 1.980s	60.500Hz/ 1.980s
Frequency - over OF1	62.00Hz/ 151s	62.010Hz/ 150.980s	62.010Hz/ 150.970s	62.010Hz/ 150.980s	62.010Hz/ 150.980s	62.010Hz/ 150.970s
Frequency - over OF1	64.00Hz/ 300s	63.995Hz/ 299.980s	63.995Hz/ 299.980s	64.010Hz/ 299.980s	63.995Hz/ 299.970s	64.010Hz/ 299.970s
Frequency - over OF2	60.50Hz/ 0.16s	60.510Hz/ 0.127s	60.510Hz/ 0.136s	60.510Hz/ 0.127s	60.510Hz/ 0.124s	60.510Hz/ 0.126s
Frequency - over OF2	62.00Hz/ 5s	62.010Hz/ 4.978s	62.010Hz/ 4.979s	62.010Hz/ 4.966s	62.010Hz/ 4.981s	62.010Hz/ 4.969s
Frequency - over OF2	64.00Hz/ 10s	64.010Hz/ 9.984s	63.993Hz/ 9.978s	64.010Hz/ 9.975s	64.010Hz/ 9.971s	64.010Hz/ 9.978s

Testing Result

5.3	Response to abnormal frequency conditions (60℃)					P
Testing item	Tripping frequency/ Clearing time setting	Measured Tripping frequency/ Clearing time				
		1	2	3	4	5
Frequency - under UF1	56.00Hz/ 2s	55.990Hz/ 1.971s	55.990Hz/ 1.977s	55.990Hz/ 1.976s	56.000Hz/ 1.978s	55.990Hz/ 1.971s
Frequency - under UF1	58.00Hz/ 151s	57.990Hz/ 150.980s	57.990Hz/ 150.970s	57.990Hz/ 150.980s	57.990Hz/ 150.980s	57.990Hz/ 150.970s
Frequency - under UF1	59.50Hz/ 300s	59.490Hz/ 299.980s	59.490Hz/ 299.970s	59.490Hz/ 299.980s	59.490Hz/ 299.980s	59.490Hz/ 299.980s
Frequency - under UF2	56.00Hz/ 0.16s	55.990Hz/ 0.134s	55.990Hz/ 0.133s	55.990Hz/ 0.137s	55.990Hz/ 0.130s	55.990Hz/ 0.135s
Frequency - under UF2	58.00Hz/ 5s	57.990Hz/ 4.986s	57.990Hz/ 4.984s	57.990Hz/ 4.975s	57.990Hz/ 4.985s	57.990Hz/ 4.975s
Frequency - under UF2	59.50Hz/ 10s	59.490Hz/ 9.972s	59.490Hz/ 9.973s	59.490Hz/ 9.966s	59.490Hz/ 9.971s	59.490Hz/ 9.965s
Frequency - over OF1	60.50Hz/ 2s	60.501Hz/ 1.981s	60.508Hz/ 1.974s	60.501Hz/ 1.974s	60.500Hz/ 1.976s	60.508Hz/ 1.972s
Frequency - over OF1	62.00Hz/ 151s	62.010Hz/ 150.970s	62.010Hz/ 150.990s	62.010Hz/ 150.970s	62.010Hz/ 150.980s	62.010Hz/ 150.970s
Frequency - over OF1	64.00Hz/ 300s	64.010Hz/ 299.970s	64.010Hz/ 299.970s	64.010Hz/ 299.970s	64.010Hz/ 299.980s	64.010Hz/ 299.970s
Frequency - over OF2	60.50Hz/ 0.16s	60.500Hz/ 0.125s	60.500Hz/ 0.126s	60.500Hz/ 0.140s	60.500Hz/ 0.135s	60.500Hz/ 0.128s
Frequency - over OF2	62.00Hz/ 5s	62.010Hz/ 4.975s	62.010Hz/ 4.965s	62.010Hz/ 4.969s	62.010Hz/ 4.981s	62.010Hz/ 4.973s
Frequency - over OF2	64.00Hz/ 10s	64.010Hz/ 9.975s	63.993Hz/ 9.967s	64.010Hz/ 9.980s	64.010Hz/ 9.978s	64.010Hz/ 9.970s

Testing Result

5.4.4	Startup current measurement (Method 2)			P
1	2	3	4	5
4.100A 4.679A 4.071A	3.990A 4.603A 3.987A	4.119A 4.743A 3.940A	4.023A 4.688A 3.963A	4.040A 4.742A 3.840A
6	7	8	9	10
4.112A 4.750A 3.910A	4.065A 4.678A 3.985A	3.988A 4.622A 3.967A	4.038A 4.846A 4.076A	4.117A 4.868A 4.031A

5.5.3	Dielectric test	P
Applied points:	Applied voltage:	Breakdown or flashover?
Between Input and output	1485V	No

5.6	DC Injection for inverters without interconnection transformers	P
Rated output load:	80kW	33 % of rated output load:	26.4kW
Output voltage:	127.12V 127.11V 127.10V	Output current (rms)	69.00A 69.09A 69.13A
DC current:	0.111A/0.053% 0.126A/0.060% 0.119A/0.057%	DC current limit	0.5%In
Rated output load:	80kW	66 % of rated output load:	52.8kW
Output voltage:	127.17V 127.15V 127.16V	Output current (rms)	138.38A 138.76A 138.58A
DC current:	0.165A/0.079% 0.166A/0.079% 0.138A/0.066%	DC current limit	0.5%In
Rated output load:	80kW	100 % of rated output load:	80kW
Output voltage:	127.21V 127.20V 127.23V	Output current (rms)	209.44A 210.08A 209.79A
DC current:	0.136A/0.065% 0.157A/0.075% 0.090A/0.043%	DC current limit	0.5%In
Model: SUN2000-80K-MGL0			

Testing Result

5.6	DC Injection for inverters without interconnection transformers		P
Rated output load:	50kW	33 % of rated output load:	16.5kW
Output voltage:	127.10V 127.14V 127.09V	Output current (rms)	43.33A 43.17A 43.33A
DC current:	0.210A/0.160% 0.136A/0.104% 0.269A/0.205%	DC current limit	0.5%In
Rated output load:	50kW	66 % of rated output load:	33.0kW
Output voltage:	127.13V 127.16V 127.12V	Output current (rms)	86.71A 86.47A 86.54A
DC current:	0.213A/0.162% 0.228A/0.174% 0.265A/0.202%	DC current limit	0.5%In
Rated output load:	50kW	100 % of rated output load:	50.0kW
Output voltage:	127.17V 127.18V 127.16V	Output current (rms)	131.32A 131.00A 130.98A
DC current:	0.294A/0.224% 0.230A/0.175% 0.378A/0.288%	DC current limit	0.5%In
Model: SUN2000-50K-MGL0			

Testing Result

5.7.1	Unintentional islanding test			P
Initial State with 100% Load				
	Q (VAR)	**Voltage**	**Watt**	**VA**
R Load	--	127.02V	78.33kW	--
L Load	76.46kVar	127.02V	--	--
C Load	78.77kVar	127.02V	--	--
Islanding Test with 100% Load				
Q(VAR)	**Voltage**	**Watt**	**VA**	**Trip time (ms)**
-5%	127.02V	78.33kW	--	255.00
-4%	127.02V	78.33kW	--	283.65
-3%	127.02V	78.33kW	--	293.65
-2%	127.02V	78.33kW	--	328.65
-1%	127.02V	78.33kW	--	383.65
0%	127.02V	78.33kW	--	545.65
1%	127.02V	78.33kW	--	388.65
2%	127.02V	78.33kW	--	363.65
3%	127.02V	78.33kW	--	328.65
4%	127.02V	78.33kW	--	313.65
5%	127.02V	78.33kW	--	210.00

Islanding Test with 100% Load			
Q(VAR)	**Trip time (ms)**		**Limit**
	the second time	**the third time**	
-1%	378.65	398.65	< 2 s
0%	698.65	678.65	< 2 s
1%	403.65	383.65	< 2 s

Testing Result

5.7.1	Unintentional islanding test			P
Initial State with 66% Load				
	Q (VAR)	**Voltage**	**Watt**	**VA**
R Load	--	126.96V	52.91kW	--
L Load	51.68kVar	126.96V	--	--
C Load	53.22kVar	126.96V	--	--
Islanding Test with 66% Load				
Q(VAR)	**Voltage**	**Watt**	**VA**	**Trip time (ms)**
-5%	126.96V	52.91kW	--	245.00
-4%	126.96V	52.91kW	--	320.00
-3%	126.96V	52.91kW	--	340.00
-2%	126.96V	52.91kW	--	425.00
-1%	126.96V	52.91kW	--	453.65
0%	126.96V	52.91kW	--	595.05
1%	126.96V	52.91kW	--	488.65
2%	126.96V	52.91kW	--	425.00
3%	126.96V	52.91kW	--	345.00
4%	126.96V	52.91kW	--	340.00
5%	126.96V	52.91kW	--	275.00

Islanding Test with 66% Load			
Q(VAR)	**Trip time(ms)**		**Limit**
	the second time	**the third time**	
-1%	433.65	438.65	< 2 s
0%	658.65	658.65	< 2 s
1%	453.65	438.65	< 2 s

Testing Result

5.7.1	Unintentional islanding test			P
Initial State with 33% Load				
	Q (VAR)	**Voltage**	**Watt**	**VA**
R Load	--	126.99V	25.64kW	--
L Load	25.91kVar	126.99V	--	--
C Load	26.63kVar	126.99V	--	--
Islanding Test with 33% Load				
Q(VAR)	**Voltage**	**Watt**	**VA**	**Trip time (ms)**
-5%	126.99V	25.64kW	--	265.00
-4%	126.99V	25.64kW	--	275.00
-3%	126.99V	25.64kW	--	321.15
-2%	126.99V	25.64kW	--	328.65
-1%	126.99V	25.64kW	--	335.00
0%	126.99V	25.64kW	--	380.00
1%	126.99V	25.64kW	--	330.00
2%	126.99V	25.64kW	--	324.55
3%	126.99V	25.64kW	--	313.65
4%	126.99V	25.64kW	--	275.00
5%	126.99V	25.64kW	--	260.00

Islanding Test with 33% Load			
Q(VAR)	**Trip time(ms)**		**Limit**
	the second time	**the third time**	
-1%	350.00	355.00	< 2 s
0%	488.35	598.65	< 2 s
1%	340.00	373.50	< 2 s

Testing Result

5.9	Open phase				P
DC input:	AC output:		Load condition:		Clearing time limit:
415.93V	127.03V		1.30kW		2 sec.
1	2	3	4	5	
250ms	250ms	150ms	250ms	150ms	
L1 disconnected					
DC input:	AC output:		Load condition:		Clearing time limit:
415.96V	127.05V		1.30kW		2 sec.
1	2	3	4	1	
150ms	200ms	200ms	250ms	150ms	
L2 disconnected					
DC input:	AC output:		Load condition:		Clearing time limit:
416.01V	126.99V		1.31kW		2 sec.
1	2	3	4	1	
200ms	250ms	150ms	250ms	150ms	
L3 disconnected					

5.10	Reconnect following abnormal condition disconnect		P
DC input:	AC output:	Load condition:	Re-connect time setting:
348.29V/237.98A/84.14kW	127.87V/211.20A/80.98kW	80.98kW	300s
Overvoltage Verification:			
Overvoltage > 1.10Un	Does the EUT trip? ☑ Yes ☐ No		
Maintain the overvoltage for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $V_{nominal}$	The reconnect time is 305.1		
Step change back to 1.10Un	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		
Undervoltage Verification:			
Undervoltage < 0.88Un	Does the EUT trip? ☑ Yes ☐ No		
Maintain the undervoltage for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $V_{nominal}$	The reconnect time is 304.7		
Step change back to 0.88Un	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		
Overfrequency Verification:			
Overfrequency > 60.5Hz	Does the EUT trip? ☑ Yes ☐ No		
Maintain the frequency for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $F_{nominal}$	The reconnect time is 305.3		
Step change back to 62Hz	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		
Underfrequency Verification:			
Underfrequency < 59.5Hz	Does the EUT trip? ☑ Yes ☐ No		

Testing Result

Maintain the underfrequency for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No
Step change back to the $F_{nominal}$	The reconnect time is 305.6
Step change back to 59.5Hz	Does the EUT reconnect? ☐ Yes ☑ No
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No

Testing Result

5.11	Harmonics test for inverters								P
Load current: 33 %			EUT rated current: 209.97A				DC input: 417.49Vdc; AC output: 127.15Vac AC output current: 69.11 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.1243 0.2066 0.1578	0.0625 0.0431 0.0653	0.0730 0.0497 0.0578	0.0441 0.0406 0.0375	0.0403 0.0403 0.0369	0.0535 0.0508 0.0814	0.0388 0.0418 0.0293	0.0703 0.0747 0.0404	0.1243 0.2066 0.1578
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.0849 0.1035 0.0417	0.1909 0.1448 0.1340	0.1030 0.1047 0.0412	0.1243 0.1768 0.1092	0.0752 0.0742 0.0420	0.0507 0.0553 0.0719	0.0512 0.0539 0.0462	0.1177 0.0894 0.0580	0.0741 0.0723 0.0466	0.0727 0.0515 0.0607
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.0487 0.0690 0.0598	0.0613 0.0623 0.0427	0.0406 0.0509 0.0527	0.0419 0.0403 0.0337	0.0792 0.1504 0.1661	0.0474 0.0405 0.0412	0.0442 0.0507 0.0341	0.0385 0.0397 0.0263	0.1534 0.1352 0.1566	0.0377 0.0375 0.0285
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.0814 0.0784 0.1022	0.0239 0.0265 0.0252	0.0331 0.0304 0.0396	0.0322 0.0359 0.0211	0.1867 0.1367 0.1865	0.0296 0.0329 0.0277	0.0234 0.0457 0.0490	0.0225 0.0235 0.0215	0.0223 0.0528 0.0480	0.0297 0.0263 0.0231
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						0.4906 0.5097 0.4678				
Limit (%)						5				
Model: SUN2000-80K-MGL0										

Testing Result

5.11	Harmonics test for inverters									P
Load current: 66 %			EUT rated current: 209.97A				DC input: 409.17Vdc; AC output: 127.19Vac AC output current: 138.37 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.2209	0.0721	0.0790	0.0905	0.0469	0.0593	0.0471	0.0612	0.0544
		0.2595	0.0713	0.0497	0.0631	0.0592	0.0547	0.0740	0.0796	0.1031
		0.3737	0.0528	0.0884	0.0635	0.0492	0.0758	0.0436	0.0709	0.0997
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.1713	0.1556	0.2704	0.0934	0.0602	0.0446	0.2251	0.1047	0.1381	0.0805
	0.1578	0.0705	0.3154	0.1490	0.0953	0.0990	0.1611	0.0896	0.1695	0.0671
	0.2187	0.0992	0.2900	0.0731	0.1360	0.0974	0.1568	0.0625	0.1362	0.0694
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.0673	0.0686	0.1115	0.0551	0.0488	0.0692	0.1206	0.0347	0.1317	0.0364
	0.1017	0.1303	0.0589	0.0690	0.1238	0.0430	0.0802	0.0479	0.1172	0.0693
	0.1188	0.0937	0.1194	0.0533	0.1129	0.0714	0.0864	0.0501	0.1511	0.0495
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.0574	0.0361	0.0995	0.0338	0.1745	0.0410	0.0592	0.0412	0.0422	0.0470
	0.0830	0.0411	0.0460	0.0378	0.1260	0.0516	0.0704	0.0473	0.0441	0.0377
	0.0819	0.0538	0.0752	0.0316	0.2091	0.0330	0.1026	0.0308	0.0497	0.0336
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						0.6892 0.6831 0.7586				
Limit (%)						5				
Model: SUN2000-80K-MGL0										

Testing Result

5.11	Harmonics test for inverters									P
Load current: 100 %			EUT rated current: 209.97A				DC input: 393.33Vdc; AC output: 127.20Vac AC output current: 209.20 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.6366	0.0996	0.1158	0.1627	0.0558	0.0433	0.0575	0.1058	0.0969
		0.3505	0.1052	0.0700	0.1176	0.0836	0.1065	0.0912	0.0614	0.0801
		0.5495	0.0785	0.1006	0.1404	0.0568	0.1035	0.0567	0.1135	0.1196
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.0521	0.0822	0.3447	0.1117	0.1053	0.1157	0.1772	0.1283	0.4785	0.1342
	0.0504	0.0612	0.3898	0.1869	0.1181	0.1165	0.0684	0.0786	0.4114	0.1620
	0.0510	0.0904	0.3623	0.1197	0.2095	0.0819	0.1486	0.0986	0.3836	0.0803
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.1767	0.0845	0.2031	0.1372	0.3328	0.0797	0.0606	0.0659	0.1356	0.0700
	0.0865	0.1308	0.1177	0.0738	0.1838	0.0689	0.1131	0.0913	0.1168	0.0608
	0.1266	0.1120	0.2071	0.1346	0.2599	0.0738	0.0974	0.0532	0.0564	0.0420
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.1748	0.0469	0.0936	0.0436	0.0941	0.0509	0.0658	0.0632	0.0726	0.0403
	0.0962	0.0539	0.1195	0.0519	0.0926	0.0519	0.0657	0.0792	0.1183	0.0399
	0.1449	0.0617	0.1347	0.0340	0.0584	0.0375	0.0571	0.0393	0.1100	0.0274
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)							1.1228 0.8967 1.0105			
Limit (%)							5			
Model: SUN2000-80K-MGL0										

Testing Result

5.11	Harmonics test for inverters									P
Load current: 33 %			EUT rated current: 131.23A				DC input: 417.53Vdc; AC output: 127.14Vac AC output current: 43.15 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.1682 0.2225 0.1588	0.0754 0.0625 0.0878	0.0726 0.0668 0.0857	0.0629 0.0707 0.0694	0.0764 0.0649 0.0845	0.0924 0.0768 0.1007	0.0504 0.0526 0.0586	0.0591 0.0675 0.0820	0.1073 0.1147 0.0718
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.2901 0.2621 0.1490	0.1773 0.1589 0.0819	0.1971 0.2221 0.1217	0.0941 0.1060 0.0825	0.0819 0.0906 0.1043	0.0892 0.1055 0.0920	0.1352 0.1392 0.1256	0.0900 0.0959 0.1043	0.1106 0.0927 0.1071	0.0911 0.0862 0.1018
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.0778 0.0969 0.1072	0.0735 0.0762 0.0883	0.0843 0.0786 0.1167	0.0801 0.0847 0.0782	0.1725 0.2754 0.1821	0.0643 0.0626 0.0732	0.0634 0.0670 0.0867	0.0631 0.0580 0.0564	0.2661 0.2086 0.2234	0.0643 0.0606 0.0514
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.1302 0.1237 0.1113	0.0466 0.0516 0.0546	0.0436 0.0973 0.0998	0.0411 0.0503 0.0420	0.2835 0.2559 0.2419	0.0405 0.0453 0.0439	0.0763 0.0492 0.0646	0.0516 0.0485 0.0432	0.0658 0.0937 0.0733	0.0383 0.0420 0.0391
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						0.4680 0.4793 0.4133				
Limit (%)						5				
Model: SUN2000-50K-MGL0										

Testing Result

5.11	Harmonics test for inverters									P
Load current: 66 %			EUT rated current: 131.23A				DC input: 409.33Vdc; AC output: 127.16Vac AC output current: 86.41 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.1524 0.3484 0.3385	0.0835 0.0651 0.0833	0.1210 0.0844 0.0851	0.0872 0.0813 0.0775	0.0733 0.0799 0.0759	0.0925 0.0950 0.1351	0.0713 0.0620 0.0713	0.0790 0.1112 0.0789	0.1361 0.1881 0.0820
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.3000 0.2680 0.2276	0.2391 0.1552 0.1362	0.2806 0.3824 0.2818	0.1202 0.2178 0.1298	0.1121 0.0974 0.1113	0.0967 0.0897 0.0786	0.1637 0.1814 0.1462	0.1006 0.1108 0.0941	0.1361 0.1130 0.1052	0.1018 0.0967 0.1014
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.0910 0.1283 0.1165	0.0978 0.1048 0.0910	0.0811 0.1006 0.0926	0.0757 0.0921 0.0933	0.1321 0.1952 0.2083	0.0807 0.0667 0.1083	0.1009 0.1215 0.1693	0.0615 0.0720 0.0615	0.1714 0.1439 0.2079	0.0505 0.0508 0.0537
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.1181 0.1643 0.2093	0.0465 0.0654 0.0877	0.0563 0.0769 0.0974	0.0546 0.0524 0.0435	0.2666 0.2701 0.3382	0.0411 0.0401 0.0439	0.1004 0.0966 0.1205	0.0581 0.0584 0.0582	0.0540 0.0715 0.0692	0.0564 0.0480 0.0446
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						0.4995 0.5753 0.5556				
Limit (%)						5				
Model: SUN2000-50K-MGL0										

Testing Result

5.11	Harmonics test for inverters									P
Load current: 100 %			EUT rated current: 131.23A				DC input: 393.75Vdc; AC output: 127.18Vac AC output current: 131.06 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.3003	0.1018	0.1296	0.1359	0.0841	0.1029	0.0534	0.0483	0.0841
		0.3394	0.0908	0.0885	0.1155	0.0712	0.0889	0.0850	0.0685	0.0821
		0.5223	0.0699	0.0926	0.1079	0.0625	0.1066	0.0619	0.0598	0.0676
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.1227	0.2256	0.4684	0.1008	0.0748	0.0731	0.1982	0.2384	0.4191	0.1612
	0.1627	0.1364	0.5234	0.2230	0.1278	0.0986	0.2224	0.1909	0.3414	0.1868
	0.1255	0.1090	0.4428	0.1569	0.1524	0.1029	0.1958	0.1291	0.2678	0.1003
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.1001	0.1083	0.1488	0.1363	0.1515	0.0893	0.1010	0.0786	0.0706	0.0493
	0.0867	0.1469	0.1142	0.1425	0.1331	0.0790	0.1802	0.0899	0.0714	0.0595
	0.1128	0.1042	0.1880	0.0727	0.1113	0.1022	0.1418	0.0584	0.0594	0.0679
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.0493	0.0587	0.0714	0.0358	0.0743	0.0377	0.0719	0.0677	0.0730	0.0554
	0.0672	0.0726	0.1412	0.0554	0.1374	0.0514	0.0712	0.0636	0.0870	0.0405
	0.0569	0.0660	0.0952	0.0557	0.1317	0.0502	0.0638	0.0764	0.0474	0.0641
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						0.6009 0.6302 0.5990				
Limit (%)						5				
Model: SUN2000-50K-MGL0										

Overview

Left view

Top view

Bottom view

Appendix 1: Photos

Terminal view

Back view

Internal view-1

Internal view-2

(End of Report)