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Invoice No.: SGI/ANU/START-UP/ AI HY PROCESSOR -PATENT-08/2026

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SATURDAY, MARCH 28, 2026
Our Ref.: **ANU/AI CPP SYSTEM -PATENT-05/2026**

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Description	**Fee. (INR)**
1. Professional fee towards providing general advisory on different intellectual property rights to start ups, providing information on protecting and promoting IPR to start ups in other countries, drafting Complete Specification and preparing and filing other documents such as Form-1, Form-2, Form-3, Form-9 and Form 18A, reporting to client the filing of the Patent Application No. **202631038691** dated **28th MARCH 2026.**	NIL
2. Government Fee for filing the Patent Application.	INR 18,020/--
3. Miscellaneous expenses including charges for typing, phone, Print outs, photocopy, stamp fee, postal charges, conveyance etc.	INR 1000/-
Total	**INR 19,020/- (excluding taxes)**
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Sr. No.	App. Number	Ref. No./Application No.	Amount Paid	C.B.R. No.	Form Name	Remarks
1	E-106/1942/2026/KOL	202631038691	0	-----	FORM28	
2	202631038691	TEMP/E-1/42452/2026-KOL	7520	4698	FORM 1	ARTIFICIAL SUPER INTELLIGENCE-BASED NEUROMORPHIC HYPERSONIC PROCESSOR

TransactionID	Payment Mode	Challan Identification Number	Amount Paid	Head of A/C No
N-0001910131	Online Bank Transfer	2803260046657	7520.00	1475001020000001

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1	E20263022084	202631038691	8000	4711	FORM 18A	

TransactionID	Payment Mode	Challan Identification Number	Amount Paid	Head of A/C No
N-0001910412	Online Bank Transfer	2903260007904	8000.00	1475001020000001

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1	E-12/768/2026/KOL	202631038691	2500	4709	FORM 9	

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(57) Abstract :
The present invention discloses a neuromorphic processor system (100) for deterministic real-time processing of input data with bounded latency and its method. The system comprises sensor interface circuits (102), an event encoder module (104), neuromorphic compute cores (NCCs) (106), a hypersonic event fabric (HEF) (108), a deterministic scheduling controller (110), an adaptive learning engine (112), a context management and task coordination controller (114), and an output interface circuit (118). The sensor interface circuits (102) is configured to receive multi-modal input signals. The event encoder module (104) is configured to convert the input signals into time-encoded spike event streams. The HEF (108) is configured to: transmit event packets between the NCCs, and perform priority-aware routing and congestion controlled communication to ensure bounded end-to-end latency. The deterministic scheduling controller (110) is configured to assign priority levels to event streams and regulate routing and processing across the hypersonic event fabric based on latency constraints.

No. of Pages : 57 No. of Claims : 15

FORM 2

THE PATENTS ACT, 1970

[39 of 1970]

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THE PATENTS RULES, 2003

COMPLETE SPECIFICATION

(Section 10; Rule 13)

ARTIFICIAL SUPER INTELLIGENCE-BASED NEUROMORPHIC HYPERSONIC PROCESSOR

SRJX RESEARCH AND INNOVATION LAB LLP

PLOT NO-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR,

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An Indian Company

The following Specification particularly describes the invention and the manner in which it is to be performed.

FIELD OF INVENTION

The present invention relates generally to the field of hypersonic processor. More particularly relates to an Artificial Super Intelligence (ASI)–based neuromorphic hypersonic processor. Additionally, the present invention relates a neuromorphic processor system for deterministic real-time processing of input data with bounded latency.

BACKGROUND

Modern intelligent systems are rapidly expanding from cloud data centers into real-world, safety-critical environments such as autonomous vehicles, industrial robotics, spacecraft, secure communication networks, and real-time decision platforms. These applications demand extremely fast perception-to-action cycles, continuous adaptation, and dependable operation under uncertain and dynamic conditions. At the same time, the volume, velocity, and variety of data generated by sensors (vision, radar, LiDAR, biomedical, telemetry, and cyber-signals) are growing dramatically. Conventional compute stacks often struggle to deliver both high intelligence and ultra-low latency within practical power, thermal, and size constraints, particularly when intelligence must be deployed at the edge rather than in a remote cloud.

Current AI acceleration is dominated by von-Neumann architectures and GPU/TPU-style parallel processors. While these platforms provide high throughput for batch inference and training, they are typically power-hungry, memory-bandwidth limited, and less efficient for sparse, event-driven, or continuously streaming workloads. The separation of memory and compute introduces a “data movement” bottleneck, where energy and time are consumed transferring activations and weights between compute units and memory hierarchies. As model sizes and real-time requirements increase, these limitations can cause unacceptable latency, elevated operating cost, and reduced reliability in embedded or mission-critical deployments, especially where thermal dissipation and battery capacity are constrained.

Neuromorphic computing has emerged as a promising alternative, inspired by biological nervous systems. Neuromorphic processors commonly employ spiking neural networks, event-driven communication, and local memory-compute co-location to reduce redundant operations and to process information only when meaningful changes occur. Such systems can offer superior energy efficiency for temporal pattern recognition, sensor fusion, and adaptive control. However, existing neuromorphic solutions still face major challenges including limited programmability, constrained on-chip learning flexibility, difficulty scaling to large networks, timing unpredictability across large interconnects, restricted precision control, and limited support for safe, verifiable, and secure continuous learning in real-world conditions.

Furthermore, a growing class of applications requires hypersonic processing in the sense of ultra-fast, deterministic, low-latency intelligence pipelines—where microsecond-level responses, rapid event routing, and high-rate sensor ingestion are essential. Current processors often rely on synchronous clocking and centralized scheduling that can introduce variable latency under load. Many neuromorphic platforms, while efficient, may lack sufficiently high-speed event fabrics, robust fault tolerance, and deterministic real-time guarantees needed for time-critical control loops and high-velocity sensor streams. In addition, as systems become more autonomous, there is a need for architectures that support higher-order reasoning, rapid context formation, and long-horizon decision consistency without sacrificing energy efficiency.

Accordingly, there exists a need for an advanced computing architecture that merges neuromorphic, event-driven computation with hypersonic-grade real-time performance, while supporting scalable learning and reliable deployment. Such an architecture should address the shortcomings of prior art by reducing memory-compute data movement, enabling ultra-low-latency spike/event routing, supporting continuous adaptation with bounded risk, and incorporating resilient operation under thermal,

power, and environmental stresses. The background motivation of the present invention is therefore to provide a processor framework capable of delivering next-generation intelligence performance—aimed toward Artificial Super Intelligence–grade capabilities—through a practical, energy-efficient, and high-speed neuromorphic processing substrate suitable for industrial and mission-critical use.

Therefore, there is a need for a neuromorphic processor system for deterministic real-time processing of input data with bounded latency to overcome the above mentioned drawbacks.

OBJECTS OF THE INVENTION

According to embodiments of the present invention, the key objectives are given below:

1. To provide an ASI-oriented neuromorphic processor architecture capable of supporting advanced intelligence functions (perception, reasoning, planning, and adaptation) on a single scalable hardware platform.
2. To achieve hypersonic-grade ultra-low latency processing for real-time decision-making by using event-driven computation and deterministic event routing.
3. To minimize the von-Neumann memory–compute bottleneck by co-locating computation with synaptic memory and reducing unnecessary data movement.
4. To enable high-speed event/spike communication across multiple neuromorphic cores using a priority-aware, congestion-controlled interconnect with bounded latency.
5. To support continuous on-chip learning and adaptation through local plasticity and hybrid learning mechanisms without requiring frequent cloud retraining.
6. To ensure safe and stable learning by enforcing bounded-update policies, validation checkpoints, drift monitoring, and rollback mechanisms.
7. To deliver high energy efficiency and reduced thermal footprint suitable for edge devices, embedded systems, and constrained environments.

8. To provide multi-modal sensor fusion capability (e.g., radar, vision, LiDAR, telemetry, biomedical, cyber-signals) using event-driven encoding and spiking inference.
9. To incorporate fault tolerance and resilience through redundancy, error correction, self-diagnostics, and robust operation under temperature/radiation/aging variations.
10. To enhance security and trustworthiness via secure boot, encrypted event channels, tamper detection, and hardware-level isolation of critical tasks.
11. To support scalable deployment and programmability across different applications by modular cores, configurable neuron/synapse models, and flexible scheduling.
12. To enable real-time verification and control safeguards by integrating confidence estimation, policy checks, and safety-gated actuation for mission-critical outputs.

SUMMARY OF THE INVENTION

The present invention relates to an Artificial Super Intelligence (ASI)–based Neuromorphic Hypersonic Processor, a next-generation computing architecture designed to deliver ultra-low-latency ("hypersonic") intelligence with high energy efficiency, continuous adaptation, and robust real-time reliability. The invention integrates brain-inspired neuromorphic computation with high-speed event routing, deterministic scheduling, and safety-aware learning to overcome the limitations of conventional von-Neumann processors and current neuromorphic chips, particularly in edge and mission-critical deployments where power, heat, and response time are constrained.

In one embodiment, the processor employs an event-driven spiking compute fabric composed of multiple neuromorphic cores arranged in a scalable mesh. Each core includes neuron-synapse arrays, local memory, and an event interface that processes input spikes/events asynchronously. Instead of processing every clock cycle,

computation is activated only by meaningful input events, thereby reducing redundant operations and minimizing data movement. The invention supports hybrid compute modes, enabling both spike-based inference and selective high-precision numerical operations when required, allowing efficient handling of mixed workloads such as sensor fusion, reasoning, anomaly detection, and control.

A key unique feature of the present invention is a Hypersonic Event Fabric (HEF) that routes events with bounded latency across cores using priority-aware, congestion-controlled communication. The HEF supports deterministic timing through time-stamped spikes, deadline tagging, and guaranteed service pathways for critical tasks. This ensures predictable response under heavy load, enabling real-time applications such as autonomous navigation, aerospace guidance, industrial automation, and cybersecurity operations. The fabric can dynamically allocate routing bandwidth based on event intensity, maintaining stable performance even when sensor activity spikes suddenly.

In another embodiment, the processor incorporates an Adaptive Synaptic Intelligence Layer that supports on-chip learning through a combination of local plasticity rules and supervised/unsupervised update schemes. The system performs continuous adaptation while enforcing safety constraints using a bounded-learning policy: learning updates are allowed only within pre-defined stability limits. Learning parameters can be versioned, validated, and rolled back if drift or instability is detected. This enables the processor to learn from live environments without risking catastrophic model corruption, providing a practical pathway for long-term deployment in changing conditions.

The present invention also includes an ASI Orchestration Engine that coordinates multiple reasoning and control modules across the neuromorphic fabric. This orchestration layer manages hierarchical goals, context windows, memory consolidation, and multi-modal fusion, allowing the processor to support higher-level

intelligent behavior beyond simple pattern recognition. The orchestration engine schedules tasks based on urgency, energy budget, and confidence estimates, and may invoke a verification pipeline before executing safety-critical outputs. This enables the architecture to function as an intelligent autonomy processor capable of fast decision-making while maintaining operational safeguards.

In some implementations, the processor provides a multi-level memory hierarchy optimized for event-driven intelligence. It includes local synaptic memory for immediate inference, fast on-chip associative memory for short-term context, and non-volatile retention memory for long-term patterns and policies. Memory reads and writes are minimized through sparse activation and local learning, substantially reducing energy consumption compared to conventional architectures. Additionally, memory integrity checks, error correction, and redundant routing paths improve fault tolerance and resilience against radiation, temperature variation, and aging effects.

To support deployment in secure environments, the present invention may include a Trusted Neuromorphic Security Module that provides encrypted event channels, secure boot, hardware-based identity, and tamper-aware logging. This module can also detect adversarial event patterns, spoofed sensor spikes, or abnormal learning updates. Security policies can be enforced at the hardware scheduling level, ensuring that sensitive tasks receive isolated compute and protected memory access, while untrusted inputs are sandboxed or filtered through anomaly detectors.

The present invention provides a neuromorphic processor system that combines event-driven spiking computation, hypersonic deterministic event routing, safe continuous learning, and high-level orchestration to deliver a practical hardware foundation for next-generation intelligent systems. It improves upon prior art by reducing the memory-compute bottleneck, enabling guaranteed low-latency responses, supporting adaptive intelligence at the edge, and ensuring resilience, security, and stability in real-world deployments. This architecture is particularly suited for applications requiring

fast, energy-efficient, and dependable intelligence under dynamic operational conditions.

An embodiment of the present invention describes a neuromorphic processor system for deterministic real-time processing of input data with bounded latency. The system comprises one or more sensor interface circuits configured to receive multi-modal input signals; an event encoder module implemented using hardware logic and operatively coupled to the sensor interface circuits, the event encoder module being configured to convert the input signals into time-encoded spike event streams; a plurality of neuromorphic compute cores (NCCs) arranged in a scalable interconnect, each neuromorphic compute core comprising: neuron processing circuits configured to process spike events, synapse circuits storing programmable synaptic weights, and local memory storing neuron state variables and routing information; a hypersonic event fabric (HEF) comprising a hardware interconnect network coupling the plurality of neuromorphic compute cores, the hypersonic event fabric being configured to: transmit event packets between the neuromorphic compute cores, each event packet comprising timestamp, priority level, and deadline metadata, and perform priority-aware routing and congestion-controlled communication to ensure bounded end-to-end latency; a deterministic scheduling controller implemented in hardware and configured to assign priority levels to event streams and regulate routing and processing across the hypersonic event fabric based on latency constraints; an adaptive learning engine implemented using hardware logic and configured to update synaptic weights within predefined bounded limits and to restore previously stored weight states upon detection of drift conditions; a context management and task coordination controller implemented in hardware and configured to aggregate outputs from the plurality of neuromorphic compute cores and generate one or more control decisions based on contextual data; and an output interface circuit configured to generate control signals for an external system; wherein the neuromorphic processor system is configured to process the spike event streams through a processing pipeline comprising: (i) event

encoding by the event encoder module, (ii) bounded-latency routing via the hypersonic event fabric, (iii) event-driven neuromorphic computation in the plurality of neuromorphic compute cores, (iv) contextual data aggregation by the context management and task coordination controller, and (v) generation of control outputs via the output interface circuit; thereby achieving reduced memory-to-compute data transfer, improved energy efficiency, and deterministic worst-case response time.

According an embodiment of the present invention, the hypersonic event fabric is further configured to assign deadline tags and guaranteed-service routing channels to event packets associated with safety-critical operations, thereby ensuring delivery within a predefined latency bound.

According another embodiment of the present invention, each neuromorphic compute core is configured to operate in an event-triggered asynchronous mode, such that computation is performed only upon receipt of spike events.

According to yet another embodiment of the present invention, the adaptive learning engine is configured to enforce bounded update constraints on synaptic weights based on magnitude and rate thresholds and to perform rollback using stored model snapshots upon detection of instability or drift.

According to yet another embodiment of the present invention, a hierarchical memory system including: (i) local synaptic memory within each neuromorphic compute core, (ii) associative memory configured to store contextual data, and (iii) non-volatile memory storing validated model parameters.

According to yet another embodiment of the present invention, the context management and task coordination controller is further configured to perform priority-based arbitration of multiple event streams and to initiate a verification operation prior

to generation of control outputs when a confidence parameter falls below a predefined threshold.

According to yet another embodiment of the present invention, a hybrid precision computation module implemented in hardware, configured to selectively execute high-precision numerical operations for verification, calibration, or normalization tasks while maintaining primary event-driven computation in the neuromorphic compute cores.

According to yet another embodiment of the present invention, a security and integrity module implemented in hardware, configured to: perform secure boot operations, encrypt event packets transmitted through the hypersonic event fabric, and detect anomalous event patterns indicative of unauthorized or adversarial inputs.

According to yet another embodiment of the present invention, the deterministic scheduling controller is further configured to implement rate limiting and adaptive throttling for non-critical event streams to preserve latency guarantees for high-priority event streams.

According to yet another embodiment of the present invention, the hypersonic event fabric and the plurality of neuromorphic compute cores are configured to provide fault tolerance by isolating malfunctioning compute cores and rerouting event packets through redundant communication paths.

Another embodiment of the present invention describes a method for deterministic real-time processing of input data with bounded latency using a neuromorphic processor system. The method comprises receiving, by one or more sensor interface circuits, multi-modal input signals; converting, by an event encoder module implemented using hardware logic, the multi-modal input signals into time-encoded spike event streams; routing, by a hypersonic event fabric (HEF) comprising a hardware interconnect network, the spike event streams as event packets between a plurality of neuromorphic

compute cores (NCCs), each event packet comprising timestamp, priority level, and deadline metadata, wherein the routing includes priority-aware and congestion-controlled communication to ensure bounded latency; processing, by the plurality of neuromorphic compute cores, the spike event streams using event-driven neuromorphic computation including neuron processing circuits and synapse circuits; assigning and regulating, by a deterministic scheduling controller implemented in hardware, priority levels for the spike event streams based on latency constraints; updating, by an adaptive learning engine implemented using hardware logic, synaptic weights within predefined bounded limits and restoring previously stored weight states upon detection of drift conditions; aggregating, by a context management and task coordination controller implemented in hardware, outputs generated by the plurality of neuromorphic compute cores to form contextual data and generate one or more control decisions; and generating, by an output interface circuit, control signals for an external system; wherein the method processes the spike event streams through a pipeline comprising event encoding, bounded-latency routing, event-driven computation, contextual aggregation, and output generation, thereby achieving reduced memory-to-compute data transfer, improved energy efficiency, and deterministic worst-case response time.

According to another embodiment of the present invention, the method of routing by the hypersonic event fabric further comprises assigning deadline tags and guaranteed-service routing channels to event packets associated with safety-critical operations, thereby ensuring delivery within a predefined latency bound.

According to yet another embodiment of the present invention, the method of processing by the plurality of neuromorphic compute cores comprises performing computation in an event-triggered asynchronous manner, such that processing is performed only upon receipt of spike events.

According to yet another embodiment of the present invention, the method of updating synaptic weights further comprises enforcing bounded update constraints based on

magnitude and rate thresholds and performing rollback using stored model snapshots upon detection of instability or drift.

According to yet another embodiment of the present invention, the method further comprises selectively executing, by a hybrid precision computation module implemented in hardware, high-precision numerical operations for verification, calibration, or normalization tasks.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

This invention is described by way of example with reference to the following drawings. These drawings being referred herein are for the purpose of illustrating preferred embodiments of the invention only, and not for the purpose of limiting the same.

FIG. 1 illustrates a block diagram of a neuromorphic processor system for deterministic real-time processing of input data with bounded latency, according to an embodiment of the present invention.

FIG. 2 illustrates a flow chart of method for deterministic real-time processing of input data with bounded latency using a neuromorphic processor system, according to an embodiment of the present invention.

FIG. 3 illustrates an Artificial Super Intelligence (ASI)-based Neuromorphic Hypersonic Processor Architecture, according to an embodiment of the present invention.

FIG. 4 illustractes a logic layer of an Artificial Super Intelligence (ASI)-based Neuromorphic Hypersonic Processor Architecture, according to an embodiment of the present invention.

FIG. 5 illustractes a flow chart of method for deterministic real-time processing of input data with bounded latency using a neuromorphic processor system, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The present invention is described hereinafter by various embodiments with reference to the accompanying drawings, wherein reference numerals used in the accompanying drawings correspond to the like elements throughout the description. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, the embodiments are provided so that this disclosure will be thorough and complete and will fully convey the scope of the invention to those skilled in the art.

It will be understood by those skilled in the art that the foregoing general description and the following detailed description are exemplary and explanatory of the invention and are not intended to be restrictive thereof. The terms "comprises", "comprising", or any other variations thereof, are intended to cover a non-exclusive inclusion, Appearances of the phrase "in an embodiment", "in another embodiment" and similar language throughout this specification may, but not necessarily do, all refer to the same embodiment.

Further, the words "a" or "an" mean "at least one" and the word "plurality" means "one or more" unless otherwise mentioned. Furthermore, the terminology and phraseology used herein is solely used for descriptive purposes and should not be construed as limiting in scope. The systems, methods, and examples provided herein are only illustrative and not intended to be limiting.

The present invention discloses an Artificial Super Intelligence (ASI)–Based Neuromorphic Hypersonic Processor that introduces multiple technical advancement over conventional neuromorphic chips and AI accelerators. The uniqueness lies not in merely combining "ASI" and "neuromorphic computing," but in providing a hardware–algorithm co-designed processor that guarantees bounded latency, supports safety-bounded continual learning, and enables hierarchical intelligence orchestration

under strict energy and reliability constraints. The present invention is engineered for real-time autonomy where inference, adaptation, and control must occur in tightly bounded time windows, even under fluctuating event loads.

A primary unique aspect is a Hypersonic Event Fabric (HEF) that enables deterministic, deadline-aware spike/event routing across a multi-core neuromorphic mesh. Unlike typical asynchronous event buses that may suffer congestion and unpredictable delays, the HEF attaches timestamps, priorities, and deadlines to events and routes them using congestion-aware arbitration with guaranteed-service channels for safety-critical flows. This ensures that key decision loops (e.g., collision avoidance, hazard detection, emergency braking, alarm triggers) have a predictable worst-case response time. The HEF further supports dynamic bandwidth allocation based on event density, preserving low latency during bursts of sensor activity without starving background tasks.

Another unique aspect is the invention's Safety-Bounded Continual Learning Framework implemented at hardware level. Prior systems often either (a) avoid on-chip learning entirely, or (b) allow limited fine-tuning without robust safeguards. In contrast, the present invention introduces a learning guardrail mechanism where synaptic updates are permitted only within predefined stability limits. Each learning window is validated using on-chip drift metrics and confidence scoring. If instability is detected, the processor can perform instant rollback to a last-known-good parameter state. This ensures that the processor can adapt continuously in real-world environments while preventing catastrophic forgetting, adversarial drift, or runaway weight changes that could lead to unsafe outputs.

The present invention also introduces a Hybrid Precision Neuromorphic Compute Pipeline that bridges event-driven spiking computation with selective high-precision arithmetic only when required. Neuromorphic chips often trade numerical precision for efficiency, while conventional AI accelerators consume excessive power for always-on high-precision compute. The disclosed processor uses spike-based sparse operations

for most workloads, but can invoke a controlled mixed-precision path for tasks requiring numerical stability (e.g., calibration, sensor fusion normalization, cryptographic checks, safety verification math). This hybrid compute model is orchestrated by latency and energy budgets, enabling high accuracy without sacrificing real-time responsiveness.

A further unique contribution is an ASI Orchestration Engine embedded into the processor architecture. This engine manages hierarchical goals, contextual memory, multi-module collaboration, and real-time arbitration between perception, reasoning, and actuation. Unlike typical neuromorphic chips that primarily accelerate pattern recognition, the disclosed invention supports a layered intelligence workflow: fast sensory event parsing at the edge, mid-level context formation via associative memory, and higher-level decision policies coordinated through the orchestration engine. This enables more general intelligent behavior—suitable for complex day-to-day autonomy—while still operating under deterministic timing control.

The processor additionally includes a multi-tier memory hierarchy optimized for spiking intelligence, which constitutes another novel aspect. It combines (i) local synaptic memory for immediate event inference, (ii) fast associative memory for short-term context and retrieval, and (iii) persistent retention memory for stable long-term behavior policies and safety rules. Importantly, the memory system supports version control of learned parameters, enabling secure updates, auditability, and rollback. This transforms the processor into not just a compute engine, but a self-maintaining intelligent system with lifecycle management for deployed learning.

Another unique aspect is the invention's resilience and trust-by-design hardware, intended for real-world reliability. The processor supports fault detection, error correction, redundant routing paths, and self-diagnostics that operate continuously. It can isolate malfunctioning cores, reroute event traffic, and maintain safe degraded operation rather than failing abruptly. Additionally, a trusted security subsystem can

enable secure boot, encrypted event channels, tamper-aware logging, and adversarial pattern detection to protect the learning pipeline and prevent manipulation of spiking inputs or synaptic updates.

The uniqueness of the present invention lies in the integrated combination of: (1) deterministic hypersonic event routing with bounded latency, (2) safety-bounded continual learning with validation and rollback, (3) hybrid precision neuromorphic computation, (4) embedded ASI orchestration for hierarchical intelligence, (5) context-optimized memory hierarchy with versioned learning, and (6) resilience and security mechanisms at hardware level. Together, these aspects provide a unique processor architecture capable of delivering high-speed, adaptive, energy-efficient intelligence suitable for everyday and mission-critical applications, while overcoming fundamental limitations of prior neuromorphic and AI accelerator systems.

FIG. 1 illustrates a block diagram of a neuromorphic processor system for deterministic real-time processing of input data with bounded latency, according to an embodiment of the present invention. The neuromorphic processor system (100) is configured for deterministic real-time processing of input data with bounded latency. The system (100) comprises a plurality of interconnected hardware components arranged to implement an event-driven processing pipeline with deterministic scheduling and safety-bounded adaptive learning.

The system (100) includes one or more sensor interface circuits (102) configured to receive multi-modal input signals. The multi-modal input signals includes, but are not limited to, vision data, radar signals, LiDAR data, biomedical signals, telemetry inputs, and cyber-event streams. The sensor interface circuits (102) includes analog-to-digital conversion units, signal conditioning circuits, and buffering elements for preparing the input signals for further processing.

The sensor interface circuits (102) are operatively coupled to an event encoder module (104) implemented using hardware logic. The event encoder module (104) converts the received input signals into time-encoded spike event streams, wherein events are generated based on temporal changes, threshold crossings, or feature extraction from the input signals. The encoding includes time-based encoding, delta encoding, or event-triggered encoding, thereby reducing redundant processing and minimizing data transfer.

The generated spike event streams are transmitted to a hypersonic event fabric (HEF) (108), which comprises a hardware interconnect network configured to route event packets between processing elements. In one embodiment, the hypersonic event fabric (108) is implemented as a network-on-chip (NoC) architecture comprising routing logic, arbitration units, communication links, and buffer memories. Each event packet includes metadata such as timestamp, priority level, and deadline information.

The routing logic is configured to determine a transmission path based on routing tables stored in a local memory, while the arbitration units are configured to select between competing event packets using priority-based scheduling implemented through hardware priority queues. Buffer memories are configured to temporarily store event packets and to support flow control mechanisms including backpressure signaling to prevent congestion.

The hypersonic event fabric (HEF) (108) performs priority-aware routing and congestion-controlled communication by allocating transmission bandwidth based on priority levels and deadline constraints associated with the event packets. In one embodiment, guaranteed-service channels are implemented using reserved bandwidth paths and dedicated buffer resources for high-priority event streams, thereby ensuring deterministic routing and bounded end-to-end latency for event delivery, including under high traffic conditions. In one embodiment, the hypersonic event fabric is configured to assign deadline tags and guaranteed-service routing channels to event

packets associated with safety-critical operations, thereby ensuring delivery within a predefined latency bound.

In one embodiment, the routing logic, arbitration units, and buffer memories are implemented as digital hardware circuits including combinational and sequential logic elements.

The plurality of neuromorphic compute cores (NCCs) (106) are operatively coupled to the hypersonic event fabric (HEF) (108). Each neuromorphic compute core (106) comprises neuron processing circuits (120), synapse circuits (122), and a local memory (124). The neuron processing circuits (120) include integrate-and-fire neuron circuits, adaptive spiking neuron circuits, or equivalent hardware neuron models configured to process incoming spike events, wherein neuron state variables are updated using hardware registers and accumulation circuits based on received spike inputs. In one embodiment, each neuromorphic compute core is configured to operate in an event-triggered asynchronous mode, such that computation is performed only upon receipt of spike events.

The synapse circuits (122) store programmable synaptic weights and are configured to apply the synaptic weights to incoming spike events using hardware multiply-accumulate units or equivalent signal scaling circuits, thereby generating weighted neuron inputs. The local memory (124) stores neuron state variables, routing information, and intermediate computation data, and may include static random-access memory (SRAM) or equivalent on-chip memory structures to reduce data movement and improve processing efficiency.

In one embodiment, the context management and task coordination controller is configured to perform priority-based arbitration of multiple event streams and to initiate a verification operation prior to generation of control outputs when a confidence parameter falls below a predefined threshold.

In one embodiment, the neuromorphic processor system (100) further comprises a hierarchical memory architecture including the local memory (124) within each neuromorphic compute core (106), associative memory configured to store contextual data used by the context management and task coordination controller (114), and non-volatile memory configured to store validated synaptic weight states and model parameters. The associative memory may be implemented using content-addressable memory (CAM) or equivalent hardware structures to enable efficient retrieval of contextual information based on input patterns. The non-volatile memory may include flash memory, resistive memory, or other persistent storage technologies configured to retain model parameters across power cycles. This hierarchical memory organization reduces external memory access, improves data locality, and supports efficient contextual processing and model persistence.

In one embodiment, the neuromorphic compute cores (106) operate in an event-triggered asynchronous manner, wherein incoming spike events are detected using event detection circuits and trigger neuron state updates and synaptic computations without requiring global clock-driven execution, thereby reducing power consumption and redundant processing.

In one embodiment, the neuron processing circuits (120) and the synapse circuits (122) are implemented using digital hardware logic including combinational and sequential circuits configured to perform the aforementioned operations.

The deterministic scheduling controller (110) is operatively coupled to the hypersonic event fabric (108) and the neuromorphic compute cores (106). The deterministic scheduling controller (110) is implemented in hardware and comprises priority assignment logic, scheduling units, queue management circuits, and control registers. The controller (110) is configured to assign priority levels to event streams based on predefined latency constraints, priority parameters, and system load conditions, and to store the event streams in hardware priority queues. In one embodiment, the

deterministic scheduling controller is further configured to implement rate limiting and adaptive throttling for non-critical event streams to preserve latency guarantees for high-priority event streams. In one embodiment, the hypersonic event fabric and the plurality of neuromorphic compute cores are configured to provide fault tolerance by isolating malfunctioning compute cores and rerouting event packets through redundant communication paths.

The scheduling units are configured to select event packets for transmission and processing based on the assigned priority levels and associated deadline metadata, thereby enforcing deterministic execution order. The controller (110) further generates control signals to regulate routing within the hypersonic event fabric (108) and processing within the neuromorphic compute cores (106).

In one embodiment, rate limiting and adaptive throttling are implemented using hardware counters, token-based control mechanisms, or equivalent logic circuits configured to restrict processing of non-critical event streams, thereby preserving latency guarantees for high-priority event streams. The controller (110) enforces bounded latency by controlling admission of event packets into processing queues and by allocating processing and communication resources based on priority and deadline constraints.

The system (100) further comprises an adaptive learning engine (112) implemented using hardware logic and operatively coupled to the neuromorphic compute cores (106). The adaptive learning engine (112) comprises weight update circuits, constraint enforcement logic, drift detection circuits, and memory interface units. The weight update circuits are configured to modify synaptic weights stored in the synapse circuits (122) based on spike timing signals, neuron output signals, and feedback signals including error signals, reinforcement signals, or performance evaluation signals received from the neuromorphic compute cores (106), using hardware arithmetic units including adders, accumulators, or equivalent logic circuits.

The adaptive learning engine (112) enforces bounded update constraints using hardware comparators and control logic configured to limit weight updates based on predefined magnitude thresholds, rate limits, and stability conditions. The drift detection circuits are configured to monitor variations in neuron output signals or synaptic weight values using statistical counters or threshold comparison circuits to detect instability or anomalous behavior.

The adaptive learning engine (112) is further associated with a weight update and rollback mechanism (116) comprising memory storage configured to store validated synaptic weight states and control logic configured to restore previously stored weight states to the synapse circuits (122) upon detection of drift or instability. The restoration is performed through hardware-controlled memory read and write operations, thereby ensuring safe and stable continual learning within predefined operational bounds. In one embodiment, the adaptive learning engine is configured to enforce bounded update constraints on synaptic weights based on magnitude and rate thresholds and to perform rollback using stored model snapshots upon detection of instability or drift.

The weight update circuits, constraint enforcement logic, drift detection circuits, and memory interface units are implemented using digital hardware circuits including combinational and sequential logic elements configured to perform the aforementioned operations.

Outputs generated by the neuromorphic compute cores (106) are provided to a context management and task coordination controller (114) implemented in hardware. The controller (114) comprises aggregation circuits, associative memory structures, and decision logic circuits. The controller (114) aggregates outputs from the neuromorphic compute cores (106) using hardware accumulation units and registers to form contextual representations based on spike event patterns, priority parameters, and stored contextual data.

The controller (114) generates control decisions using hardware decision logic including comparators, threshold evaluation circuits, and rule-based logic units configured to evaluate the aggregated contextual data. The controller (114) further coordinates task execution by generating control signals for downstream components. In certain embodiments, the controller (114) performs priority-based arbitration using hardware arbitration logic and initiates verification operations using dedicated validation circuits when confidence levels fall below predefined thresholds.

The control decisions generated by the context management and task coordination controller (114) are transmitted to an output interface circuit (118). The output interface circuit (118) comprises hardware output drivers, communication interface circuits, and/or digital-to-analog conversion circuits configured to generate control signals for external systems, including robotic actuators, autonomous vehicle systems, industrial control systems, and security systems.

In operation, the system (100) processes input data through a deterministic event-driven pipeline comprising:

(i) conversion of input signals into spike events by the event encoder module (104),

(ii) bounded-latency routing of event packets via the hypersonic event fabric (108),

(iii) event-driven neuromorphic computation within the neuromorphic compute cores (106),

(iv) contextual aggregation and decision generation by the context management and task coordination controller (114), and

(v) generation of control outputs via the output interface circuit (118).

The architecture illustrated in Figure 1 achieves reduced memory-to-compute data transfer, improved energy efficiency, and deterministic worst-case response time compared to conventional computing architectures.

It is to be noted that the event encoder module (104), hypersonic event fabric (108), neuromorphic compute cores (106), deterministic scheduling controller (110), adaptive learning engine (112), context management and task coordination controller (114), and output interface circuit (118) are implemented as dedicated hardware components, including digital logic circuits, state machines, and/or application-specific integrated circuits (ASICs), configured to perform the recited functions. The processing involves physical transformation of input signals into spike event representations and hardware-level event propagation and computation, thereby providing a technical solution to a technical problem and not constituting a computer program per se.

Further, the integration of bounded-latency event routing, deterministic scheduling, and safety-bounded adaptive learning enables reliable operation in real-time environments and ensures that the system (100) maintains stability, predictability, and efficiency under varying input conditions.

In one embodiment, the system comprises a hierarchical memory system. The hierarchical memory system includes local synaptic memory within each neuromorphic compute core, associative memory configured to store contextual data, and non-volatile memory storing validated model parameters. In one embodiment, the system further includes associative memory for contextual storage and non-volatile memory for long-term storage of validated model parameters.

In certain embodiments, the system (100) further comprises a hybrid precision computation module implemented in hardware and operatively coupled to the neuromorphic compute cores (106). The hybrid precision computation module includes arithmetic units configured to selectively perform high-precision numerical operations, including floating-point or fixed-point computations, for verification, calibration, or normalization tasks. The module is configured to operate in conjunction with the event-driven neuromorphic compute cores (106), such that high-precision computation is

invoked only for selected operations requiring enhanced numerical accuracy, thereby maintaining overall computational efficiency while improving result fidelity.

In certain embodiments, the system (100) further comprises a security and integrity module implemented in hardware and configured to ensure secure operation of the neuromorphic processor system (100). The security and integrity module includes secure boot logic, encryption circuits, and anomaly detection circuits. The encryption circuits are configured to encrypt event packets transmitted through the hypersonic event fabric (108) using hardware-based cryptographic engines. The anomaly detection circuits are configured to monitor event patterns and system behavior using hardware comparators and statistical analysis circuits to detect unauthorized or adversarial inputs. The secure boot logic ensures that only authenticated firmware or configuration data is executed within the system.

In certain embodiments, the deterministic scheduling controller (110) is further configured to implement rate limiting and adaptive throttling using hardware counters, token-based control mechanisms, and queue management circuits to regulate processing of non-critical event streams and preserve latency guarantees for high-priority event streams.

In certain embodiments, the hypersonic event fabric (108) and the plurality of neuromorphic compute cores (106) are configured to provide fault tolerance through hardware-based error detection and recovery mechanisms. The system includes error detection circuits, redundant communication paths within the hypersonic event fabric (108), and isolation logic configured to identify and isolate malfunctioning neuromorphic compute cores (106). Upon detection of a fault, event packets are rerouted through alternate communication paths using hardware routing logic, thereby maintaining system operation in a degraded but functional state. The fault tolerance mechanism ensures reliable operation under hardware faults or adverse conditions.

In one embodiment, the system comprises a hybrid precision computation module implemented in hardware, configured to selectively execute high-precision numerical operations for verification, calibration, or normalization tasks while maintaining primary event-driven computation in the neuromorphic compute cores.

In one embodiment, the system comprises a security and integrity module implemented in hardware, configured to: perform secure boot operations, encrypt event packets transmitted through the hypersonic event fabric, and detect anomalous event patterns indicative of unauthorized or adversarial inputs.

The present invention relates to an Artificial Super Intelligence (ASI)–based neuromorphic hypersonic processor, hereinafter referred to as "the processor", which is designed to deliver ultra-low-latency (hypersonic) intelligent computation with high energy efficiency, safe continual learning, and deterministic real-time performance. The present invention combines event-driven neuromorphic computation with bounded-latency routing, hybrid precision processing, and a supervisory orchestration engine to overcome limitations of conventional von-Neumann AI processors and earlier neuromorphic chips.

In a preferred embodiment, the processor comprises a plurality of Neuromorphic Compute Cores (NCCs) interconnected through a Hypersonic Event Fabric (HEF). Each NCC includes programmable neuron circuits, synapse arrays, local memory, event encoders/decoders, and core-level controllers. The NCCs operate using an event-driven model wherein computation is triggered by incoming events/spikes rather than continuous clocked execution, thereby reducing redundant operations and minimizing unnecessary energy consumption.

Each neuromorphic compute core further implements configurable neuron models such as integrate-and-fire, adaptive spiking neurons, and other spiking dynamics, wherein neuron state variables are stored locally and updated only when events are received.

Synapses are implemented using programmable synaptic weight units that may be stored in digital memory, mixed-signal memory, or non-volatile weight retention memory. The synapse arrays support sparse activation, ensuring that only active pathways consume power, thereby enabling high efficiency for real-world temporal signals such as speech, motion, vibration, radar, or biomedical waveforms.

The invention introduces the Hypersonic Event Fabric (HEF) as a key architectural component. The HEF is an interconnect system configured to transport spikes/events among NCCs with bounded latency guarantees. In one embodiment, each event packet includes metadata fields such as event type, timestamp, priority level, and deadline. The HEF includes routing logic with priority-aware arbitration, congestion control, and guaranteed-service lanes for safety-critical tasks. This ensures that time-sensitive event streams such as collision alerts, emergency control signals, hazard detection triggers, or critical alarms are always delivered within a predetermined worst-case latency window.

In an embodiment, the processor further includes a Deterministic Scheduling and QoS Controller, which assigns priority classes to workloads based on safety criticality, latency requirement, and energy budget. The controller manages event admission, resource allocation, and execution scheduling across NCCs, ensuring that background learning tasks do not degrade real-time decision-making tasks. The scheduling mechanism may use deadline tagging, rate limiting for non-critical streams, and adaptive throttling during event storms to preserve deterministic performance.

The present invention also discloses a Hybrid Precision Compute Layer integrated with the neuromorphic cores. While primary inference is performed through spike/event-based computation, certain operations requiring numeric stability or verification can be executed using selective high-precision arithmetic units. These units may be invoked only under specified conditions, such as uncertainty resolution, sensor calibration, normalization of fused signals, safety-rule verification, or cryptographic integrity

checking. This hybrid approach enables higher accuracy and trustworthiness without sacrificing event-driven efficiency.

A further element of the invention is a Safety-Bounded Continual Learning Engine (SBCL Engine). The SBCL Engine performs adaptive updates of synaptic weights using local learning rules (e.g., spike-timing dependent plasticity, reward-modulated learning, error-gated plasticity) and/or supervised micro-updates depending on the application. Importantly, the SBCL Engine enforces bounded update constraints: synaptic updates are limited in magnitude, rate, and direction within predefined stability envelopes. The engine continuously monitors drift indicators, confidence scores, and performance metrics. If the processor detects instability, abnormal drift, adversarial event patterns, or degradation, it triggers a rollback mechanism that restores the last verified stable parameter version.

In one embodiment, the processor includes a Model Versioning and Rollback Memory System, comprises a multi-level memory hierarchy: (i) fast local synaptic memory per core, (ii) associative context memory for short-term retrieval and pattern linking, and (iii) persistent retention memory for long-term stable policies and verified parameters. The rollback mechanism maintains multiple signed snapshots of learned weights, allowing secure restoration when needed. This makes the processor suitable for long-duration deployment in changing environments while maintaining safety and reliability.

The processor further contains an ASI Orchestration Engine, which coordinates higher-level intelligent behaviors across the neuromorphic fabric. The orchestration engine manages context formation, goal selection, task switching, memory consolidation, and multi-module collaboration (perception, reasoning, planning, and action). In one embodiment, the orchestration engine uses confidence-aware arbitration, meaning that outputs with low confidence trigger additional verification, alternative inference paths, or human-in-the-loop escalation depending on deployment configuration.

In another embodiment, the invention includes a Trusted Security and Integrity Module. This module provides secure boot, hardware identity, encrypted event channels, tamper-aware logging, and anomaly detection. It monitors event flow patterns to identify spoofing, adversarial spikes, malicious learning updates, or unauthorized parameter changes. This ensures that the processor's continual learning and real-time decision outputs remain trustworthy, especially in applications where security threats exist.

The present invention also provides fault tolerance and resilience mechanisms. Each NCC and the HEF may include error correction, redundancy, and self-diagnostics. If a core experiences errors, overheating, or malfunction, the orchestration engine can isolate the core, reroute event flows through healthy paths, and continue operation in a degraded yet safe mode. Such resilience is critical for safety-critical and daily-use systems where uninterrupted service is required.

In operation, multi-modal sensor inputs are first converted into event streams via encoders that generate spikes based on change detection, temporal encoding, or feature thresholds. These events are routed via the HEF to relevant NCCs, where spiking inference and feature extraction occur. The orchestration engine aggregates outputs into context states, triggers appropriate policies, and generates control outputs. Simultaneously, the SBCL Engine performs bounded learning updates in the background, ensuring adaptation while preserving stability. When uncertainty or risk is detected, the hybrid precision units execute verification steps before final actuation. Accordingly, the disclosed invention provides a complete processor architecture and method that achieves hypersonic real-time intelligence, energy-efficient neuromorphic processing, safe continual learning, hierarchical orchestration, secure operation, and fault-resilient deployment. These features enable broad industrial applicability across everyday consumer devices, smart homes, vehicles, healthcare monitoring, robotics, and secure digital infrastructure.

FIG. 2 illustrates a flow chart of method for deterministic real-time processing of input data with bounded latency using a neuromorphic processor system, according to an embodiment of the present invention.

1) Multi-Modal Sensor Inputs at one or more sensor interface circuits (102)

The process begins when multiple sensors generate real-world data streams. These may include Radar (range and velocity), Vision (images/video), LiDAR (3D depth and point clouds), Biomedical signals (physiological waveforms), and Telemetry (system health, navigation, and status signals). The purpose of using multi-modal inputs is to build a richer, more reliable understanding of the environment and the device state. Because each sensor has different noise and failure characteristics, combining them improves robustness and reduces false alarms.

2) Spike Generation & Encoding at an event encoder module (104)

In this step, the raw sensor streams are transformed into spike/event streams suitable for neuromorphic processing. Instead of continuously processing every sample, the encoder generates events primarily when significant changes occur (for example, motion edges in vision, sudden range changes in radar/LiDAR, abnormal biomedical patterns, or telemetry threshold violations). The encoding is time-aware (time-encoded), meaning the event timing itself carries information. This reduces data volume, lowers energy consumption, and prepares signals for ultra-fast event routing.

3) Hypersonic Event Routing

The encoded events are sent to the Hypersonic Event Routing stage, which routes events through a bounded-latency, priority-aware mechanism. Here, events may be assigned priorities and deadlines based on urgency (e.g., collision risk events get the highest priority). The routing ensures that even under heavy sensor activity, critical events reach the correct neuromorphic cores within a guaranteed time window. The side connection to Learning Snapshots & Rollback indicates that routing and system

state are continuously monitored, and safety snapshots of the learning state can be triggered when abnormal patterns or instability are detected.

4) Spiking Neural Network Processing

After routing, the events enter the Spiking Neural Network Processing block. In this stage, neurosynaptic arrays and spiking neuron models perform event-driven inference, such as detection, recognition, prediction, or anomaly identification. Because this is spike-based computation, only the relevant pathways activate when events arrive, enabling high efficiency. This stage typically performs initial feature extraction and fast classification—turning raw event streams into structured information, such as object presence, threat probability, signal anomalies, or environmental changes.

5) Contextual Memory Formation

The output features from spiking processing are then organized into Contextual Memory Formation. This stage maps incoming patterns into temporal context, meaning it builds an understanding of "what is happening over time," not just at one instant. It may store associations in short-term memory and link new events with previous events to create a coherent situation model. The arrow labeled Learning Updates indicates that learning signals can update memory structures or synaptic weights so that the system adapts to changing environments while maintaining time continuity and relevance.

6) Hypersonic Decision Making

Using the formed context, the system performs Hypersonic Decision Making, which means selecting an action or response quickly within bounded deadlines. This stage uses context and goals to choose an optimized policy—for example, avoid obstacle, raise alert, adjust speed, modify actuator position, or trigger safety protocol. The term "hypersonic" here refers to extremely fast decision cycles and predictable response times, which are essential for real-time control systems.

7) ASI Orchestration Engine (Side Module)

The ASI Orchestration Engine acts as a supervisory intelligence coordinator connected to the decision and verification blocks. It manages global context, schedules tasks, assigns priorities, and coordinates decision planning across multiple processing paths. If multiple goals compete (e.g., safety vs performance), the orchestration engine applies arbitration rules. It can also trigger additional processing or verification when uncertainty is high, ensuring that the system behaves reliably under complex scenarios.

8) Action Policy Selection & Verification (Safety Gate)

Before final actuation, the selected action policy is passed through Action Policy Selection & Verification, where the system validates that the chosen output is safe and reliable. This may include confidence scoring, rule-based safety checks, boundary-condition validation, and fail-safe constraints. The diagram shows this block prominently because it is a key patent-worthy mechanism: decisions are not executed blindly; they are verified before being allowed to control real-world systems.

9) Duplicate "Action Policy Selection & Verification" Block

In the flowchart, this block appears twice (one in green and one in red). In patent terms, this can be interpreted as a two-stage verification pipeline: a first-pass verification (normal safety checks) and a second-pass or stricter verification (high-risk mode, emergency mode, or low-confidence mode). This is a valid architectural concept, but if simpler and cleaner name is required, it can be renamed as "Primary Policy Verification" and "Secondary Safety Validation / Fail-Safe Gate" to avoid repetition and to show clear functional difference.

10) Control Output (Robotics, Autonomous Vehicles, Defense Systems)

Finally, after verification, the system produces a Control Output. This output can drive actuators in robotics, steering/braking in autonomous vehicles, or command and alert outputs in defense or security systems. Because the architecture routes events quickly, processes them efficiently, forms context, and verifies policies before action, the resulting outputs are both fast and safer for real-world operation.

11) Learning Snapshots & Rollback (Safety Feedback Loop)

The side loop indicates a safety mechanism for continuous learning. When the system updates its learning parameters, snapshots are stored. If drift, instability, or abnormal event patterns are detected, the processor can roll back to a prior stable snapshot. This prevents unsafe behavior due to uncontrolled adaptation and supports long-term deployment in changing environments.

FIG. 3 illustrates an Artificial Super Intelligence (ASI)-based Neuromorphic Hypersonic Processor Architecture, according to an exemplary embodiment of the present invention.

1) Multi-Modal Sensor Inputs (Vision, Radar, LiDAR, Biomedical, Telemetry, Cyber Signals)

This block represents all real-world data sources feeding the processor. Vision provides image/video streams, radar and LiDAR provide range and motion information, biomedical signals include physiological waveforms, telemetry includes system/vehicle health and navigation data, and cyber signals include network and security events. The processor is designed to accept both high-rate continuous signals and sparse event-like signals, enabling real-time intelligence for everyday and mission-critical applications.

2) Event Encoder Module (Spike Generation & Encoding)

The event encoder converts raw sensor data into spike/event streams suitable for neuromorphic computation. Instead of continuously processing all samples, the encoder produces events only when meaningful changes occur (e.g., intensity change, edge movement, anomaly threshold crossing, timing features). This reduces redundant computation and power consumption, and it prepares data in a time-aware, event-driven format to be routed efficiently across the neuromorphic fabric.

3) ASI Orchestration Engine (Context Management, Decision Planning, Task Coordination)

This is the high-level supervisory unit that manages "what the system should do next." Context management maintains a live internal state—what is happening now, what has changed, and what matters. Decision planning selects actions or responses based on goals, constraints, and predicted outcomes. Task coordination distributes workloads across neuromorphic cores, assigns priorities, and ensures critical tasks (safety, emergencies) are handled first while background tasks (learning, optimization) run without disturbing real-time performance.

4) Hypersonic Event Fabric (HEF) – Priority-Aware Routing & Bounded Latency Interconnect

The HEF is the interconnect backbone that moves spikes/events between modules and cores with high speed and predictability. Unlike ordinary interconnects that can become slow or unpredictable during heavy traffic, the HEF uses priority-aware routing, congestion control, and bounded latency mechanisms. It ensures that urgent events (e.g., collision warnings, anomaly alarms) reach the required compute core within a guaranteed time limit, enabling "hypersonic" real-time reactions.

5) Neuromorphic Compute Cores (Core 1…Core N)

These cores are the primary processing units where neuromorphic inference and event-driven computation occur. Each core operates asynchronously or semi-asynchronously and processes incoming spikes to generate outputs such as classifications, predictions, detected patterns, or control signals. Multiple cores enable parallel processing—different cores can specialize in different sensor channels or different tasks (vision, navigation, anomaly detection, control), increasing throughput and reducing latency.

6) Neuron–Synapse Arrays (inside each core)

This component implements the spiking neural network computation. Artificial neurons integrate incoming spikes and fire output spikes when thresholds or dynamics are met. Synapses represent weighted connections that define how strongly one neuron influences another. These arrays allow time-based computation, temporal pattern learning, and event-driven inference, which is highly efficient for real-world streaming data compared to frame-based or batch-based processing.

7) Local Memory (inside each core)

Local memory stores neuron states, synaptic weights, routing tables, and intermediate results close to where computation happens. This reduces the need to fetch data from distant memory, reducing energy use and improving speed. It also supports fast real-time processing because frequently accessed parameters (weights, states, thresholds) are available within the core, enabling quick response to incoming events

8) Adaptive Synaptic Intelligence Layer (Bounded Learning Updates, Drift Detection & Rollback)

This layer is responsible for safe, controlled adaptation. It updates synaptic weights or learning parameters based on observed events and outcomes, enabling the processor to improve over time in changing environments. The “bounded learning updates” feature ensures updates remain within safe limits (magnitude and rate). Drift detection monitors for performance degradation, abnormal changes, or potential adversarial influence. If the system detects instability, it can trigger rollback to a previously verified stable model state, preventing unsafe behavior.

9) Model Version & Rollback Memory (Short-Term & Long-Term Storage)

This block stores multiple versions of learned parameters and policies. Short-term storage holds recent learning snapshots for quick revert if a new update causes instability. Long-term storage holds verified stable versions and baseline safety policies. This component enables lifecycle management of intelligence: the system can

learn continuously while still remaining accountable, auditable, and recoverable—important for both safety and regulatory compliance.

10) Trusted Security & Integrity Module (Secure Boot & Encryption, Anomaly Detection & Monitoring)

This module ensures the processor operates securely and resists tampering or malicious inputs. Secure boot ensures only authenticated firmware and configurations run on the device. Encryption protects event traffic and sensitive parameters during movement or storage. Anomaly detection monitors unusual event patterns, unauthorized learning attempts, or suspicious behavior. This is crucial for preventing adversarial attacks (spoofed sensor spikes, manipulated updates) and for maintaining trust in real-time outputs.

11) Real-Time Control Outputs (Actuation, Robotics, Defense Systems, Autonomous Vehicles)

This is the final output interface where the processor's decisions are translated into actions. Outputs may include motor commands, braking/steering signals, robotic arm movements, alerts, system control messages, or safety shutdown triggers. Because the architecture is designed for bounded latency and deterministic priority handling, the outputs can be generated quickly and reliably, even when the system is under heavy sensor load.

FIG. 4 illustractes a logic layer of an Artificial Super Intelligence (ASI)-based Neuromorphic Hypersonic Processor Architecture, according to an embodiment of the present invention, according to an embodiment of the present invention.

ASI Orchestration Layer:

The ASI Orchestration Layer constitutes the top-level intelligent control unit of the proposed system, configured to manage overall system objectives, contextual awareness, and decision governance. It performs goal and context management to

dynamically adapt system behavior based on mission requirements, while memory consolidation ensures retention and utilization of historical knowledge. The task arbitration module allocates computational and operational resources efficiently across subsystems. Additionally, the policy verification and safeguards mechanism enforces predefined safety, ethical, and operational constraints, thereby ensuring reliable and compliant execution of actions.

This is the **highest-level decision-making layer** responsible for global system intelligence and coordination.

- **Goal & Context Management:** Defines mission objectives and operational context dynamically.
- **Memory Consolidation:** Maintains long-term knowledge using adaptive memory models.
- **Task Arbitration:** Prioritizes and assigns tasks across subsystems.
- **Policy Verification & Safeguards:** Ensures all decisions comply with safety, ethical, and system constraints.

Hybrid Neuromorphic Computation Layer:

The Hybrid Neuromorphic Computation Layer serves as the primary processing core, integrating event-driven spiking neural networks with conventional computational pipelines. It processes time-encoded sensor data using sparse event-based representations to achieve high efficiency and low latency. The controlled mixed-precision pipeline dynamically adjusts computational precision to balance accuracy and speed, while time-stamped confidence outputs provide probabilistic decision metrics. This hybrid approach enables real-time, high-performance intelligence suitable for hypersonic and mission-critical environments.

This layer performs **high-speed, energy-efficient AI computation**.

- **Event-Driven Spiking Network:** Processes sparse, time-encoded signals similar to biological neurons.

- **Time-Encoded Sensor Data Handling:** Converts real-world inputs into spike-based formats.
- **Controlled Mixed-Precision Pipeline:** Optimizes performance using adaptive precision computing.
- **Confidence Outputs:** Produces probabilistic, time-stamped decision outputs.

Hypersonic Event Routing Layer:

The Hypersonic Event Routing Layer is designed to facilitate ultra-fast and deterministic communication between system modules. It incorporates deadline-tagged event transport mechanisms to ensure that time-sensitive data is delivered within strict latency constraints. Priority-aware scheduling optimizes resource allocation based on event urgency, while deterministic congestion control ensures stable and predictable data flow even under high-load conditions. This layer is critical for maintaining synchronization and responsiveness in high-speed operational scenarios.

This layer is responsible for **real-time data transport and scheduling**.

- **Deadline-Tagged Event Transport:** Ensures time-critical delivery of events.
- **Priority-Aware Scheduling:** Allocates resources based on urgency.
- **Deterministic Congestion Control:** Prevents delays in high-speed environments.

Safe Adaptive Learning Engine:

The Safe Adaptive Learning Engine enables continuous learning and system adaptation while maintaining operational safety. It implements safety-bounded synaptic updates to ensure that learning processes remain within predefined limits, thereby preventing instability. Drift monitoring and detection mechanisms identify changes in system behavior or environmental conditions, triggering adaptive responses. Furthermore, the inclusion of preemptive snapshots and rollback capabilities allows the system to revert to previously stable states in case of anomalies, ensuring robustness and reliability.

This layer handles **real-time learning and adaptation with safety guarantees**.

- **Safety-Bounded Synaptic Updates:** Learning occurs within predefined safe limits.
- **Drift Monitoring & Detection:** Identifies performance degradation or anomalies.
- **Preemptive Snapshots & Rollback:** Enables system recovery to stable states.

Trusted Security and Safety Layer:

The Trusted Security and Safety Layer provides comprehensive protection for both data and hardware components of the system. It incorporates encrypted event interfaces to secure communication across layers and prevent unauthorized access or data breaches. Hardware security policies are enforced to safeguard against tampering, malicious attacks, and system-level vulnerabilities. This layer ensures that the system operates in a secure and trustworthy manner, which is essential for critical applications such as defense and autonomous control.

This layer ensures **system integrity, security, and reliability**.

- **Encrypted Event Interface:** Secures communication between modules.
- **Hardware Security Policies:** Protects against tampering and cyber threats.

Event Encoder and Preprocessing Module:

The Event Encoder and Preprocessing module is responsible for converting raw multimodal input data into structured event-based representations compatible with neuromorphic processing. Continuous signals from sensors are transformed into discrete event signals, enabling efficient handling by spiking neural networks. This preprocessing step reduces redundancy, enhances computational efficiency, and ensures that only relevant temporal information is propagated through the system.

This layer transforms raw inputs into **event-based signals** for neuromorphic processing.

- Converts continuous sensor data → discrete spike/event signals.

Multimodal Inputs and Sensors:

The system is designed to accept diverse multimodal inputs, including vision, radar, LiDAR, biomedical signals, telemetry, and cyber inputs. These inputs provide comprehensive situational awareness by capturing environmental, operational, and system-level data. The integration of multiple sensor modalities enhances robustness, accuracy, and adaptability of the system in dynamic and complex environments.

This layer provides **diverse real-world data sources**:

- Vision, Radar, LiDAR
- Biomedical signals
- Telemetry & Cyber inputs

Intelligent Control Outputs:

The Intelligent Control Outputs represent the actionable decisions generated by the system. These outputs are directed toward various application domains, including robotics, automation systems, defense platforms, and autonomous vehicles. The outputs are generated in real-time based on processed data and learned intelligence, enabling precise and adaptive control of external systems.

This layer delivers **final actionable outputs**:

- Robotics control
- Automation systems
- Defense applications
- Autonomous vehicles

Signal Flow (Closed-Loop Architecture)

- Inputs → Encoding → Processing → Routing → Learning → Decision → Output
- Continuous feedback loop ensures **adaptive, real-time optimization**.

Overall System Operation:

The overall architecture operates as a closed-loop, event-driven system wherein multimodal inputs are encoded into event signals, processed through neuromorphic and hybrid computation layers, routed via ultra-low latency communication channels, and refined through adaptive learning mechanisms. The system continuously updates its behavior through feedback while maintaining security and safety constraints, thereby delivering reliable, intelligent, and real-time decision-making suitable for advanced autonomous and hypersonic applications.

FIG. 5 illustractes a flow diagram of a method for deterministic real-time processing of input data with bounded latency using a neuromorphic processor system, according to an embodiment of the present invention. In one embodiment, each of the steps 502–516 is implemented using dedicated hardware components and interconnections within the neuromorphic processor system, thereby ensuring that the method is executed through physical signal processing and hardware-level transformations rather than a computer program per se. The implementation of each step is described in detail below.

At step 502, the method comprises receiving multi-modal input signals is performed by the sensor interface circuits through hardware input ports, analog-to-digital converters (ADCs), and signal conditioning circuits. The sensor interface circuits are configured to sample incoming analog or digital signals at predefined sampling rates, normalize signal amplitudes, and buffer the signals in input registers or first-in-first-out (FIFO) buffers. In one embodiment, separate interface channels are provided for different sensor modalities, enabling parallel acquisition and preprocessing of input data streams.

At step 504, the method comprises converting the multi-model input signals into time-encoded spike event streams, which is performed by the event encoder module using hardware logic circuits. The event encoder module comprises comparator circuits, threshold detection units, temporal encoding circuits, and event generation logic. The

module generates spike events when the input signal exceeds predefined thresholds, exhibits temporal variation beyond a delta value, or satisfies feature detection conditions. The time of occurrence of each event is encoded using hardware timestamp generators, thereby producing time-encoded spike events suitable for event-driven processing.

At step 506, the method comprises routing of spike event streams as event packets between a plurality of neuromorphic compute cores (NCCs), which is performed by the hypersonic event fabric (HEF) using a hardware interconnect network comprising routers, arbiters, and communication links. Each event packet comprises timestamp, priority level, and deadline metadata, wherein the routing includes priority-aware and congestion-controlled communication to ensure bounded latency. Each router includes routing tables stored in local memory and arbitration logic configured to select output paths based on priority level and deadline metadata associated with each event packet. Congestion control is achieved through buffer management, backpressure signaling, and adaptive routing policies implemented in hardware. Guaranteed-service channels are allocated for high-priority events, thereby ensuring bounded latency even under high traffic conditions.

At step 508, the method comprises processing of spike event streams that is performed within the neuromorphic compute cores using event-driven neuromorphic computation including neuron processing circuits and synapse circuits. The neuron processing circuits implement hardware neuron models, including integrate-and-fire or adaptive spiking neuron circuits, wherein neuron state variables are updated using local registers or memory elements upon receipt of spike events. The synapse circuits apply stored synaptic weights to incoming events using multiply-accumulate or equivalent hardware operations. The computation is event-driven, such that processing occurs only when spike events are received, thereby reducing redundant operations and improving energy efficiency.

At step 510, the method comprises assigning and regulating priority levels for the spike event streams based on latency constraints, which is performed by the deterministic scheduling controller implemented in hardware. The controller includes priority assignment logic, scheduling tables, and control registers configured to classify event streams based on latency requirements and task criticality. The controller regulates event flow by issuing control signals to the hypersonic event fabric and neuromorphic compute cores, including rate limiting signals, admission control signals, and throttling commands. In one embodiment, the controller uses deadline-based scheduling and priority queues implemented in hardware memory structures.

At step 512, the method comprises updating synaptic weights within predefined bounded limits and restoring previously stored weight states upon detection of drift conditions, which is performed by the adaptive learning engine using hardware learning circuits. The adaptive learning engine comprises weight update units, constraint enforcement logic, drift detection circuits, and memory interface units. The weight update units compute synaptic weight adjustments based on spike timing relationships, error signals, or reinforcement signals. The constraint enforcement logic ensures that updates remain within predefined magnitude and rate limits. Drift detection circuits monitor statistical variations in output signals or weight values. Upon detection of instability or drift conditions, the engine retrieves previously stored weight states from a rollback memory and restores them to the synapse circuits.

At step 514, the method comprises aggregating outputs generated by the plurality of neuromorphic compute cores to form contextual data and generate one or more control decisions, which is performed by a context management and task coordination controller implemented in hardware. The controller comprises aggregation logic, associative memory structures, and decision logic circuits. Outputs from the neuromorphic compute cores are combined using hardware accumulation units and stored in context memory. The decision logic evaluates the aggregated data based on

predefined rules, priority parameters, and contextual relationships to generate control decisions. In certain embodiments, verification logic is included to validate decision outputs prior to execution.

At step 516, the method comprises generating control signals for an external system, which is performed by the output interface circuit through hardware output drivers, digital-to-analog converters (DACs), communication interfaces, or actuator control circuits. The output interface circuit converts processed digital signals into appropriate control signals compatible with external systems such as robotic actuators, vehicle control systems, or industrial devices. The output signals may include voltage levels, pulse-width modulated signals, or digital communication packets depending on the application.

Further, the method processes the spike event streams through a pipeline comprising event encoding, bounded-latency routing, event-driven computation, contextual aggregation, and output generation, thereby achieving reduced memory-to-compute data transfer, improved energy efficiency, and deterministic worst-case response time.

Accordingly, the method illustrated in Figure 5 is implemented through a sequence of hardware-executed operations involving physical transformation of input signals into spike events, hardware-level event routing, neuromorphic computation, bounded learning updates, and generation of control outputs. This implementation provides a technical solution to the problem of achieving deterministic real-time processing with bounded latency, reduced data movement, and improved energy efficiency.

The present invention provides a hardware-implemented neuromorphic processing architecture that can be deployed across multiple industrial and consumer applications requiring event-driven computation, bounded-latency decision-making, and safe adaptive learning. The system enables efficient processing of multi-modal data streams

in real-time environments. Some exemplary embodiments illustrating applications of the present invention are described below:

1. **Smartphones & personal assistants**
    - Faster on-device speech recognition, translation, and intent understanding with lower battery drain.
    - Always-on wake word detection and contextual reminders without sending data to the cloud.
2. **Wearables (smartwatch, fitness band)**
    - Continuous health monitoring (heart rhythm anomalies, stress patterns) with very low power.
    - Personalized coaching based on real-time sensor data.
3. **Smart home automation**
    - Instant detection of unusual sounds (glass break, smoke alarm, baby cry) and quick response.
    - Adaptive energy control (AC, lights) based on human activity patterns.
4. **Home security cameras & doorbells**
    - Real-time person/vehicle detection, intrusion alerts, and face recognition locally (privacy-friendly).
    - Event-driven processing reduces storage and power usage.
5. **Automobiles (cars, bikes, EVs)**
    - Advanced driver assistance: collision avoidance, lane monitoring, pedestrian detection with microsecond-level reaction.
    - Battery and thermal optimization through efficient edge inference.
6. **Traffic & smart city systems**
    - Faster signal control based on live traffic flow.
    - Real-time anomaly detection (accidents, crowd risk) with low energy cost.
7. **Education & learning devices**
    - AI tutoring on tablets/laptops that adapts instantly to student performance.

- Offline intelligent content summarization and personalized quizzes.

8. **Healthcare at home**
    - Smart medical devices: glucose monitors, digital stethoscopes, blood pressure devices with intelligent alerts.
    - Early warning for respiratory or cardiac risk patterns from continuous signals.
9. **Banking & digital payments security**
    - On-device fraud detection by monitoring unusual patterns in authentication and device behavior.
    - Faster biometric authentication (face/voice/fingerprint) with lower power.
10. **Customer service & communication**
    - Live call noise suppression, echo cancellation, and emotion/intent detection for better call quality.
    - Real-time captioning during meetings.
11. **Gaming & AR/VR**
    - Lower-latency gesture tracking and environment understanding for smoother AR/VR.
    - Smart NPC behavior and adaptive rendering optimization.
12. **Industrial safety for daily-use spaces**
    - Elevators, escalators, and building systems detecting abnormal vibration, overload, or hazards early.
    - Predictive maintenance alerts before breakdown.
13. **Public transport**
    - Smart ticketing, crowd flow analytics, and quick anomaly detection at stations.
    - Real-time monitoring of vehicle health and route optimization.
14. **Personal robotics**

- Vacuum robots, service robots, and assistants reacting instantly to obstacles and human movement.
- Better navigation indoors with low power consumption.

15. **Cybersecurity for home/office networks**

- Real-time threat detection on routers and endpoints by monitoring network events and device behavior.
- Faster response to suspicious activity without heavy cloud dependence.

The foregoing description describes embodiments of the present invention. It should be appreciated that these embodiments are described for the purpose of illustration only, and that numerous alterations and modifications may be practiced by those skilled in the art without departing from the scope of the invention. It is intended that all such modifications and alterations be included in so far as they come within the scope of the invention as claimed or the equivalents thereof.

We claim:

1. A neuromorphic processor system (100) for deterministic real-time processing of input data with bounded latency, the system comprising:

one or more sensor interface circuits (102) configured to receive multi-modal input signals;

an event encoder module (104) implemented using hardware logic and operatively coupled to the sensor interface circuits, the event encoder module being configured to convert the input signals into time-encoded spike event streams;

a plurality of neuromorphic compute cores (NCCs) (106) arranged in a scalable interconnect, each neuromorphic compute core comprising:

neuron processing circuits (120) configured to process spike events,

synapse circuits (122) storing programmable synaptic weights, and

a local memory (124) storing neuron state variables and routing information;

a hypersonic event fabric (HEF) (108) comprising a hardware interconnect network coupling the plurality of neuromorphic compute cores, the hypersonic event fabric being configured to:

transmit event packets between the neuromorphic compute cores, each event packet comprising timestamp, priority level, and deadline metadata, and

perform priority-aware routing and congestion-controlled communication to ensure bounded end-to-end latency;

a deterministic scheduling controller (110) implemented in hardware and configured to assign priority levels to event streams and regulate routing and processing across the hypersonic event fabric based on latency constraints;

an adaptive learning engine (112) implemented using hardware logic and configured to update synaptic weights within predefined bounded limits and to restore previously stored weight states upon detection of drift conditions;

a context management and task coordination controller (114) implemented in hardware and configured to aggregate outputs from the plurality of neuromorphic compute cores and generate one or more control decisions based on contextual data; and

an output interface circuit (118) configured to generate control signals for an external system;

wherein the neuromorphic processor system is configured to process the spike event streams through a processing pipeline comprising:

event encoding by the event encoder module,

bounded-latency routing via the hypersonic event fabric,

event-driven neuromorphic computation in the plurality of neuromorphic compute cores,

contextual data aggregation by the context management and task coordination controller, and

generation of control outputs via the output interface circuit;

thereby achieving reduced memory-to-compute data transfer, improved energy efficiency, and deterministic worst-case response time.

2. The neuromorphic processor system as claimed in claim 1, wherein the hypersonic event fabric is further configured to assign deadline tags and guaranteed-service routing channels to event packets associated with safety-critical operations, thereby ensuring delivery within a predefined latency bound.
3. The neuromorphic processor system as claimed in claim 1, wherein each neuromorphic compute core is configured to operate in an event-triggered asynchronous mode, such that computation is performed only upon receipt of spike events.
4. The neuromorphic processor system as claimed in claim 1, wherein the adaptive learning engine is configured to enforce bounded update constraints on synaptic weights based on magnitude and rate thresholds and to perform rollback using stored model snapshots upon detection of instability or drift.

5. The neuromorphic processor system as claimed in claim 1, further comprising a hierarchical memory system including:

local synaptic memory within each neuromorphic compute core,

associative memory configured to store contextual data, and

non-volatile memory storing validated model parameters.

6. The neuromorphic processor system as claimed in claim 1, wherein the context management and task coordination controller is further configured to perform priority-based arbitration of multiple event streams and to initiate a verification operation prior to generation of control outputs when a confidence parameter falls below a predefined threshold.

7. The neuromorphic processor system as claimed in claim 1, further comprising a hybrid precision computation module implemented in hardware, configured to selectively execute high-precision numerical operations for verification, calibration, or normalization tasks while maintaining primary event-driven computation in the neuromorphic compute cores.

8. The neuromorphic processor system as claimed in claim 1, further comprising a security and integrity module implemented in hardware, configured to:

perform secure boot operations,

encrypt event packets transmitted through the hypersonic event fabric, and

detect anomalous event patterns indicative of unauthorized or adversarial inputs.

9. The neuromorphic processor system as claimed in claim 1, wherein the deterministic scheduling controller is further configured to implement rate limiting and adaptive throttling for non-critical event streams to preserve latency guarantees for high-priority event streams.

10. The neuromorphic processor system as claimed in claim 1, wherein the hypersonic event fabric and the plurality of neuromorphic compute cores are configured to provide fault tolerance by isolating malfunctioning compute cores and rerouting event packets through redundant communication paths.

11. A method for deterministic real-time processing of input data with bounded latency using a neuromorphic processor system, the method comprising:

receiving, by one or more sensor interface circuits, multi-modal input signals;

converting, by an event encoder module implemented using hardware logic, the multi-modal input signals into time-encoded spike event streams;

routing, by a hypersonic event fabric (HEF) comprising a hardware interconnect network, the spike event streams as event packets between a plurality of neuromorphic compute cores (NCCs), each event packet comprising timestamp, priority level, and deadline metadata, wherein the routing includes priority-aware and congestion-controlled communication to ensure bounded latency;

processing, by the plurality of neuromorphic compute cores, the spike event streams using event-driven neuromorphic computation including neuron processing circuits and synapse circuits;

assigning and regulating, by a deterministic scheduling controller implemented in hardware, priority levels for the spike event streams based on latency constraints;

updating, by an adaptive learning engine implemented using hardware logic, synaptic weights within predefined bounded limits and restoring previously stored weight states upon detection of drift conditions;

aggregating, by a context management and task coordination controller implemented in hardware, outputs generated by the plurality of neuromorphic compute cores to form contextual data and generate one or more control decisions; and

generating, by an output interface circuit, control signals for an external system;

wherein the method processes the spike event streams through a pipeline comprising event encoding, bounded-latency routing, event-driven computation, contextual aggregation, and output generation,

thereby achieving reduced memory-to-compute data transfer, improved energy efficiency, and deterministic worst-case response time.

12. The method as claimed in claim 11, wherein routing by the hypersonic event fabric further comprises assigning deadline tags and guaranteed-service routing channels to event packets associated with safety-critical operations, thereby ensuring delivery within a predefined latency bound.

13. The method as claimed in claim 11, wherein processing by the plurality of neuromorphic compute cores comprises performing computation in an event-triggered asynchronous manner, such that processing is performed only upon receipt of spike events.

14. The method as claimed in claim 11, wherein updating synaptic weights further comprises enforcing bounded update constraints based on magnitude and rate thresholds and performing rollback using stored model snapshots upon detection of instability or drift.

15. The method as claimed in claim 11, further comprising selectively executing, by a hybrid precision computation module implemented in hardware, high-precision numerical operations for verification, calibration, or normalization tasks.

Dated this 28th day of March 2026

Signature

-Digitally Signed-
Anuradha Gupta
Patent Agent (IN/PA-1514)
Agent for the Applicant

ABSTRACT

ARTIFICIAL SUPER INTELLIGENCE-BASED NEUROMORPHIC HYPERSONIC PROCESSOR

The present invention discloses a neuromorphic processor system (100) for deterministic real-time processing of input data with bounded latency and its method. The system comprises sensor interface circuits (102), an event encoder module (104), neuromorphic compute cores (NCCs) (106), a hypersonic event fabric (HEF) (108), a deterministic scheduling controller (110), an adaptive learning engine (112), a context management and task coordination controller (114), and an output interface circuit (118). The sensor interface circuits (102) is configured to receive multi-modal input signals. The event encoder module (104) is configured to convert the input signals into time-encoded spike event streams. The HEF (108) is configured to: transmit event packets between the NCCs, and perform priority-aware routing and congestion-controlled communication to ensure bounded end-to-end latency. The deterministic scheduling controller (110) is configured to assign priority levels to event streams and regulate routing and processing across the hypersonic event fabric based on latency constraints.

FIG. 1

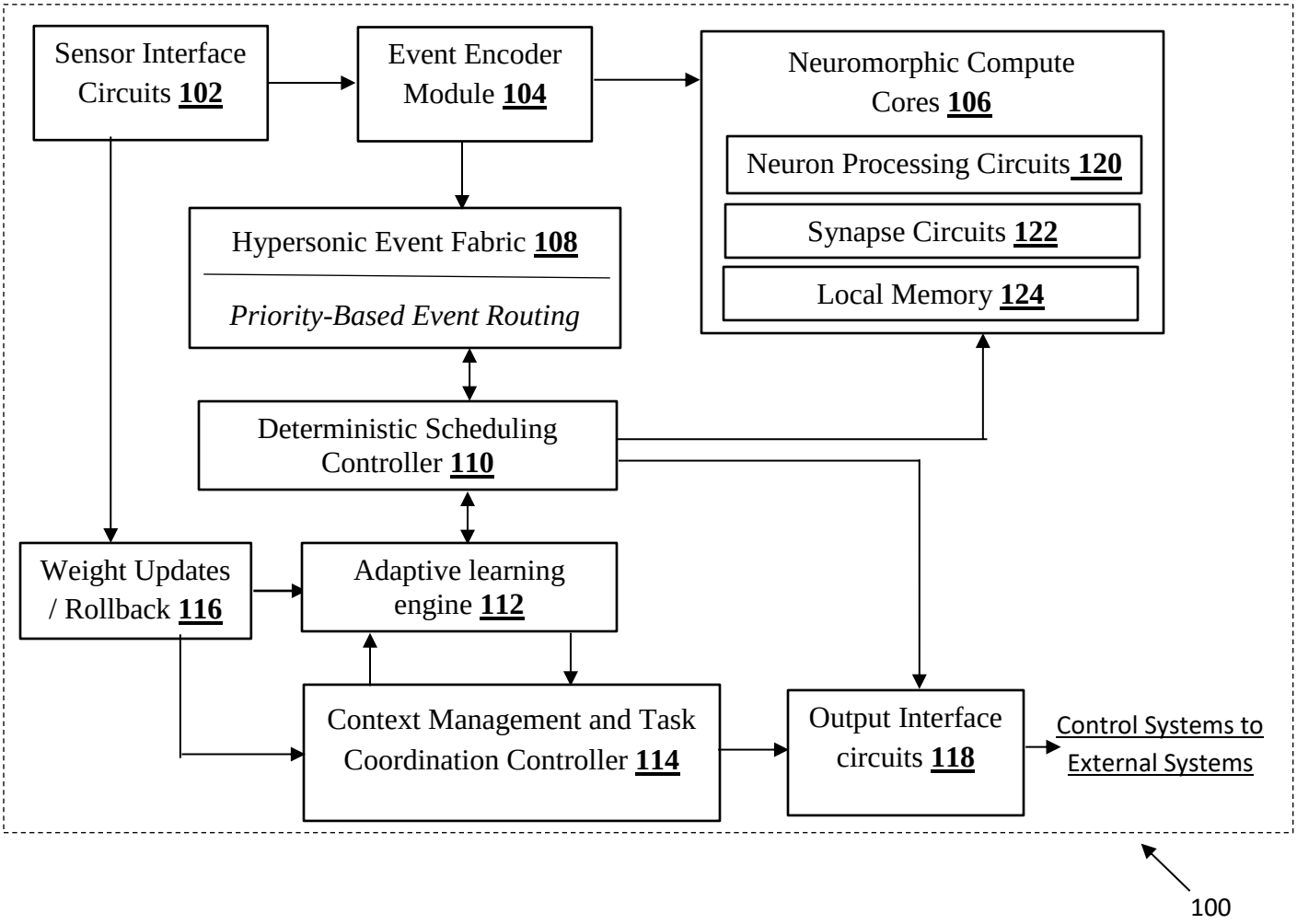

FIG. 1

-Digitally Signed-
ANURADHA GUPTA
Patent Agent (IN/PA-1514)
Agent for the applicant

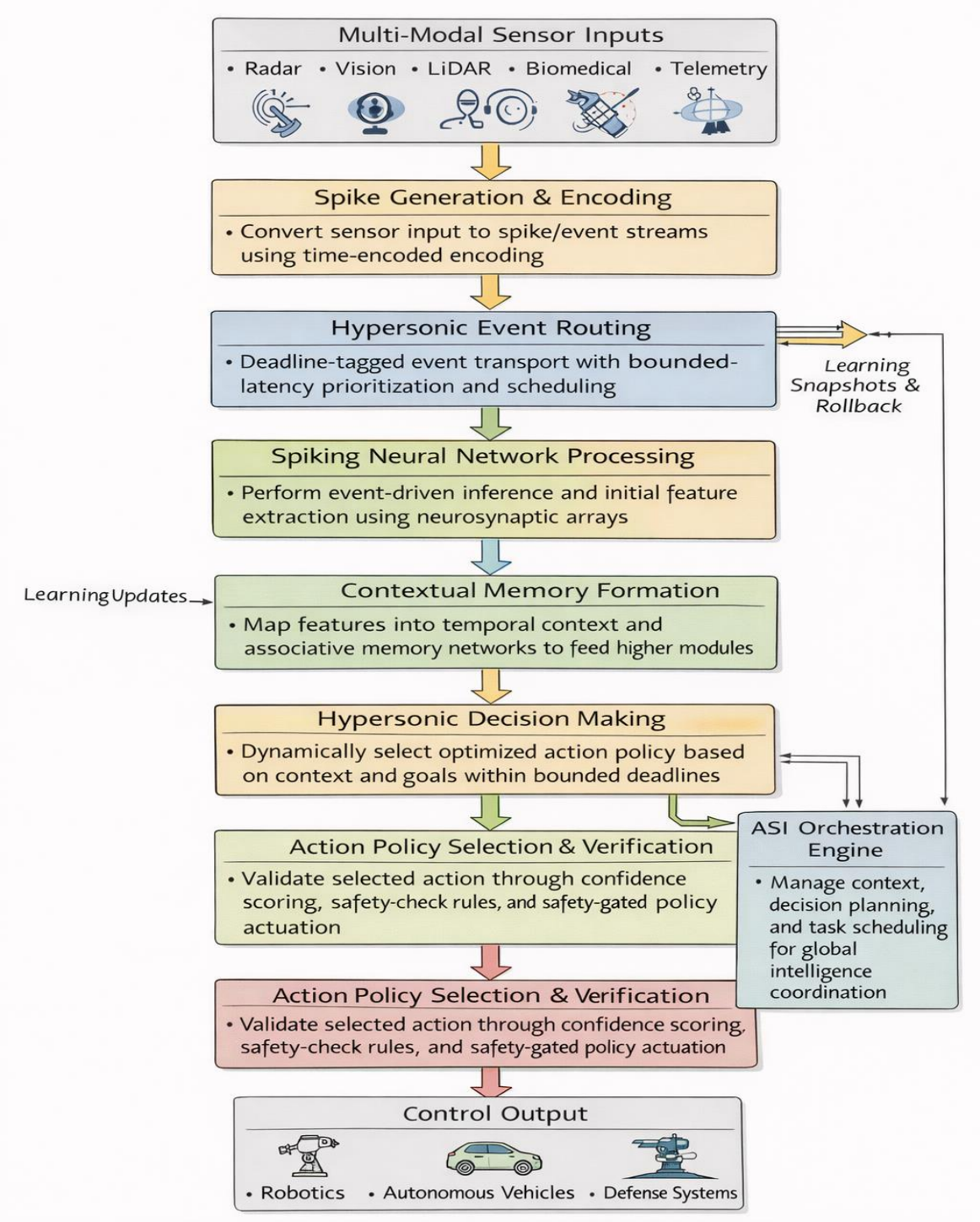

FIG. 2

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ANURADHA GUPTA
Patent Agent (IN/PA-1514)
Agent for the applicant

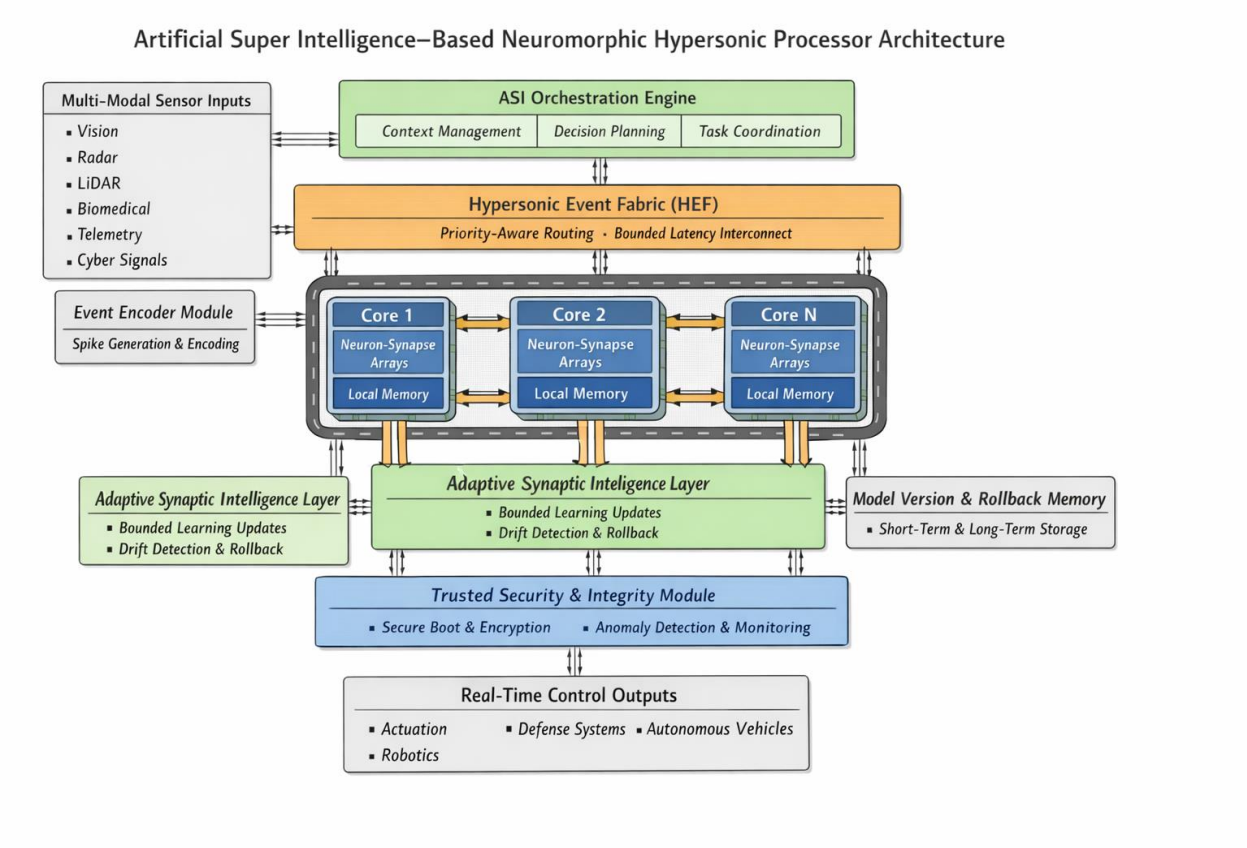

FIG. 3

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ANURADHA GUPTA
Patent Agent (IN/PA-1514)
Agent for the applicant

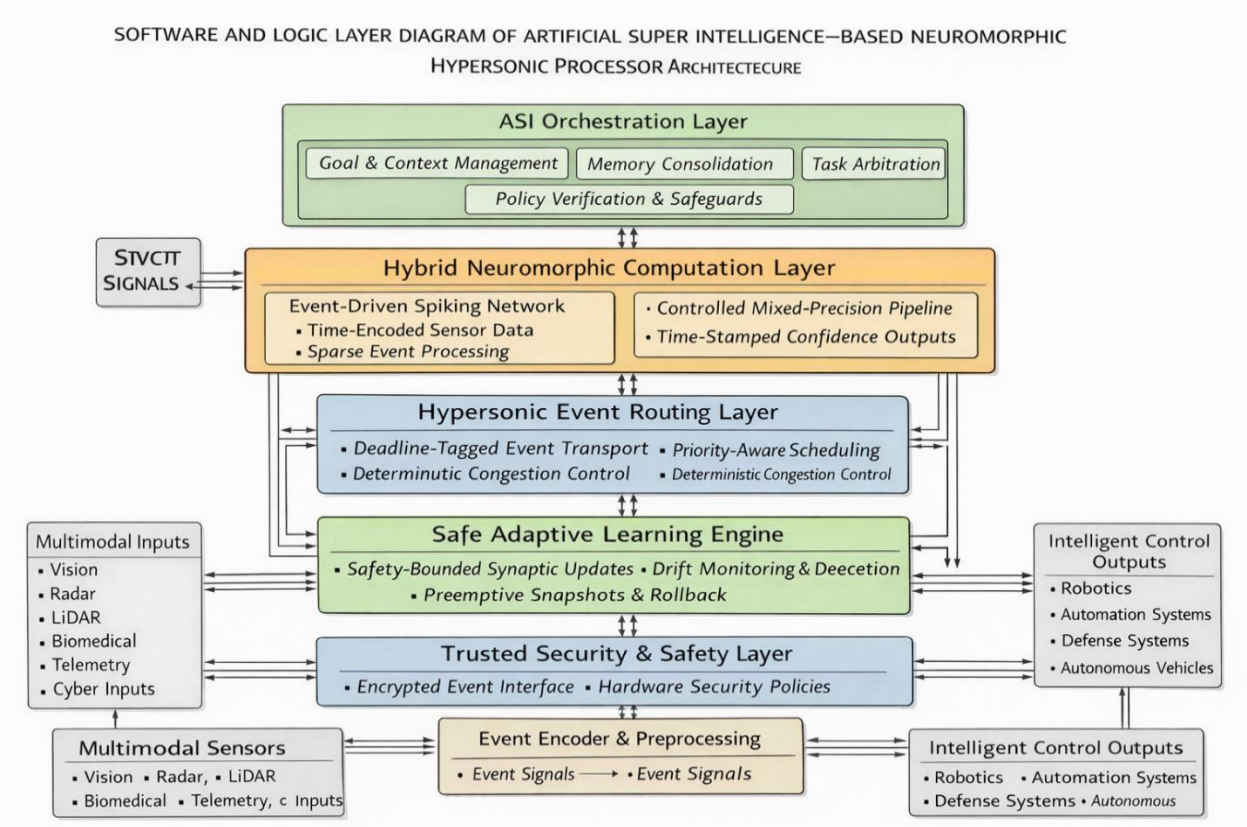

FIG. 4

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ANURADHA GUPTA
Patent Agent (IN/PA-1514)
Agent for the applicant

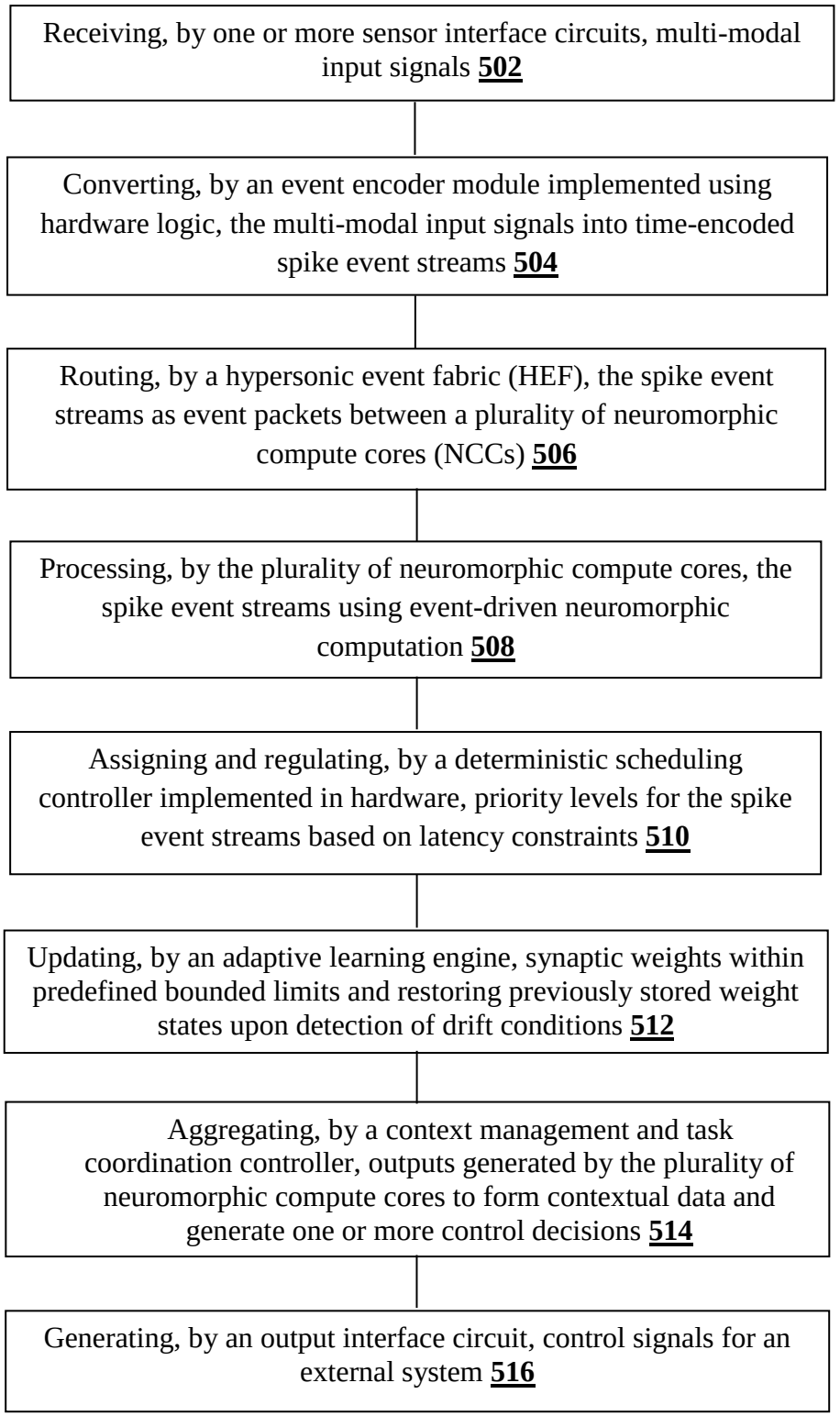

FIG. 5

-Digitally Signed-
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Patent Agent (IN/PA-1514)
Agent for the applicant

Digitally Signed By:
ANURADHA GUPTA
Date: 28-03-2026 18:34:58

FORM 1 THE PATENTS ACT 1970 (39 of 1970) and THE PATENTS RULES, 2003 APPLICATION FOR GRANT OF PATENT (See section 7, 54 and 135 and sub-rule (1) of rule 20)	(FOR OFFICE USE ONLY)

	Application No.	
	Filing date:	
	Amount of Fee paid:	
	CBR No:	
	Signature:	

1. APPLICANT'S REFERENCE / IDENTIFICATION NO. (AS ALLOTTED BY OFFICE)	

2. TYPE OF APPLICATION *Please tick (✓) at the appropriate category+

Ordinary (✓)		Convention ( )		PCT-NP ( )	
Divisional ( )	Patent of Addition ( )	Divisional ( )	Patent of Addition ( )	Divisional ( )	Patent of Addition ( )

3A. APPLICANT(S)

Name in Full	Nationality	Country of Residence	Address of the Applicant	
SRJX RESEARCH AND INNOVATION LAB LLP	**Indian Company**	**INDIA**	House No.	PLOT NO.-3E/474 SECTOR-9, CDA
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			City	CUTTACK
			State	ODISHA
			Country	**INDIA**
			Pin code	753014

3B. CATEGORY OF APPLICANT *Please tick (✓) at the appropriate category+

Natural Person ()	Other than Natural Person (✓)		
	Small Entity ( )	Startup (✓)	Others ()

4. INVENTOR(S) *Please tick (✓) at the appropriate category+

Are all the inventor(s) same as the applicant(s) Named above?	Yes ()	No (✓)

If "No", furnish the details of the inventor(s)

Name in Full	Nationality	Country of Residence	Address of the Inventor	
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			City	**CUTTACK**
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			Country	**INDIA**
			Pin code	753014
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SAHUKAR, Yamini Prasanna	**INDIAN**	**INDIA**	House No.	**No. 314, 3rd STAGE, 4th BLOCK, BASAVESHWARA NAGARA, BENGALURU-560079, KARNATAKA, INDIA**

5. TITLE OF THE INVENTION: **ARTIFICIAL SUPER INTELLIGENCE–BASED NEUROMORPHIC HYPERSONIC PROCESSOR**

6. AUTHORISED REGISTERED PATENT AGENT(S)	Patent Agent No.	**1514**
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7. ADDRESS FOR SERVICE OF APPLICANT IN INDIA	Name	**S G INTELLECTUAL**
	Postal Address	**4-D (UPPER FLOOR), DDA POCKET-2 SECTOR-6, DWARKA, NEW DELHI-110075, DELHI**
	Telephone No.	**011 35586108**
	Mobile No.	**9213764385**
	E-mail ID	sav@sgintellectual.com

8. IN CASE OF APPLICATION CLAIMING PRIORITY OF APPLICATION FILED IN CONVENTION COUNTRY, PARTICULARS OF CONVENTION APPLICATION				
Country	Application Number	Filing date	Name of the Applicant	Title of the Invention
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9. IN CASE OF PCT NATIONAL PHASE APPLICATION, PARTICULARS OF INTERNATIONAL APPLICATION FILED UNDER PATENT CO-OPERATION TREATY (PCT)	
International application number	International filing date
---	---

10. IN CASE OF DIVISIONAL APPLICATION FILED UNDER SECTION 16, PARTICULARS OF ORIGINAL (FIRST) APPLICATION-NA	
Original (first) application No	Date of filing of original (first) application
---	---

11. IN CASE OF PATENT OF ADDITION FILED UNDER SECTION 54, PARTICULARS OF MAIN APPLICATION OR PATENT-NA	
Main application/patent No.----------	Date of filing of main application ----------

12. DECLARATIONS

(i) Declaration by the inventor(s)-
(In case the applicant is an assignee: the inventor(s) may sign herein below or the applicant may upload the assignment or enclose the assignment with this application for patent or send the assignment by post/electronic transmission duly authenticated within the prescribed period).

We, the above named inventors are the true & first inventors for this Invention and declare that the applicant herein is our assignee ~~or legal representative~~.

i) (a) Date: 28-MAR-2026

(b) Signature: Soumya Ranjan Jena
(c) Name : **JENA, Soumya Ranjan**

ii) (a) Date: 28-MAR-2026

(b) Signature:
(c) Name: **GOWDA, Shankar B N**

iii) (a) Date: 28-MAR-2026

(b) Signature: P. Yamini Sahukar
(c) Name: **SAHUKAR, Yamini Prasanna**

ii) Declaration by the applicant(s) in the convention country ---N/A

~~(In case the applicant in India is different than the applicant in the convention country: the applicant in the convention country may sign herein below or applicant in India may upload the assignment from the applicant in the convention country or enclose the said assignment with this application for patent or send the assignment by post/electronic transmission duly authenticated within the prescribed period)~~

~~I/We, the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.~~

~~(a) Date~~

~~(b) Signature(s)~~

~~(c) Name(s)~~

(iii) Declaration by the applicant(s)

- ~~I~~/We the applicant(s) hereby declare(s) that: -
- ~~I am~~/We are in possession of the above-mentioned invention.
- The Complete Specification relating to the invention is filed with this Application.
- ~~The invention as disclosed in the specification uses the biological material from India and the necessary permission from the competent authority shall be submitted by me/us before the grant of patent to me/us.~~
- There is no lawful ground of objection(s) to the grant of the Patent to me/us.
- ~~I am/we are the true & first inventor(s).~~
- ~~I am~~/we are the assignee or legal representative of true & first inventor(s).
- ~~The application or each of the applications, particulars of which are given in Paragraph-8, was the first application in convention country/countries in respect of my/our invention(s).~~
- ~~I/We claim the priority from the above-mentioned application(s) filed in convention country/countries and state that no application for protection in respect of the invention had been made in a convention country before that date by me/us or by any person from which I/We derive the title.~~
- ~~My/our application in India is based on international application under Patent Cooperation Treaty (PCT) as mentioned in Paragraph-9.~~
- ~~The application is divided out of my /our application particulars of which is given in Paragraph-10 and pray that this application may be treated as deemed to have been filed on DD/MM/YYYY under section 16 of the Act.~~

13. FOLLOWING ARE THE ATTACHMENTS WITH THE APPLICATION

(a) Form 1

Item	Details	Fee	Remarks
Complete specification	No. of Pages - 46	Rs. 7520/-	
Claim(s)	No. of Claims - 15 No. of Pages - 5	----------	----------
Abstract	No. of Pages - 1		
Drawing(s)-	No. of Drawings - 5 No. of Pages - 5		

(b) Complete Specification
(d) Drawings
(c) Abstract
(d) Application Form-1
(e) Power of Attorney
(f) DIPP Certificate.
(g) Form-28
.....

We hereby declare that to the best of our knowledge, information and belief, the fact and matters stated herein are correct and We request that a patent may be granted to us for the said invention.

Dated this 28th day of March 2026

Signature: Soumya Ranjan Jena
(Dr. Soumya Ranjan Jena)
DIRECTOR
Name of Applicant: SRJX RESEARCH AND INNOVATION LAB LLP

To
The Controller of Patents
The Patent Office, KOLKATA

SRJX Research and Innovation Lab LLP
LLPIN: ACO-1435

Digitally Signed By:
ANURADHA GUPTA
Date: 11-04-2026 13:51:51

FORM 18 A **THE PATENTS ACT,1970** **and THE PATENT RULES,2003** **REQUEST FOR EXPEDITED EXAMINATION OF APPLICATION FOR PATENT** **[See section 11B and Rule 24C]**	(FOR OFFICE USE ONLY) RQ. No.: Filing Date: Amount of fee Paid: CBR no: Signature:

1. APPLICANT:

(A) NAME: **SRJX RESEARCH AND INNOVATION LAB LLP**

(B) NATIONALITY: **Indian Company**

(C) ADDRESS: **PLOT No.-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK- 753014, ODISHA, INDIA**

2. We, **SRJX RESEARCH AND INNOVATION LAB LLP** established at PLOT No-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK- 753014, ODISHA, INDIA, hereby request that our Application Patent No. 202631038691 filed on 28th March 2026 for invention Titled "**ARTIFICIAL SUPER INTELLIGENCE-BASED NEUROMORPHIC HYPERSONIC PROCESSOR"** shall be examined under sections 12 and 13 of the Act.

~~or~~

~~I/We ---------- hereby request that my/our application for patent no. ---------- filed on ---------- for ---------- the ---------- invention titled ---------- based on Patent Cooperation Treaty (PCT) application no……..…. dated…….. made in country …….. shall be examined under sections 12 and 13 of the Act, immediately without waiting for the expiry of 31 months as specified in rule 20(4)(ii). or~~

~~I/We hereby request that my/our request for examination bearing no. ---------- for application for patent no. ---------- filed on ---------- for ---------- the ---------- invention titled ---------- may be converted to a request for expedited examination of patent application under rule 24C and the application shall be examined under sections 12 and 13 of the Act.~~

3. The applicant(s) to indicate (by ticking the appropriate box) any of the grounds applicable for request for expedited examination:

() that India has been indicated as the competent International Searching Authority or elected as an International Preliminary Examining Authority in the corresponding international application; or

(✓) that the applicant is a startup; or

( ) that the applicant is a small entity; or

( ) that the applicant is a natural person or in the case of joint applicants, all the applicants are natural persons, then applicant or at least one of the applicants is a female; or

( ) that the applicant is a department of the Government; or

( ) that the applicant is an institution established by a Central, Provincial or state Act, which is owned or controlled by the Government; or

( ) that the applicant is a Government company as defined in clause (45) of section 2 of the Companies Act, 2013 (18 of 2013); or

( ) that the applicant is an institution wholly or substantially financed by the Government; or

( ) that the application pertains to a sector which has been notified by the Central Government, on the basis of a request from the head of department of the Central Government; or

( ) that the applicant is eligible under an arrangement for processing a patent applicant pursuant to an agreement between Indian Patent Office and a foreign Patent Office.

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4-D (UPPER FLOOR), DDA Pocket-2, Sector-6, Dwarka, New Delhi-110075, India
Mobile No. +91 9213764385
Email: sav@sgintellectual.com; anuradha@sgintellectual.com

Dated this 29th day of March, 2026

Signature

-Digitally Signed-

Name of the signatory: **Anuradha Gupta**

Agent for the Applicant

IN/PA-1514

To
The Controller of Patent
The Patent Office, at Kolkata

FORM 3

THE PATENT ACT, 1970

(39 of 1970)

and

THE PATENTS RULES, 2003

STATEMENT AND UNDERTAKING UNDER SECTION 3

(See Section 8; Rule 12)

1. Name of Applicant	I/We, **SRJX RESEARCH AND INNOVATION LAB LLP** established at PLOT No-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK- 753014, ODISHA, INDIA, Hereby Declare:
	(i) That I/We who have made the application for Patent number 202631038691 in India, dated 28th March 2026 alone (ii) that I/We have not made any application for the same/substantially the same invention outside India Or (ii) ~~that I/We have made for the same/substantially same invention, application(s) for patent in the other countries, the particular of which are given below:~~

Name of the Country	**Date of application**	**Application No.**	**Status of the application**	**Date of publication**	**Date of grant**
---	---	NIL	---	---	---

2. Name and address of the assignee	~~(i) that the rights in the application(s) filed in India has/have been assigned to…….~~ (ii) that I/We undertake that upto the date of grant of the patent by the Controller, I/We would keep him informed in writing regarding the details of corresponding applications for patents filed outside India in accordance with the provisions contained in section 8 and rule 12. Dated this 29th day of March 2026.
3. To be signed by the applicant or his authorized registered patent agent	-Digitally Signed- Signature
4. Name of the Natural person who has signed	(**Anuradha Gupta)** Patent Agent (IN/PA-1514) Agent for the Applicant
	To The Controller of Patents, The Patent Office At Kolkata

Digitally Signed By:
ANURADHA GUPTA
Date: 29-03-2026 13:30:01

FORM 5
THE PATENTS ACT, 1970
(39 of 1970)
&
The Patents Rules, 2003
DECLARATION AS TO INVENTORSHIP
[See section 10(6) and Rule 13 (6)]

1. **NAME OF THE APPLICANTS: SRJX RESEARCH AND INNOVATION LAB LLP** established at PLOT No-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK-753014, ODISHA, INDIA,

hereby declare that the true and first inventor(s) of the invention disclosed in the Complete specification filed in pursuance of our application Numbered 202631038691 dated 28th March 2026 are:

2. INVENTORS:

(i) (a) NAME : JENA, Soumya Ranjan
(b) NATIONALITY : INDIAN
(c) ADDRESS : PLOT NO-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK- 753014, ODISHA, INDIA

(ii) (a) NAME : GOWDA, Shankar B N
(b) NATIONALITY: INDIAN
(c) Address : No. 6, KANNAGUNI, N M PURA POST, YEDIUR HOBLI, KUNIGAL TALUK, TUMKUR DISTRICT, BANGALORE-572130, KARNATAKA, INDIA

(iii) (a) NAME : SAHUKAR, Yamini Prasanna
(b) NATIONALITY: INDIAN
(c) Address : No. 314, 3rd STAGE, 4th BLOCK, BASAVESHWARA NAGARA, BENGALURU-560079, KARNATAKA, INDIA

3. DECLARATION TO BE GIVEN WHEN THE APPLICATION IN INDIA IS FILED BY THE APPLICANT(~~S~~) IN THE CONVENTION COUNTRY :- N/A

~~We the applicant in the convention country hereby declares that our right to apply for a Patent in India is by way of assignment from the true and first inventors.~~

-Digitally Signed-

Dated this 29th day of March 2026 Name of the signatory **Anuradha Gupta**
Patent agent - IN/PA-1514

4. STATEMENT (to be signed by the additional inventor(s) not mentioned in the application **F**orm : **N/A**

~~/We assent to the invention referred to in the above declaration, being included in the Complete specification filed in pursuance of the stated application.~~

Dated this day of 20……..

Signature of the additional inventor(s):

Name----------

To
The Controller of Patent
The Patent Office Branch
At KOLKATA

Digitally Signed By:
ANURADHA GUPTA
Date: 29-03-2026 13:30:28

FORM 9
THE PATENTS ACT, 1970
(39 of 1970)
&
The Patents Rules, 2003
REQUEST FOR PUBLICATION
[See section 11A (2); Rule 24A]

1. Name, address and nationality of Applicant(s)	We, **SRJX RESEARCH AND INNOVATION LAB LLP** a Company registered in India, having office at PLOT No.-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK- 753014, ODISHA, India,
2. To be signed by the applicant or his authorized registered patent agent	hereby request for early publication of our Patent Application No. 202631038691 **dated 28th March 2026** under Section 11A (2) of the Patent Act.

.

Dated this 29th day of March 2026

3. Name of the natural person who has signed.	-Digitally Signed- (Anuradha Gupta) Patent Agent (IN/PA-1514) Agent for the Applicant

To
The Controller of Patents,
The Patent Office,
At KOLKATA

Digitally Signed By:
ANURADHA GUPTA
Date: 29-03-2026 13:21:25

FORMS 28
THE PATENTS ACT, 1970
(39 of 1970)
AND
THE PATENTS RULES, 2003
TO BE SUBMITTED BY A SMALL ENTITY / STARTUP
[See rules 2 (fa), 2(fb) and 7]

1.	Insert name, address and nationality	We, **SRJX RESEARCH AND INNOVATION LAB LLP**, a company registered in India, having office at PLOT NO.-3E/474, SECTOR-9, CDA, POST- MARKAT NAGAR, CUTTACK-753014, ODISHA, INDIA Applicant in respect of the patent application No. 202631038691. Hereby declare that we are a startup in accordance with rule 2(fb) and submit the following documents(s) as proof:
2.	Documents to be submitted	
	ii. For claiming the status of a startup	
	A. For an Indian applicant: Any document as evidence of eligibility, as defined in rule 2(fb).	
	Certificate of Recognition issued by DIPP: Certificate No. DIPP203406	
3.	To be signed by the applicant(s) / patentee(s) / authorized registered patent agent.	The information provided herein is correct to the best of our knowledge and belief. Dated this 29th day of March 2026.
4.	Name of the natural person who has signed. Designation and official seal, if any, of the person who has signed.	Signature : -Digitally Signed- (Anuradha Gupta) Patent Agent (IN/PA-1514) Agent for the Applicant To The Controller of Patents, The Patent Office, At Kolkata.

Digitally Signed By:
ANURADHA GUPTA
Date: 29-03-2026 14:19:01

FORM 1 THE PATENTS ACT 1970 (39 of 1970) and THE PATENTS RULES, 2003 APPLICATION FOR GRANT OF PATENT (See section 7, 54 and 135 and sub-rule (1) of rule 20)	(FOR OFFICE USE ONLY)

	Application No.	
	Filing date:	
	Amount of Fee paid:	
	CBR No:	
	Signature:	

1. APPLICANT'S REFERENCE / IDENTIFICATION NO. (AS ALLOTTED BY OFFICE)	

2. TYPE OF APPLICATION *Please tick (✓) at the appropriate category+

Ordinary (✓)		Convention ( )		PCT-NP ( )	
Divisional ( )	Patent of Addition ( )	Divisional ( )	Patent of Addition ( )	Divisional ( )	Patent of Addition ( )

3A. APPLICANT(S)

Name in Full	Nationality	Country of Residence	Address of the Applicant	
SRJX RESEARCH AND INNOVATION LAB LLP	**Indian Company**	**INDIA**	House No.	PLOT NO.-3E/474 SECTOR-9, CDA
			Street	POST- MARKAT NAGAR,
			City	CUTTACK
			State	ODISHA
			Country	**INDIA**
			Pin code	753014

3B. CATEGORY OF APPLICANT *Please tick (✓) at the appropriate category+

Natural Person ()	Other than Natural Person (✓)		
	Small Entity ( )	Startup (✓)	Others ()

4. INVENTOR(S) *Please tick (✓) at the appropriate category+

Are all the inventor(s) same as the applicant(s) Named above?	Yes ()	No (✓)

If "No", furnish the details of the inventor(s)

Name in Full	Nationality	Country of Residence	Address of the Inventor	
JENA, Soumya Ranjan	**INDIAN**	**INDIA**	House No.	**PLOT NO.-3E/474 SECTOR-9, CDA**
			Street	**POST- MARKAT NAGAR**
			City	**CUTTACK**
			State	**ODISHA**
			Country	**INDIA**
			Pin code	753014
GOWDA, Shankar B N	**INDIAN**	**INDIA**	House No.	**No. 6, KANNAGUNI, N M PURA POST YEDIUR HOBLI KUNIGAL TALUK TUMKUR DISTRICT BANGALORE - 572130, KARNATAKA, INDIA**
SAHUKAR, Yamini Prasanna	**INDIAN**	**INDIA**	House No.	**No. 314, 3rd STAGE, 4th BLOCK, BASAVESHWARA NAGARA, BENGALURU-560079, KARNATAKA, INDIA**

5. TITLE OF THE INVENTION: **ARTIFICIAL SUPER INTELLIGENCE–BASED NEUROMORPHIC HYPERSONIC PROCESSOR**

6. AUTHORISED REGISTERED PATENT AGENT(S)	Patent Agent No.	**1514**
	Name	**ANURADHA GUPTA**
	Mobile No.	**9213764385**
7. ADDRESS FOR SERVICE OF APPLICANT IN INDIA	Name	**S G INTELLECTUAL**
	Postal Address	**4-D (UPPER FLOOR), DDA POCKET-2 SECTOR-6, DWARKA, NEW DELHI-110075, DELHI**
	Telephone No.	**011 35586108**
	Mobile No.	**9213764385**
	E-mail ID	sav@sgintellectual.com

8. IN CASE OF APPLICATION CLAIMING PRIORITY OF APPLICATION FILED IN CONVENTION COUNTRY, PARTICULARS OF CONVENTION APPLICATION				
Country	Application Number	Filing date	Name of the Applicant	Title of the Invention
---	---	---	---	---

9. IN CASE OF PCT NATIONAL PHASE APPLICATION, PARTICULARS OF INTERNATIONAL APPLICATION FILED UNDER PATENT CO-OPERATION TREATY (PCT)	
International application number	International filing date
---	---

10. IN CASE OF DIVISIONAL APPLICATION FILED UNDER SECTION 16, PARTICULARS OF ORIGINAL (FIRST) APPLICATION-NA	
Original (first) application No	Date of filing of original (first) application
---	---

11. IN CASE OF PATENT OF ADDITION FILED UNDER SECTION 54, PARTICULARS OF MAIN APPLICATION OR PATENT-NA	
Main application/patent No.----------	Date of filing of main application ----------

12. DECLARATIONS

(i) Declaration by the inventor(s)-
(In case the applicant is an assignee: the inventor(s) may sign herein below or the applicant may upload the assignment or enclose the assignment with this application for patent or send the assignment by post/electronic transmission duly authenticated within the prescribed period).

We, the above named inventors are the true & first inventors for this Invention and declare that the applicant herein is our assignee ~~or legal representative~~.

i) (a) Date: 28-MAR-2026

(b) Signature: Soumya Ranjan Jena
(c) Name : **JENA, Soumya Ranjan**

ii) (a) Date: 28-MAR-2026

(b) Signature:
(c) Name: **GOWDA, Shankar B N**

iii) (a) Date: 28-MAR-2026

(b) Signature: P. Yamini Sahukar
(c) Name: **SAHUKAR, Yamini Prasanna**

ii) Declaration by the applicant(s) in the convention country ---N/A

~~(In case the applicant in India is different than the applicant in the convention country: the applicant in the convention country may sign herein below or applicant in India may upload the assignment from the applicant in the convention country or enclose the said assignment with this application for patent or send the assignment by post/electronic transmission duly authenticated within the prescribed period)~~

~~I/We, the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.~~

~~(a) Date~~

~~(b) Signature(s)~~

~~(c) Name(s)~~

(iii) Declaration by the applicant(s)

- ~~I~~/We the applicant(s) hereby declare(s) that: -
- ~~I am~~/We are in possession of the above-mentioned invention.
- The Complete Specification relating to the invention is filed with this Application.
- ~~The invention as disclosed in the specification uses the biological material from India and the necessary permission from the competent authority shall be submitted by me/us before the grant of patent to me/us.~~
- There is no lawful ground of objection(s) to the grant of the Patent to me/us.
- ~~I am/we are the true & first inventor(s).~~
- ~~I am~~/we are the assignee or legal representative of true & first inventor(s).
- ~~The application or each of the applications, particulars of which are given in Paragraph-8, was the first application in convention country/countries in respect of my/our invention(s).~~
- ~~I/We claim the priority from the above-mentioned application(s) filed in convention country/countries and state that no application for protection in respect of the invention had been made in a convention country before that date by me/us or by any person from which I/We derive the title.~~
- ~~My/our application in India is based on international application under Patent Cooperation Treaty (PCT) as mentioned in Paragraph-9.~~
- ~~The application is divided out of my /our application particulars of which is given in Paragraph-10 and pray that this application may be treated as deemed to have been filed on DD/MM/YYYY under section 16 of the Act.~~

13. FOLLOWING ARE THE ATTACHMENTS WITH THE APPLICATION

(a) Form 1

Item	Details	Fee	Remarks
Complete specification	No. of Pages - 46	Rs. 7520/-	
Claim(s)	No. of Claims - 15 No. of Pages - 5	----------	----------
Abstract	No. of Pages - 1		
Drawing(s)-	No. of Drawings - 5 No. of Pages - 5		

(b) Complete Specification
(d) Drawings
(c) Abstract
(d) Application Form-1
(e) Power of Attorney
(f) DIPP Certificate.
(g) Form-28
.....

We hereby declare that to the best of our knowledge, information and belief, the fact and matters stated herein are correct and We request that a patent may be granted to us for the said invention.

Dated this 28th day of March 2026

Signature: Soumya Ranjan Jena
(Dr. Soumya Ranjan Jena)
DIRECTOR
Name of Applicant: SRJX RESEARCH AND INNOVATION LAB LLP

To
The Controller of Patents
The Patent Office, KOLKATA

SRJX Research and Innovation Lab LLP
LLPIN: ACO-1435

Digitally Signed By:
ANURADHA GUPTA
Date: 11-04-2026 13:51:51

सत्यमेव जयते

INDIA NON JUDICIAL

Government of National Capital Territory of Delhi

₹100

e-Stamp

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Certificate No.	:	IN-DL49794072924674Y
Certificate Issued Date	:	07-Feb-2026 06:44 PM
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Second Party	:	SATYA NARAYAN SAV AND ANURADHA GUPTA
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SELF PRINTED CERTIFICATE TO BE VERIFIED BY THE RECIPIENT AT WWW.SHCILESTAMP.COM

IN-DL49794072924674Y

Please write or type below this line

FORM 26

THE PATENTS ACT, 1970

(39 of 1970)

&

THE PATENTS RULES, 2003

Form of authorization of a patent agent/or any person in a matter or proceeding under the Act

(See sections 127 and 132 and rule 135)

We,

SRJX RESEARCH AND INNOVATION LAB LLP, a company registered in India, having office at **PLOT NO.-3E/474, SECTOR-9, CDA, POST-MARKAT NAGAR, CUTTACK- 753014, ODISHA, INDIA**

do hereby authorize **S. N. Sav and Anuradha Gupta**, Patent Agent of **S G Intellectual**, 4-D (UPPER FLOOR) DDA Pocket-2, Sector-6, Dwarka, New Delhi--110075, **Delhi** , and also at A-108, Block -A, MBR Shangri La, Mysore Road, Kengeri, **Bangalore**-560059, India and/or all or any Associates/ Partners of the firm, to act on our behalf in connection with filing any and all Patent Application for any and all the inventions with the Controller of Patents, appearing on our behalf before the Controller, processing our application in respect of the same, filing provisional and/or complete specifications, and other necessary request and documents in connection with the grant of Patent for the patent application, obtaining certified copies/extracts from the Patent Office, Certificate/s of Registration, filing request for renewal of the Patent and generally to do all acts, deeds and things that may be necessary in connection with the above application, including appointment of any substitute or substitutes.

We request that all notices, requisitions and communication relating thereto may be sent to such person at the above address unless otherwise specified.

We hereby revoke all our previous authorization, if any made, in respect of same matter or proceeding.

We hereby assent to the action already taken by the above said person in the matter.

Dated this 7th day of **February 2026**

Soumya Ranjan Jena

(Dr. Soumya Ranjan Jena)
Designation: Director
SRJX RESEARCH AND INNOVATION LAB LLP

To,
The Controller of Patents
Patent Office, Kolkata

SRJX Research and Innovation Lab LLP
LLPIN: ACO-1435

Digitally Signed By:
ANURADHA GUPTA
Date: 11-04-2026 13:52:37

CERTIFICATE NO:
DIPP203406

सत्यमेव जयते

Government of India
Ministry of Commerce & Industry
Department for Promotion of Industry and Internal Trade

#startupindia

CERTIFICATE OF RECOGNITION

This is to certify that ***SRJX RESEARCH AND INNOVATION LAB LLP*** *incorporated as a* ***Limited Liability Partnership*** *on* ***05-05-2025****, is recognized as a startup by the Department for Promotion of Industry and Internal Trade. The startup is working in 'Professional & Commercial Services' Industry and 'Professional Information Services' sector as self-certified by them.*

This certificate shall only be valid for the Entity up to **Ten** years from the date of its incorporation only if its turnover for any of the financial years has not extended ₹ **100 Cr.**

14-05-2025
DATE OF ISSUE

Scan to Verify

04-05-2035
VALID UPTO

Digitally Signed By:
ANURADHA GUPTA
Date: 29-03-2026 14:19:01