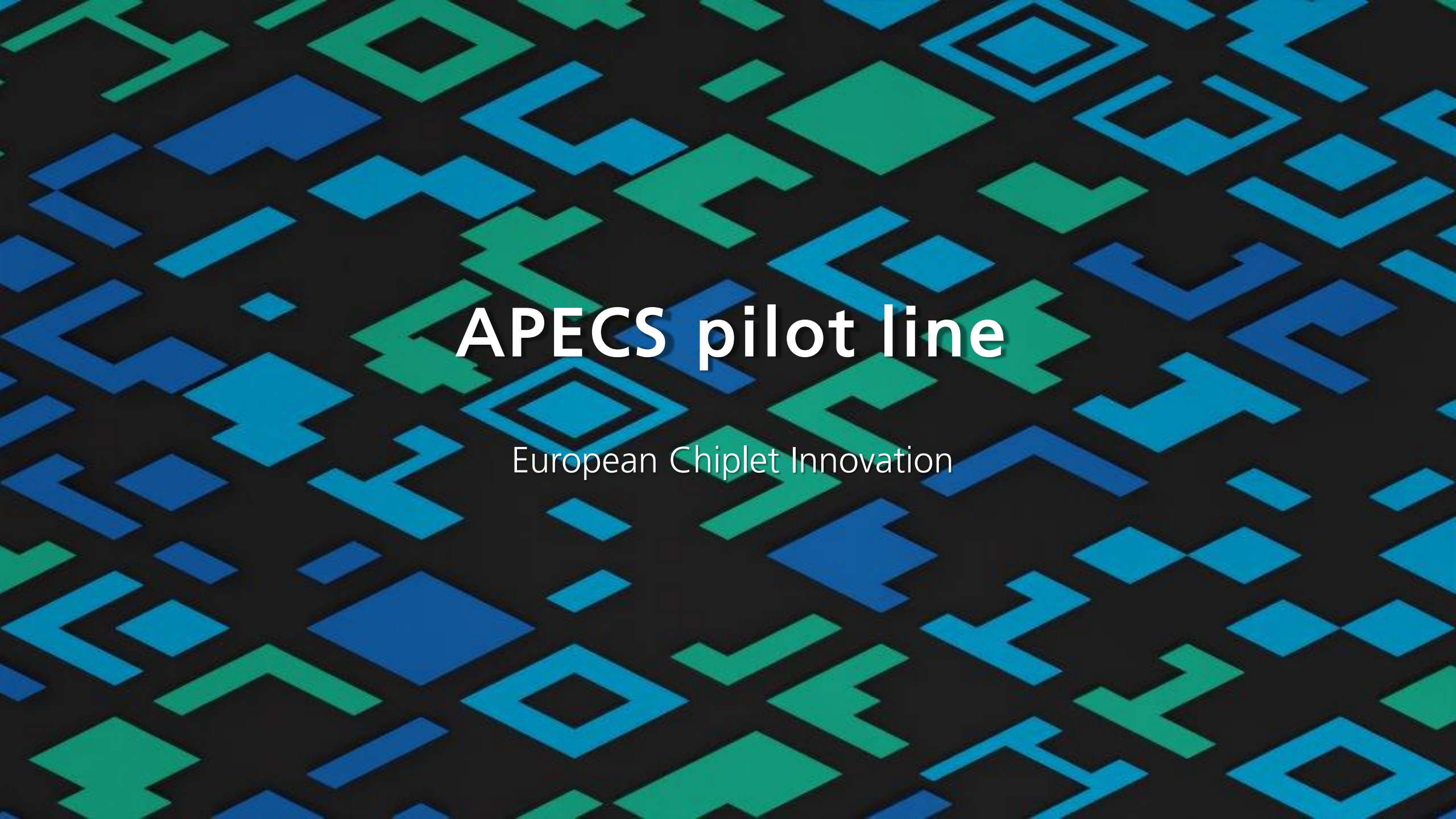




APECS pilot line

European Chiplet Innovation

Reshaping the European semiconductor ecosystem

EU Chips Act (2023):

- The EU Chips Act bridges the gap between the EU's advanced research and innovation capabilities and their sustainable industrial exploitation
- Ensures large-scale capacity building and innovation within the EU



Creation of innovative pan-European Pilot Lines by major European RTOs together with partners



5 innovative pilot lines for Europe



APECS pilot line: Coordinated by Fraunhofer and implemented by the FMD, dedicated to advanced packaging and heterogeneous system integration.



FAMES pilot line
led by CEA-Leti (France)



NanoIC pilot line
led by imec (Belgium)



PIXEurope pilot line
led by ICFO (Spain)



WBG pilot line
led by Consiglio Nazionale delle Ricerche (Italy)



Key Figures

1

Global semiconductor market:

- ~ USD 700 billion in 2025
- > USD 1 trillion by 2030

Market growth driven strongly by

- Computing and data storage (AI)
- Wireless communication
- Automotive electronics

2

✓ **Advanced Packaging** paves the way to overcome the limitations of Moore's Law

✓ Total semiconductor packaging market:

- ~ USD 70 billion by 2030
- ~ 50% Advanced Packaging market share today

✓ Asia-Pacific holds strong packaging ecosystems

3

Europe's growing semiconductor demand is increasingly shaped by **Compound Semiconductors** (power electronics & photonics) & **Advanced Packaging**

What are the challenges in heterogeneous integration?

Design complexity

- Integrating different materials (CMOS, InP, GaAs, SiPh)
- Managing electrical and optical coupling
- Ensuring co-design efficiency and thermal stability

Manufacturing precision

- High density interposers (organic/inorganic)
- Sub-micron alignment
- Controlling process variations
- Enabling stress-free bonding
- New testing concepts

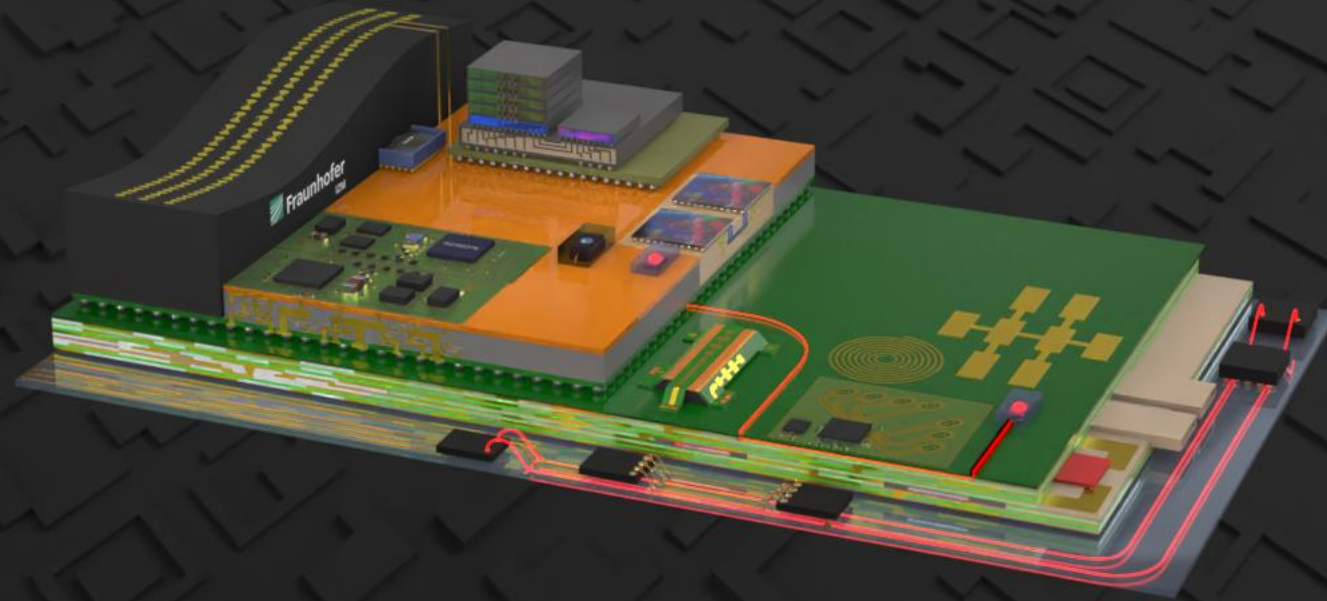
Standardization

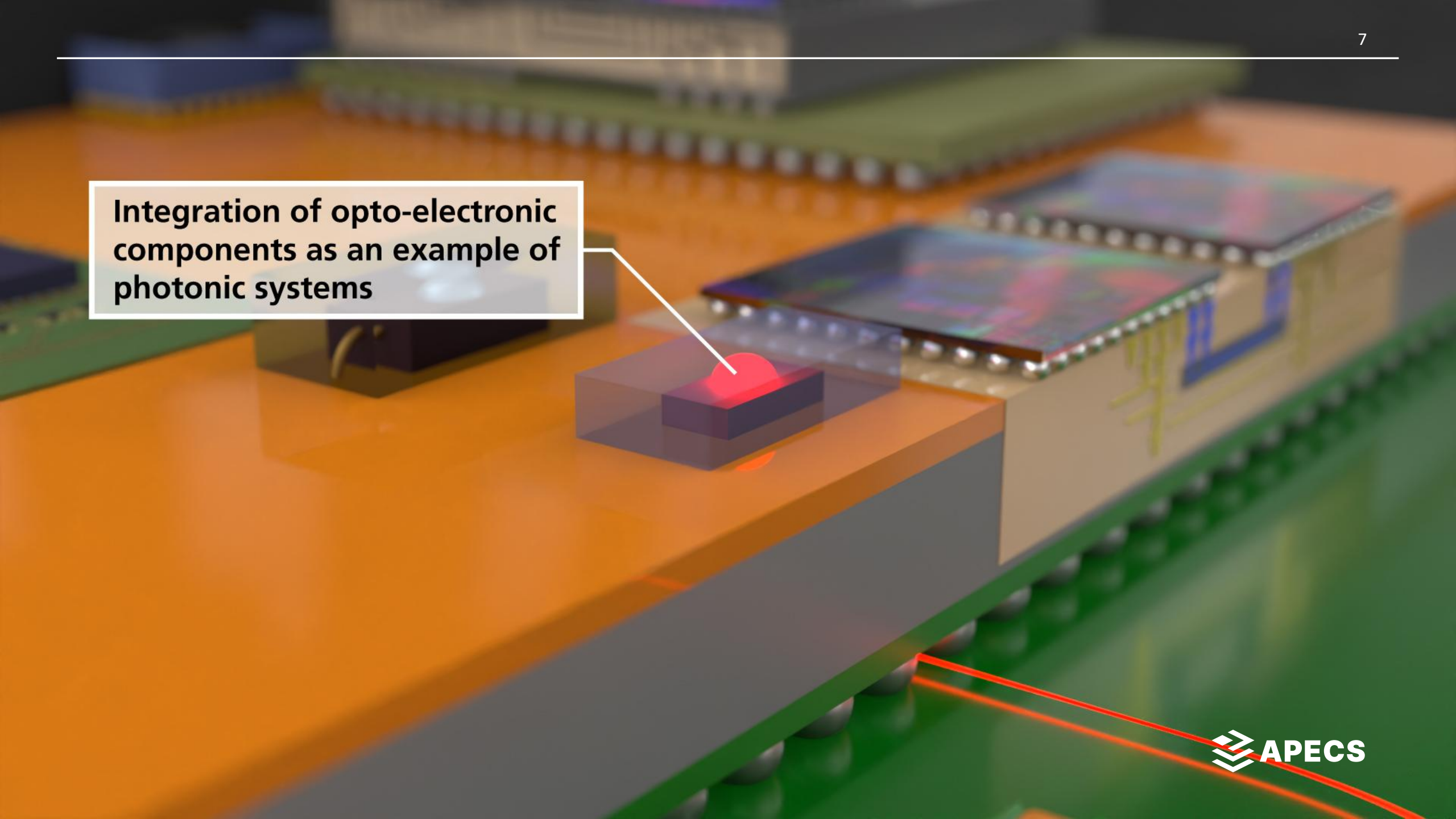
- Defining universal design rules
- Standardizing interfaces
- Ensuring process compatibility
- Establishing reliability benchmarks

Cost management

- Reducing fabrication costs
- Improving yield
- Scaling automated assembly
- Minimizing supplier dependency

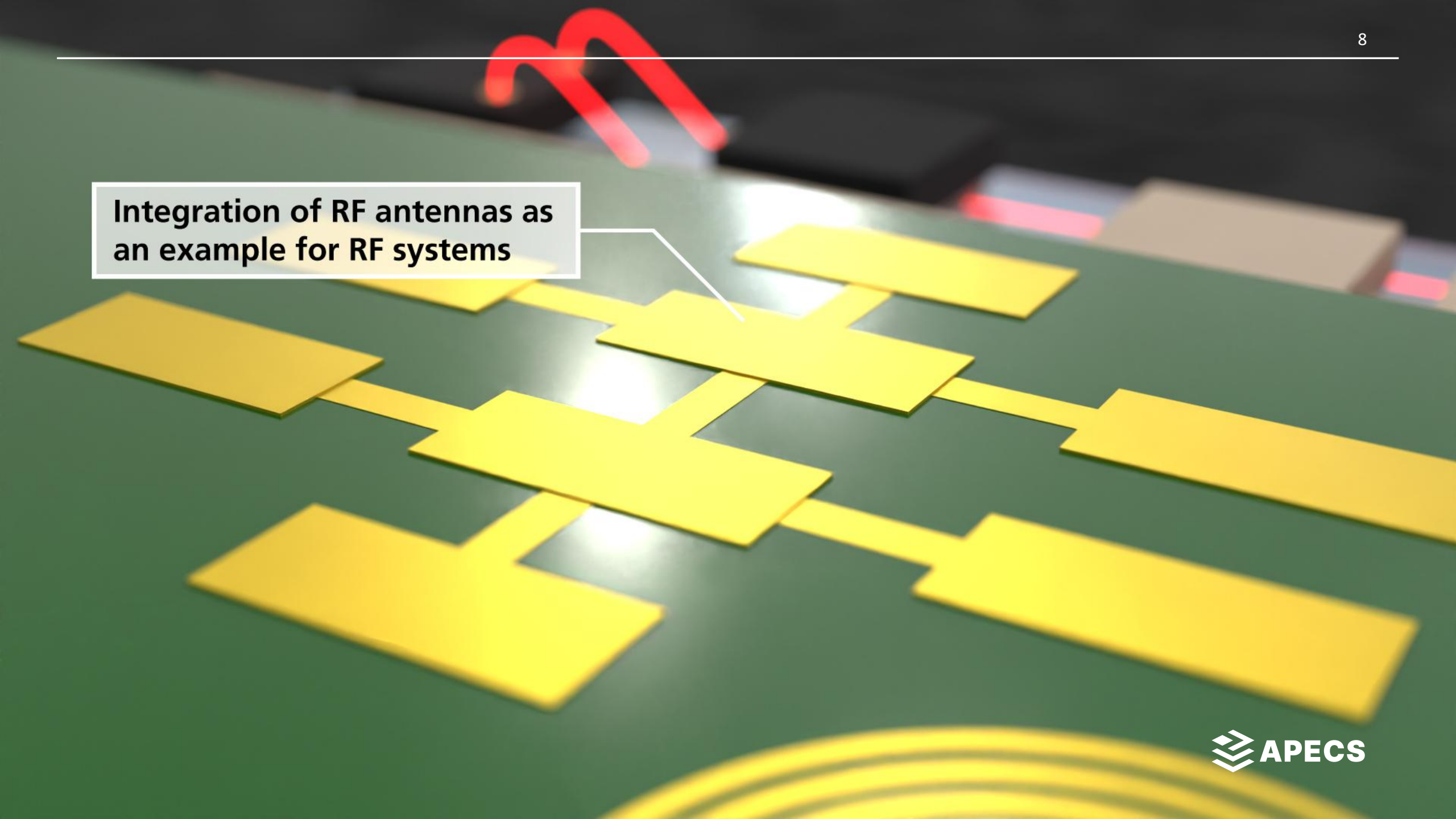
Illustration of possibilities and the complexity of advanced heterogeneous system integration and advanced packaging





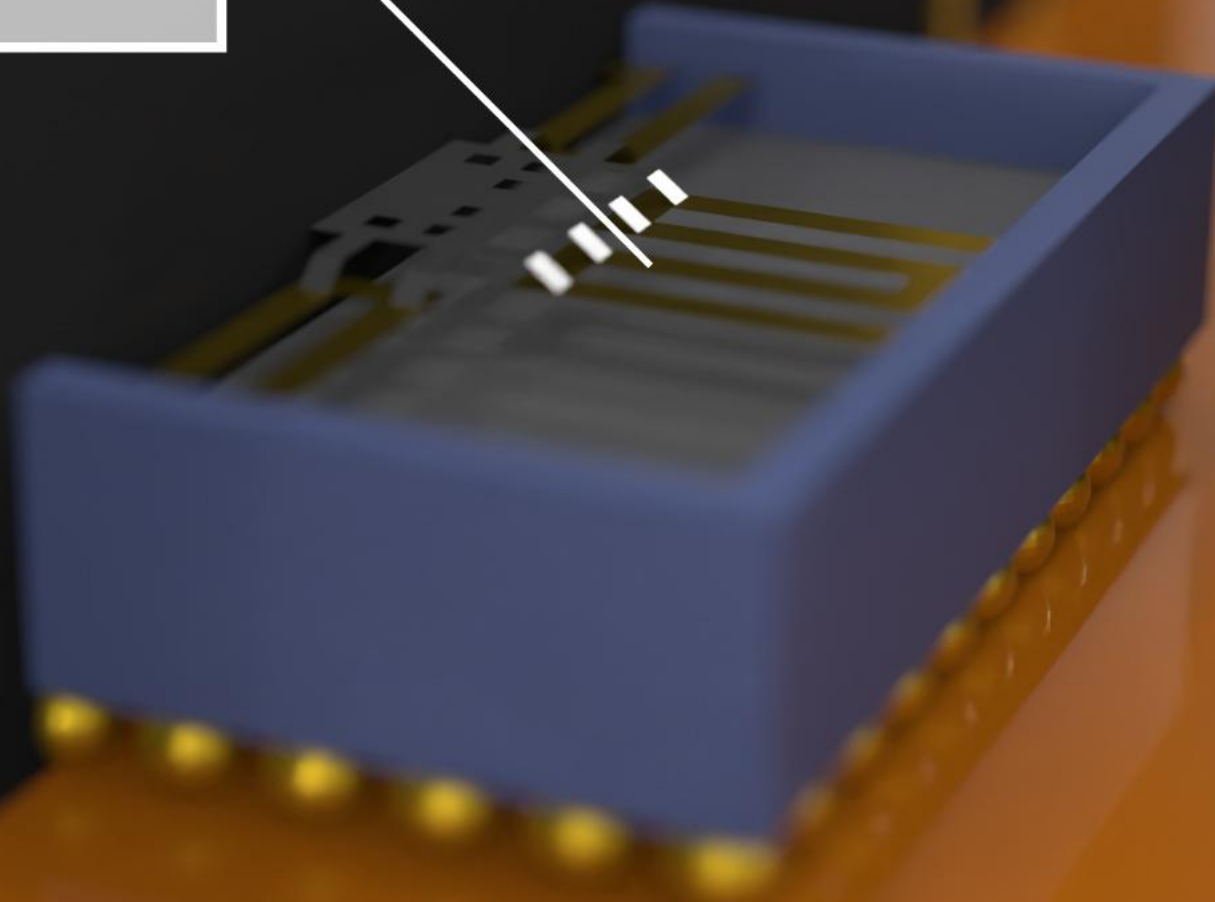
Integration of opto-electronic components as an example of photonic systems

This 3D rendering illustrates a complex photonic system. It features a central orange substrate with a grey waveguide structure. A red laser beam is shown entering from the bottom right, passing through a series of small grey spheres (likely waveguide components) and reflecting off a surface. A white callout box points to a small red component on the orange substrate. In the background, there are several rectangular components with colorful, iridescent surfaces, possibly representing different photonic materials or coatings. The overall scene is set against a dark background, emphasizing the components and the light path.

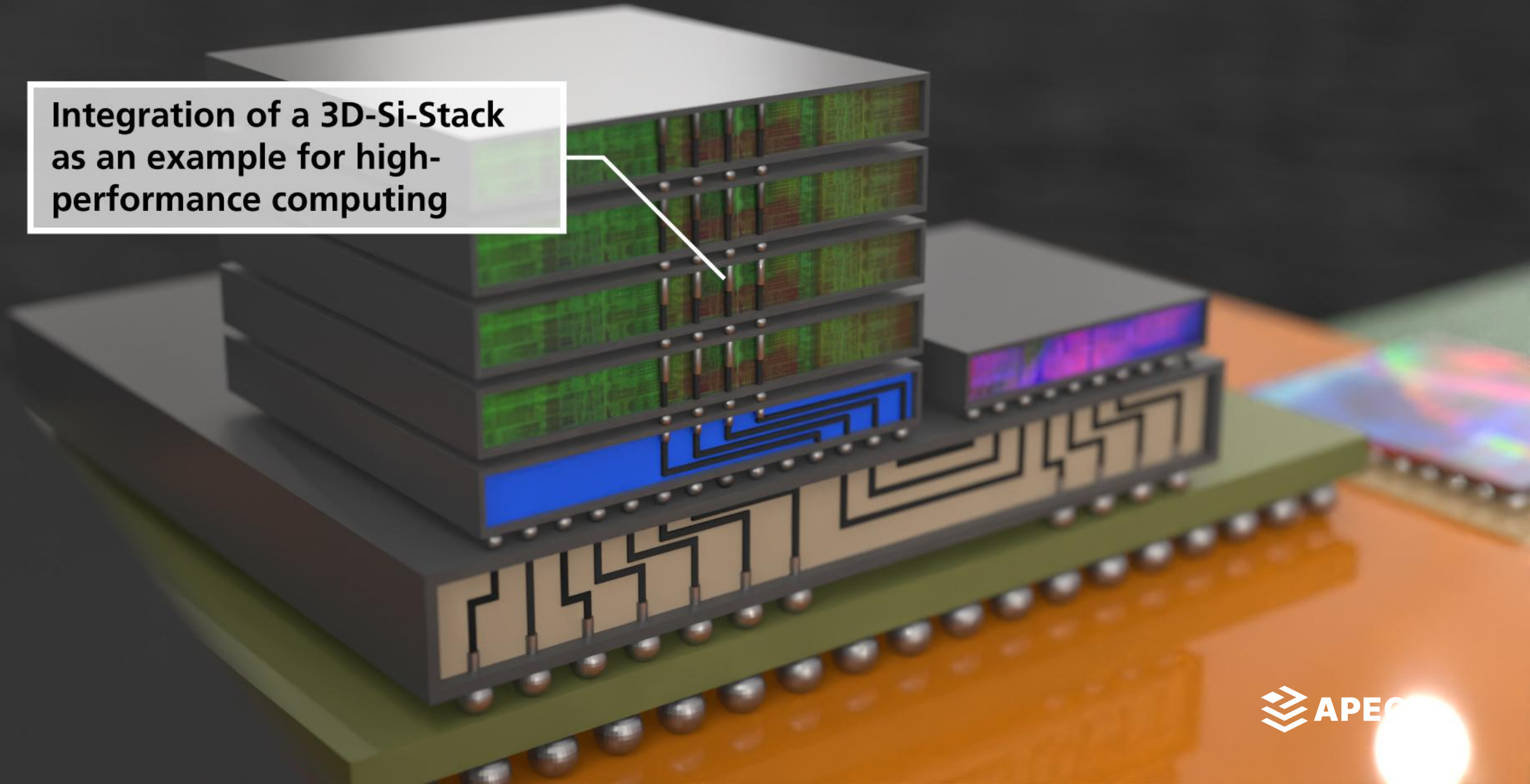


Integration of RF antennas as
an example for RF systems

Integration of components
for high-performance
sensing systems



Integration of a 3D-Si-Stack
as an example for high-
performance computing



Examples for the integration at wafer and substrate level

Integration at wafer level

Hybrid Cu/Cu bonds

HDML Si-Interposer

TF-embedded thin chip

3D-shaped mold cap

TSV/TGV/TPV

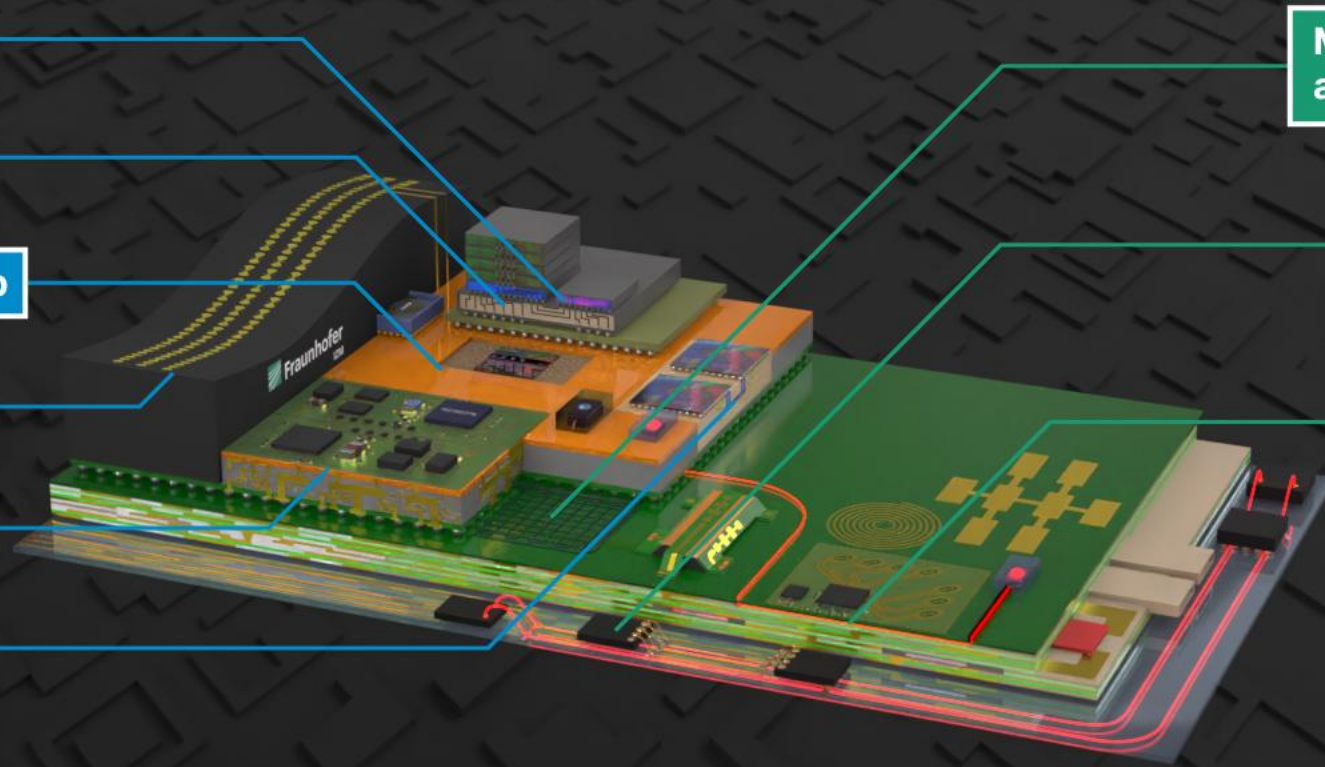
Embedded Si-bridge

Integration at substrate level

Metallic TF-on-organic anti-tampering structures

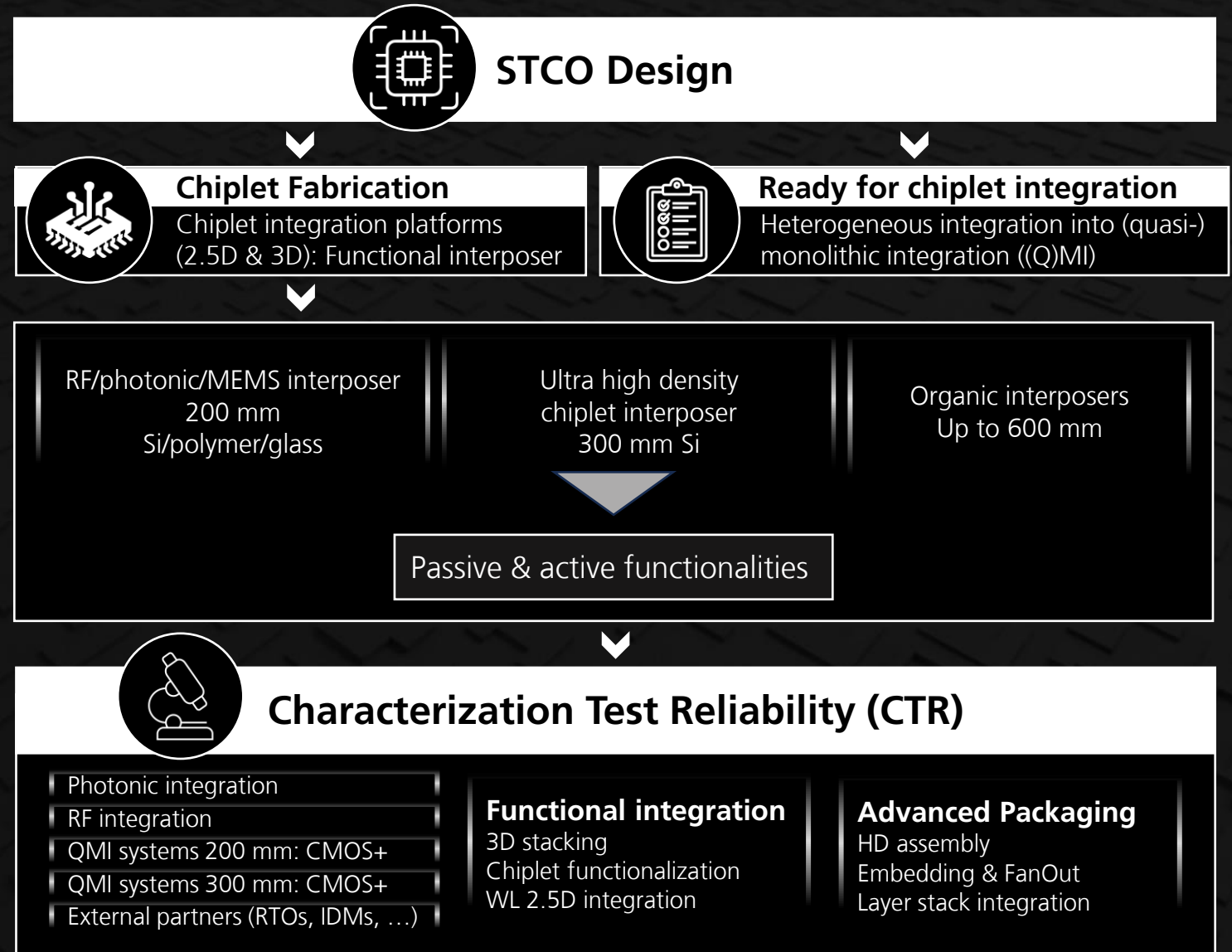
Embedded passives, chips or SiP module

Embedded optical waveguides



APECS brings the connection between design, technology and testing for wide range of applications

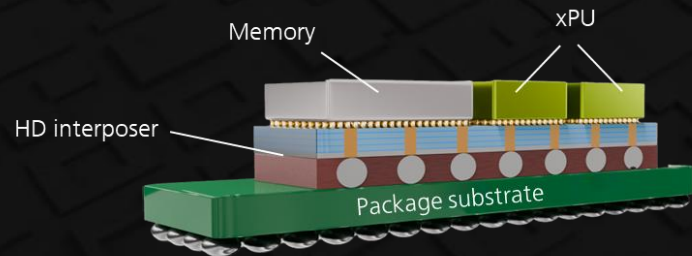
All the developments are taking place under the dictum of the European Green Deal.



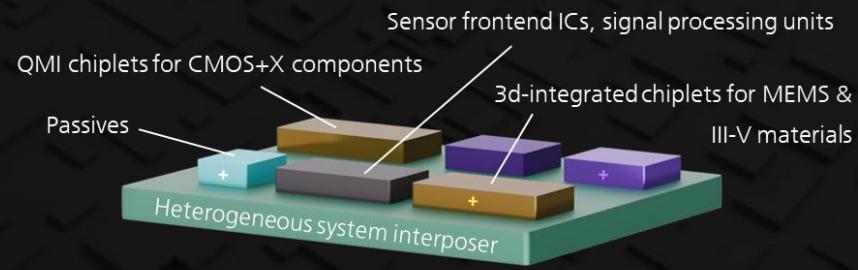
Demonstrators: Advanced Packaging solutions for various applications

- Demonstrating that the pilot line can seamlessly perform all conceivable process steps
- Showing possibilities of the pilot line, but do not deliver specific products

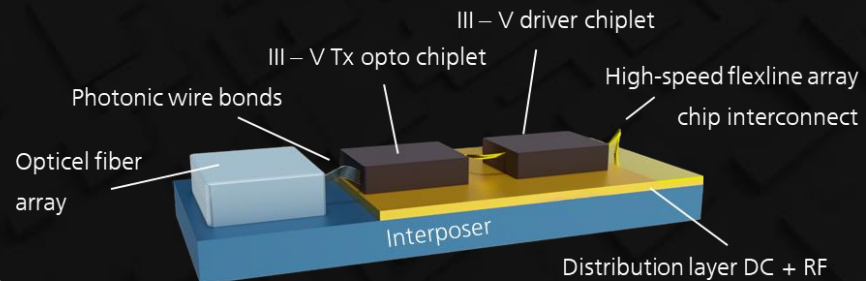
Demo 1 - High Performance Computing



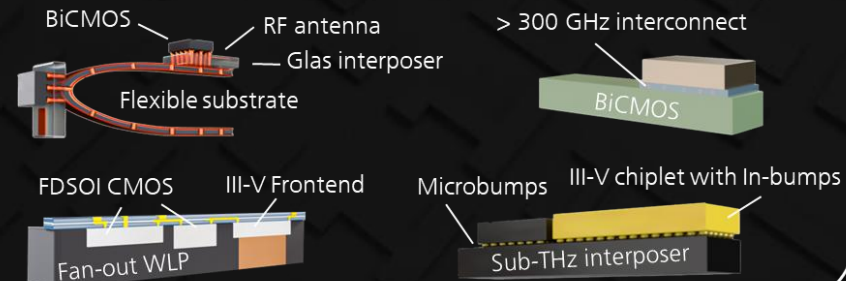
Demo 2 - Multi-Materials Sensors



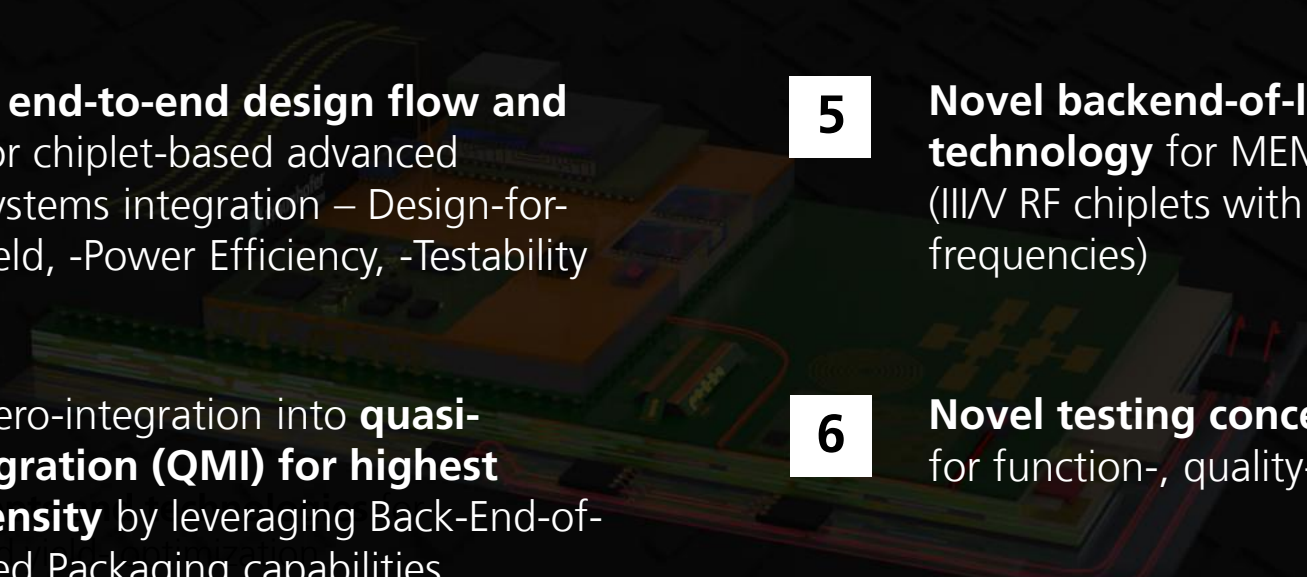
Demo 3 - Photonic Systems



Demo 4 - Modules for Radar and Mobile Communication



Key innovations of the APECS pilot line

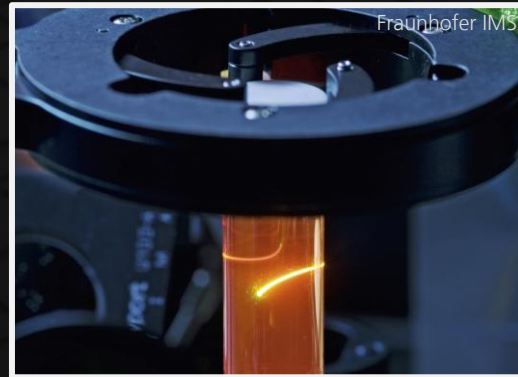
- 
- 1** Unique **chiplet integration platform** (2.5D and 3D) for multiple core technologies (CMOS, Opto/RF) and non-electronic devices (MEMS, Opto, OLED), leveraging the innovations of advanced packaging
 - 2** **Comprehensive end-to-end design flow and methodology** for chiplet-based advanced heterogeneous systems integration – Design-for-Performance, -Yield, -Power Efficiency, -Testability
 - 3** Expansion of hetero-integration into **quasi-monolithic integration (QMI) for highest performance density** by leveraging Back-End-of-Line and Advanced Packaging capabilities
 - 4** Prototyping of **high performance chiplet-based systems for specific needs of the European industries**, in particular, automotive, medical device and health care, sensors and advanced manufacturing industries
 - 5** **Novel backend-of-line interfacing technology** for MEMS, opto/RF chips (III/V RF chiplets with (Bi)CMOS for 300 GHz+ frequencies)
 - 6** **Novel testing concepts and technologies** for function-, quality- and yield- optimization

Application areas of the APECS pilot line



Fraunhofer IAF

High performance computing



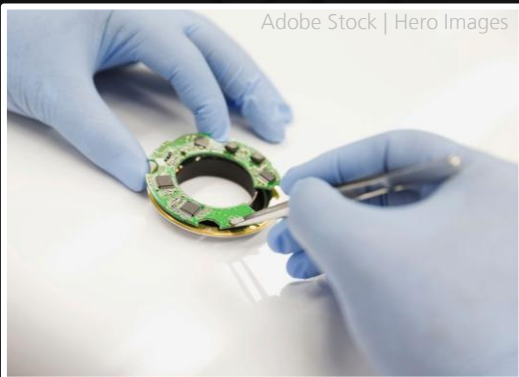
Fraunhofer IMIS

Sensor systems



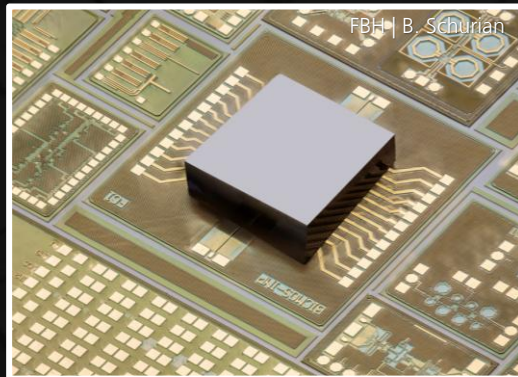
iStock | yoh4nn

Industrial manufacturing



Adobe Stock | Hero Images

Medical instrumentation



FBH | B. Schüran

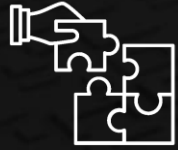
Telecommunications



Fraunhofer EMFT | B. Müller

AI/ Machine Learning

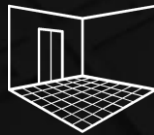
Research Fab Microelectronics Germany (FMD)



Strong Cooperation of
13 Fraunhofer and
2 Leibniz Institutes
under one virtual roof



> **5,400** employees,
including > **2,900** scientists
First patent applications: **191**
Active patent families: **2,986**



19,500 m² cleanroom space
ISO9001 Certification
1 MES over 10 institutes



2,200 tools/equipment
in **13 cleanrooms**

€ 2,2 bn

Assets/Investment

€ 673 m

Budget/a

€ 272 m

Industry Projects



FMD joins forces with Europe's leading RTOs

VTT: IPD and RF on silicon and glass substrates; Heterogenous 3D integration: ALD for TSV and Wafer Level and LTCC Packaging of RF and optical MEMS

imec: RDL 1st Chiplet Packaging Demonstrator and Chiplet Integration Package

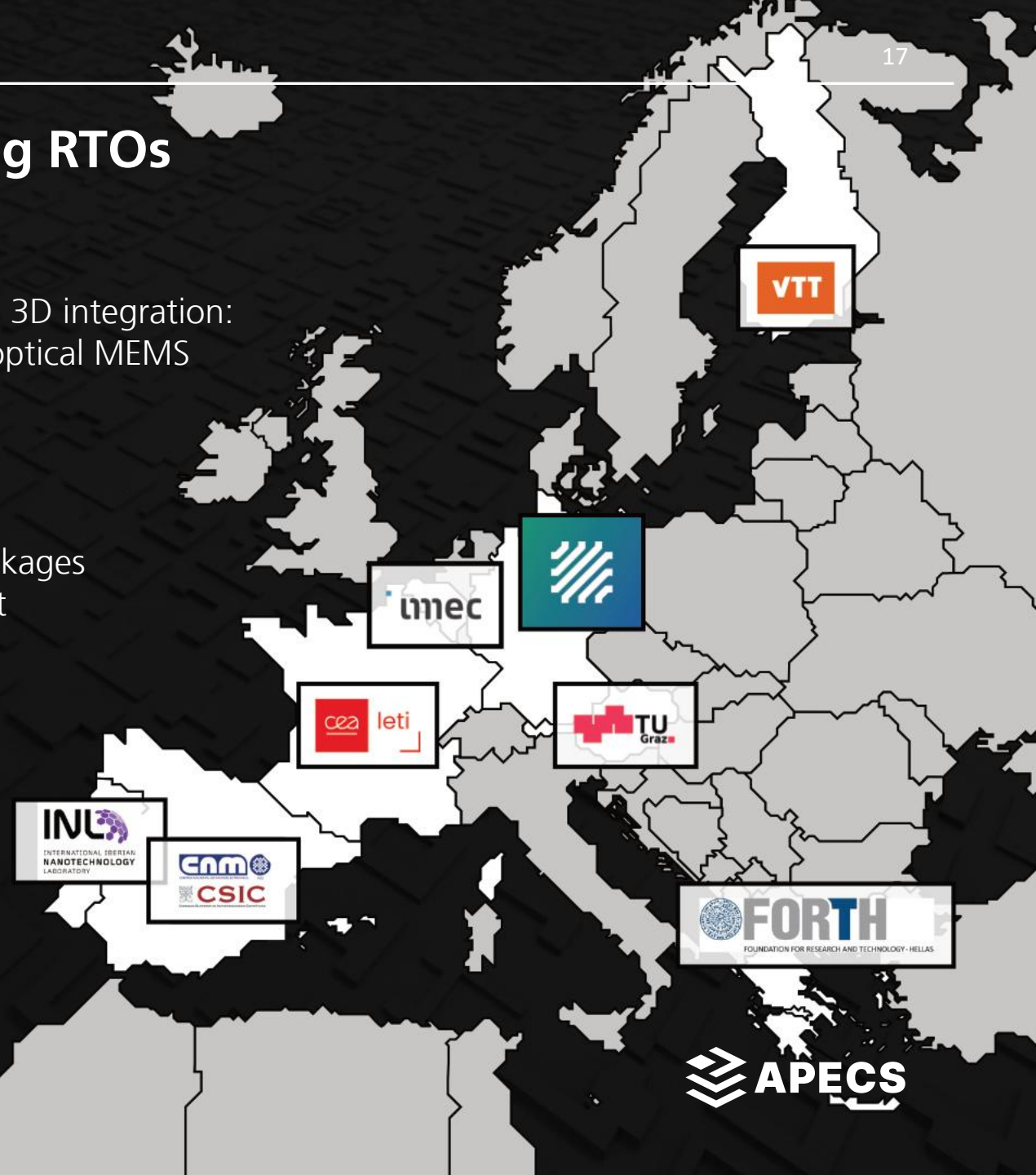
CEA-Leti: FOWLP technology for RF (>150GHz) System-in-Packages (SiP) and Glass substrates for > 100GHz RF passive component

TU Graz: ESD for heterogeneous integration

INL: 3D heterogenous integration of graphene FET biosensors

CNM/CSIC: Microchannel cooling, Printed antennas

FORTH: 3D Sequential Integration (3D SI) of GaN based RF front end (RFFE) chips



How to access APECS technologies: One-Stop-Shop



The new flagship event for microelectronics in Europe



What:

Two-day high-level event designed as a trend radar and a strategic meeting point for the European microelectronic industry

When:

September 30 – October 01, 2026

Where:

Berlin

Who:

over **500 participants** expected

Language:

English

Why:

Strategically shaping Europe's future with microelectronics



Coordinated by



Implemented by



Pilot Line Project Partners



Co-funded by



Co-funded by
the European Union

With funding from the:



APECS is co-funded by the European Commission and national ministries of the eight member states within the framework of the EU Chips Act. Overall funding for APECS amounts to € 730 million over 4.5 years.



Flanders
State of the Art





apecs.eu
experts@apecs.eu