NIRCA MkII based Front-End Electronics Breadboard Final Report

The NIRCA MkII Front-End Electronics Breadboard (FEE BB) project, developed by IDEAS AS under an ESA contract, marks a significant advancement in detector interfacing and data acquisition technologies. This initiative encompasses the design, manufacturing, and testing of a sophisticated electronics system intended to support high-performance imaging and sensor applications. Future Earth Observation mission studies have identified the need for high-frame rate, low noise, high dynamic range, 2D array detectors with high efficiency. Such missions could have scientific objectives, regard defense or other commercial applications, including agriculture.

At the heart of the FEE BB are two Near-InfraRed Control and Acquisition (NIRCA MkII) Application Specific Integrated Circuits (ASIC). The ASIC was developed by IDEAS under various ESA contracts and is currently undergoing space qualification. The NIRCA MkII is key for minimizing the size, weight and power (SWaP) of the readout electronics in infrared payloads.

An Engineering Model of the NIRCA MkII ASIC is shown in Figure 1 with its corresponding block diagram in Figure 2. In brief, the ASIC includes:

1. 16x Video ADCs sampling at up to 12 Msps.
2. 1x Housekeeping ADC for various monitoring of non-video analog signals.
3. 8x biases that can provide up to 100 mA current programmable from 0 – 3.3 V.
4. A sequencer that can be programmed using a microcontroller-like instruction set, controlling the readout of the ADCs and control sequence using the Sensor IO interface.

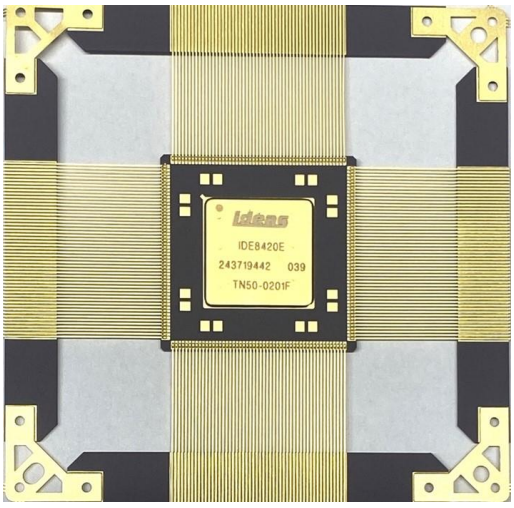

Figure 1 NIRCA MkII in a CQFP-208 package

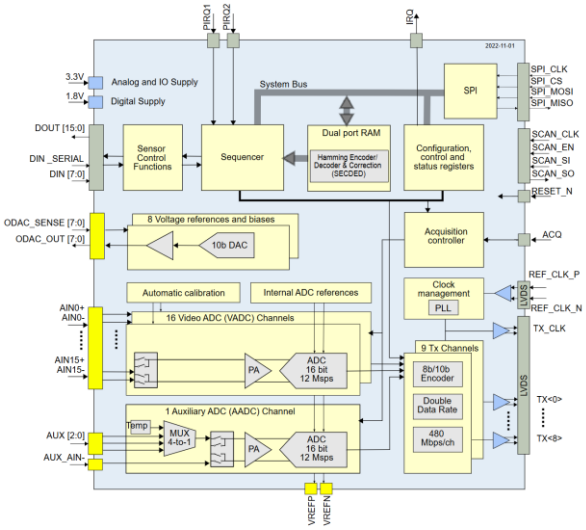

Figure 2 NIRCA MkII Block Diagram

The FEE BB is designed to a concept that uses the NIRCA MkII ASIC together with an FPGA, together with all required proximity electronics. The FEE BB FPGA is based on a System-on-Module that houses a Xilinx Zynq FPGA. Although the FEE BB uses a non-radiation hard FPGA, its design is transferable to several radiation-hardened FPGA families. The board otherwise uses space components. The board is engineered to offer a versatile platform for sensor integration. Its design includes the benefits of NIRCA MkII in addition to providing a robust SpaceWire control interface and CameraLink as data interface. A picture of the designed FEE BB is shown in Figure 3.

Tests were conducted through a comprehensive plan that included both simulation verification and laboratory validation measurements. The NIRCA MkII together with the FPGA design was verified using a SystemVerilog UVM-based testbench, ensuring that all functional blocks performed as intended.

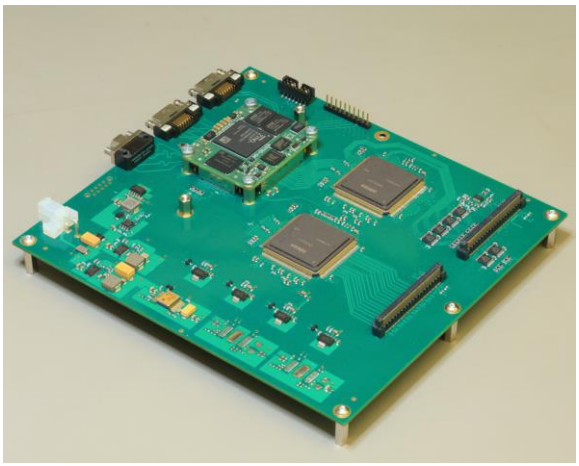

Figure 3 FEE BB

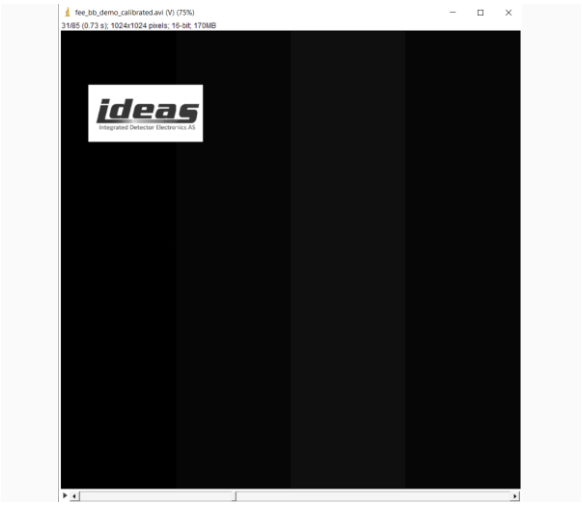

Figure 4 FEE BB readout from Detector Emulator

A Detector Emulator was also designed and played a central role in verification and validation by emulating the behavior of real analog-output sensors. The detector emulator can be modified to represent any 8 (or less) analog output sensor and can thus help for validation before real sensor integration. The Detector Emulator allowed for the generation of various test patterns and supported in detailed analysis of signal fidelity, and characteristics of input noise, crosstalk and settling. One of key achievements is illustrated in Figure 4, where the Detector Emulator was successfully controlled and read out by the FEE BB. The 1MPixel image is one of the frames in the video (.avi-format). Once the Emulator was correctly controlled by NIRCA MkII, it starts to send out analog data that is digitized by NIRCA MkII and passed onwards to the FPGA data handler and out over CameraLink in 16-bit data format. In this example, the Emulator was set in “movie-mode” where the IDEAS-logo moves around in the image. A scaled-up version demonstrating synchronization between two NIRCA MkII ASICs was also tested where 4x analog outputs of the Detector Emulator were routed to the primary NIRCA and 4x analog outputs were routed to the secondary NIRCA MkII ASIC. This demonstrates capability of scaling the FEE to read out 32 analog output image sensors. A picture of the FEE Detector Emulator is shown in Figure 5.

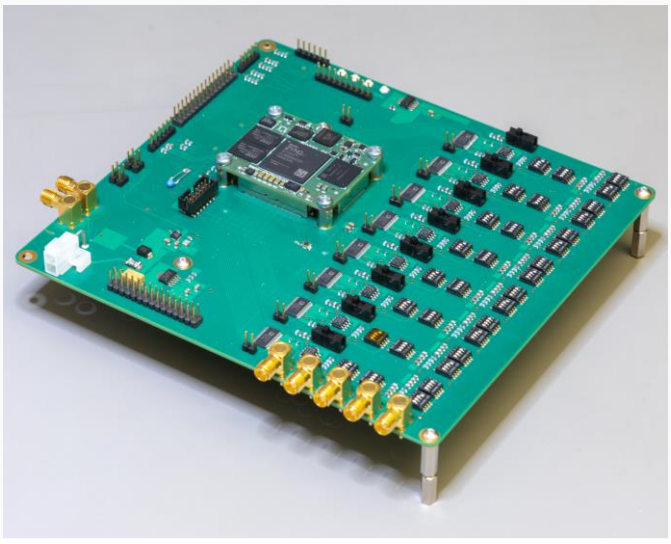

Figure 5 FEE Detector Emulator

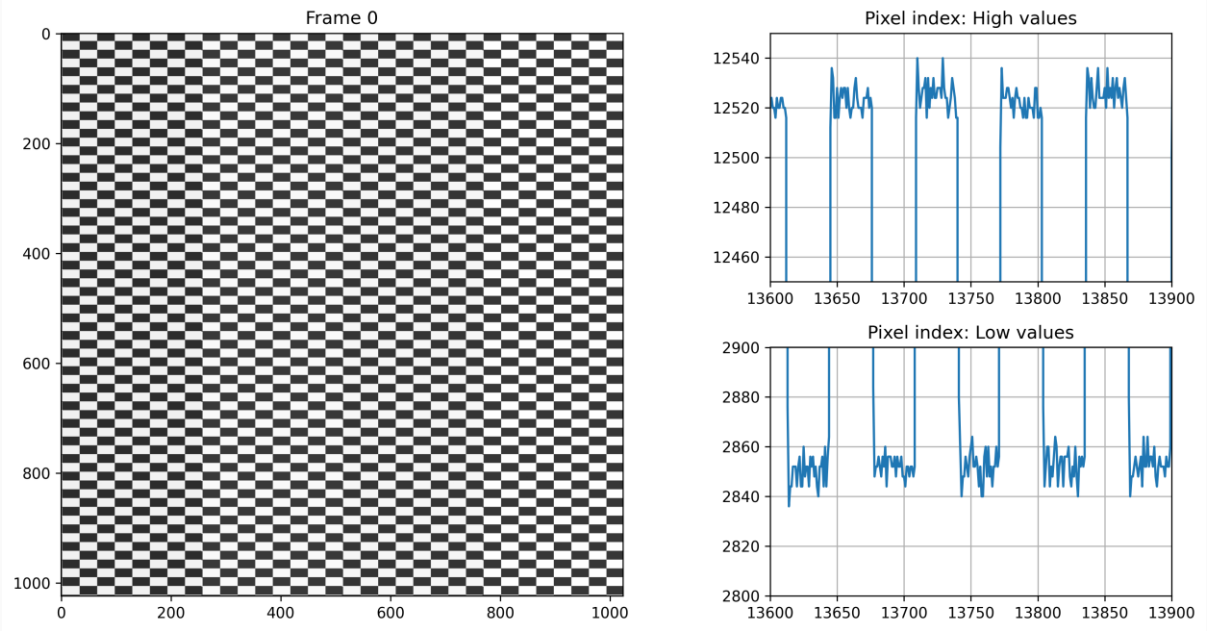

Figure 6 FEE BB readout of Detector Emulator is chess-mode.

Another example illustrating one of the achievements achieved in this project is shown in Figure 6. The Detector Emulator was configured to chess-mode. The chess-pattern contains low (dark, 2850 ADC LSB) and high level (light, 12525 LSB) regions. The system was set to sample at 12 Msps. On the right-hand side in the image, we see 300 pixels in an arbitrary row in the image. The measurements demonstrate good settling for the complete test setup with the FEE BB including the Detector Emulator.

Overall, the NIRCA MkII FEE BB project demonstrates a successful integration of advanced electronics design, precise manufacturing, and rigorous testing. It lays a strong foundation for future models, including the ongoing development of the FEE engineering model. IDEAS believes the FEE has reached Technology Readiness Level 4 (TRL 4).