Technolution

How RISC-V Will Set You Free

FreNox RISC-V - flexible & portable solutions

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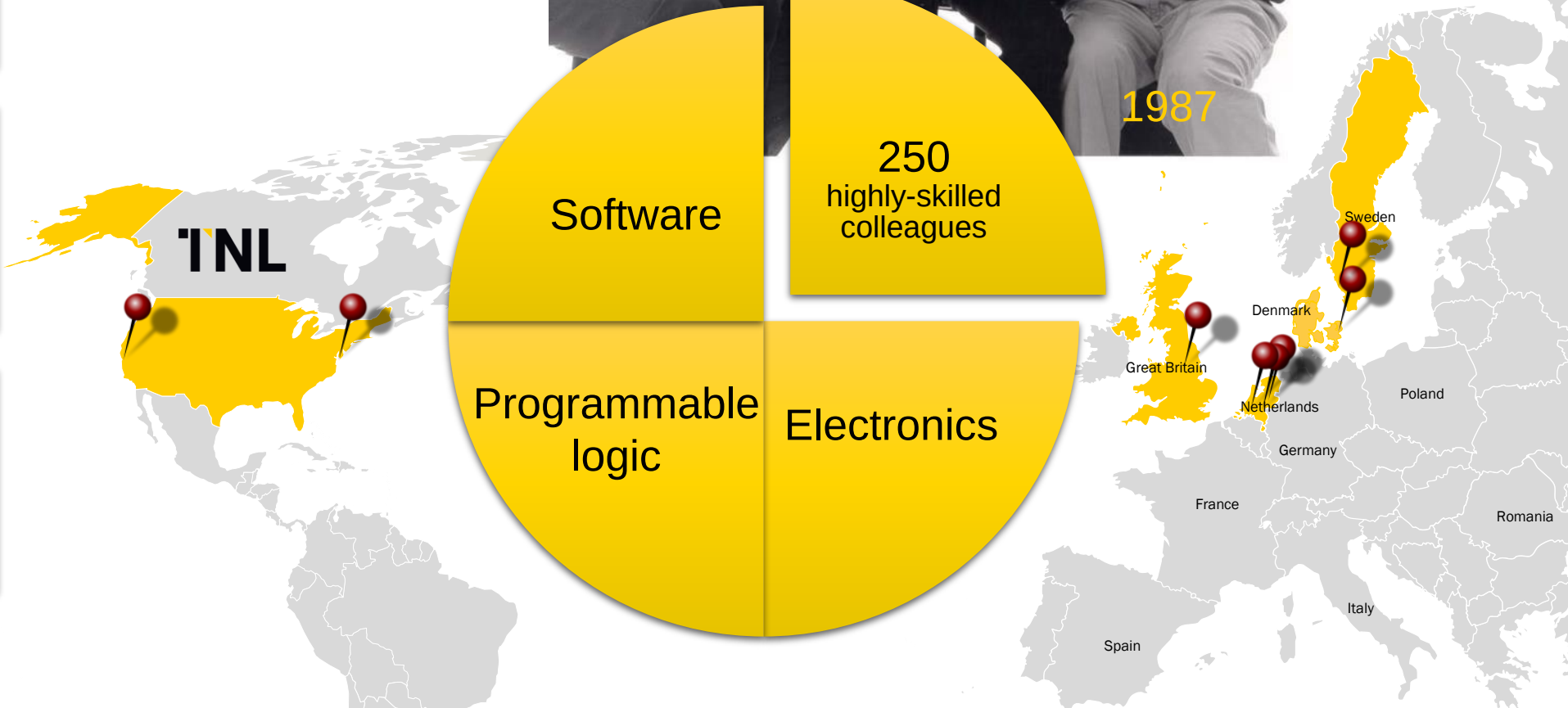
Redefining **solutions**

About Technolution

Passion for technology

Solutions that matter

Reliable technology



Software

250 highly-skilled colleagues

Programmable logic

Electronics

Technolution Advance
High-tech & big science

Technolution Prime
Security

Technolution Perform
Manufacturing

High-speed data
acquisition & control

Classified
line encryption

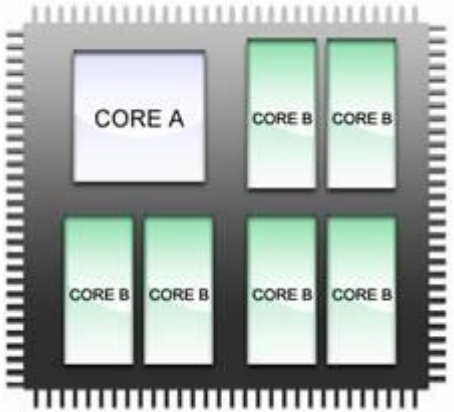
Fully automated
packaging machine

= open standard; ≠ open source

Redefining
solutions

Flexibility & Portability

- Heterogeneous systems



- Hybrid solutions
  - Control flow in software
  - Data flow in hardware
- Security, safety & reliability
  - separation of concerns,
  - by executing each software component,
  - on multiple isolated cores in mixed criticality systems

Flexibility & Portability

- Technology agnostic platform development
  - Target multiple FPGA vendors

intel XILINX Microsemi a Microchip company NanoXplore

⇒ NIOS II soft processor (Intel)

⇒ MicroBlaze soft processor (Xilinx)

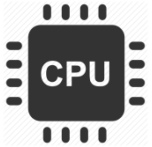
- Our RISC-V processor IP allows for portability without vendor lock-in
  - Re-using hardware sources ⇒ same processor
  - Re-using software tools ⇒ same compiler
  - Re-using software sources ⇒ same software

So RISC-V®...

- Offers open standard collaboration
  - Default instruction set
  - Default instruction set extensions
  - Custom instruction extensions
- Embraces a rich eco-system
- Implies:
  - Flexibility
  - Portability
  - Transparency

- **FreNox** RISC-V IP
  - RISC-V processor family, 100% developed by Technolution
  - No dependencies on open-source implementations
  - Implemented in intel XILINX Microsemi NanoXplore

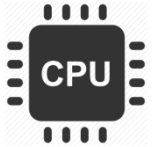
Technolution
FOUNDING
Co-founder of the RISC-V® Foundation



FreNox-E

Embedded processor

- hardware
  - RV32I(M)
  - 32bits, mul/div
  - 5 stages - Harvard arch
  - cache or internal RAM
  - IO space
- software
  - Bare metal
  - FreeRTOS
  - ThreadX



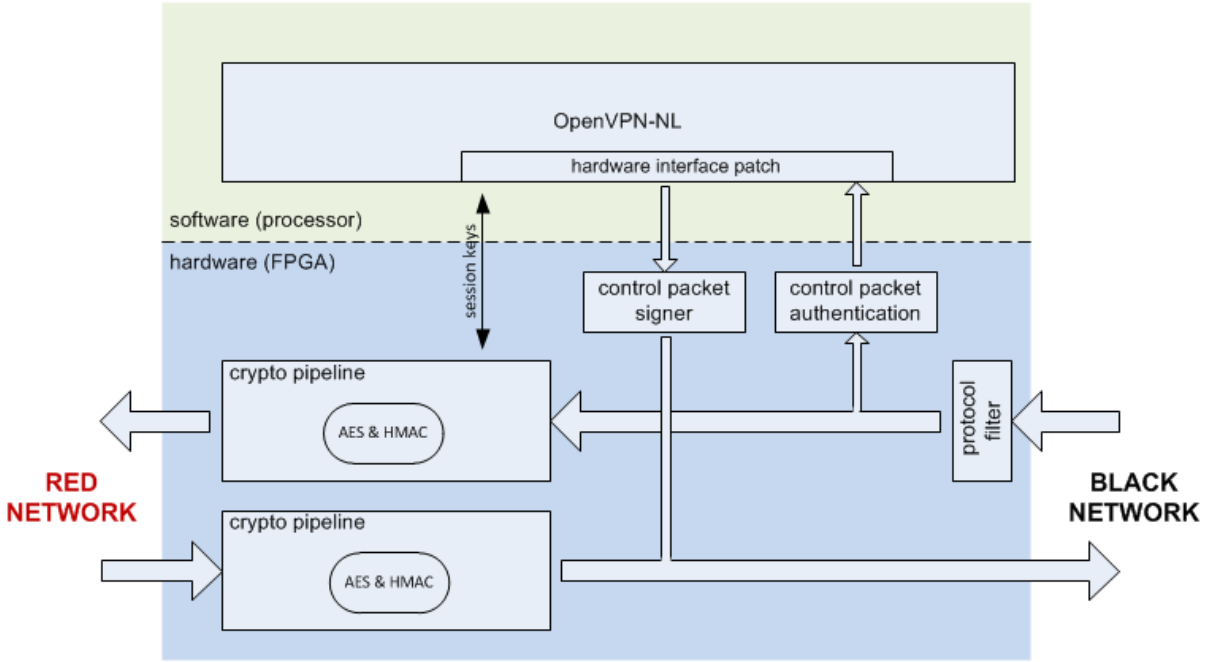
FreNox-S

Application processor

- hardware
  - RV32IMAS
  - 32bits, mul/div, atomic, supervisor
  - 5 stages - Harvard arch
  - iMMU, dMMU (1 - 128 entries)
  - 8 way associative cache (4 - 32k)
  - cache coherency (DMA)
  - IO space
- software
  - Linux
  - Buildroot

Secure line encryption

- Hardware VPN solution (NATO/EU Restricted)
  - Control flow in software / RISC-V®
  - Data encryption in hardware logic



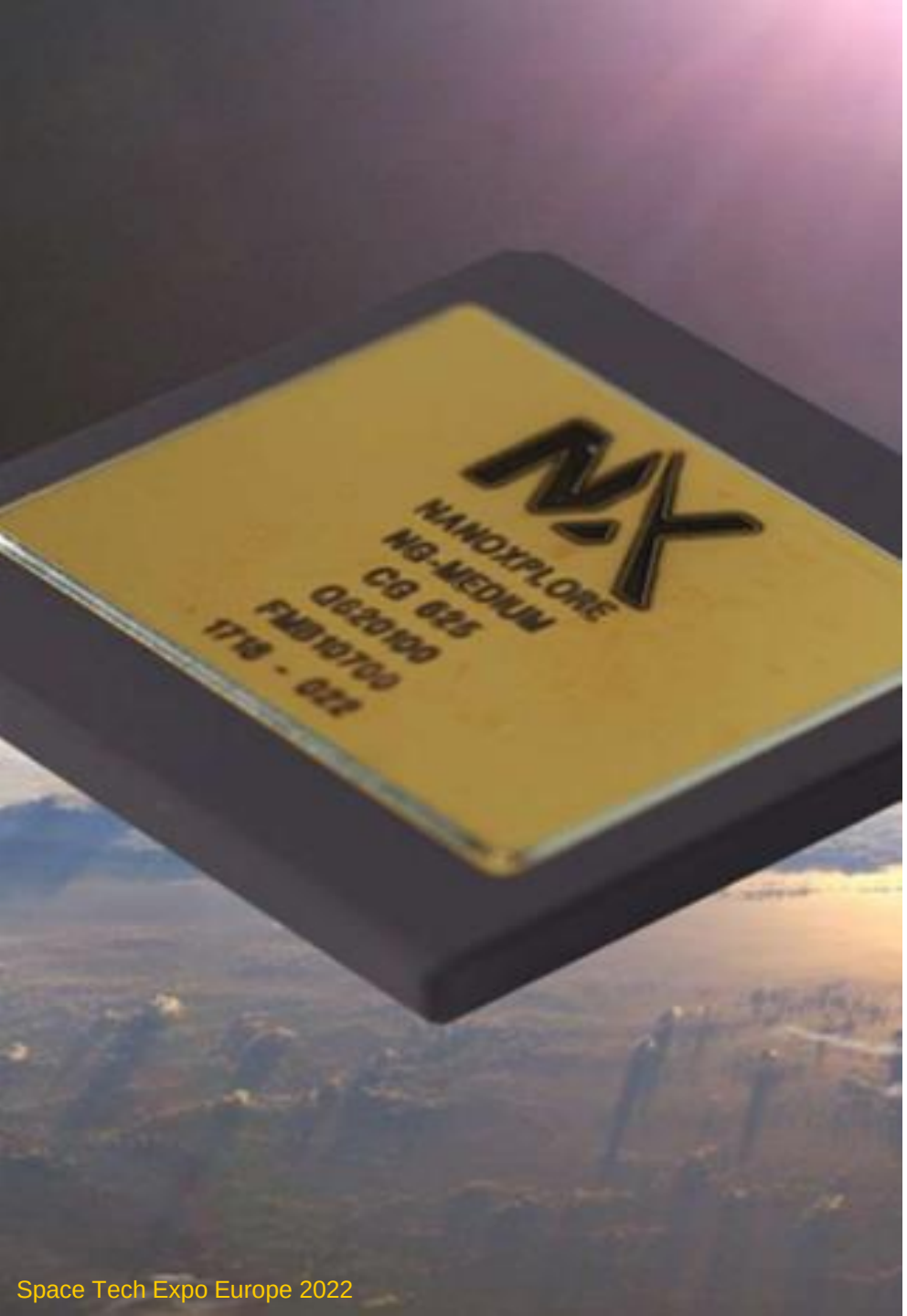
Secure line encryption

- Hardware VPN solution (NATO/EU Restricted)
  - Control flow in software / RISC-V®
  - Data encryption in hardware logic

⇒ Full understanding of our custom implementation

⇒ Transparency for customer/evaluator

⇒ Lifecycle management (transparency & portability)

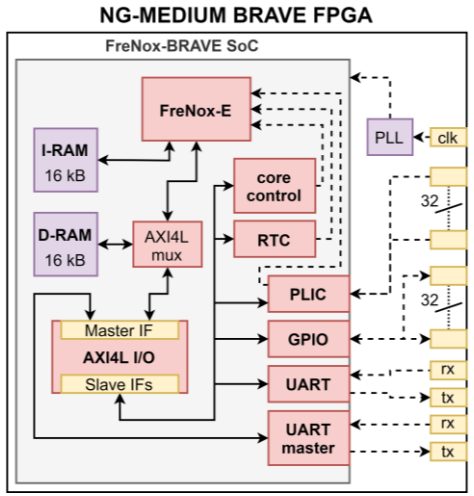


Radiation hardened FPGA

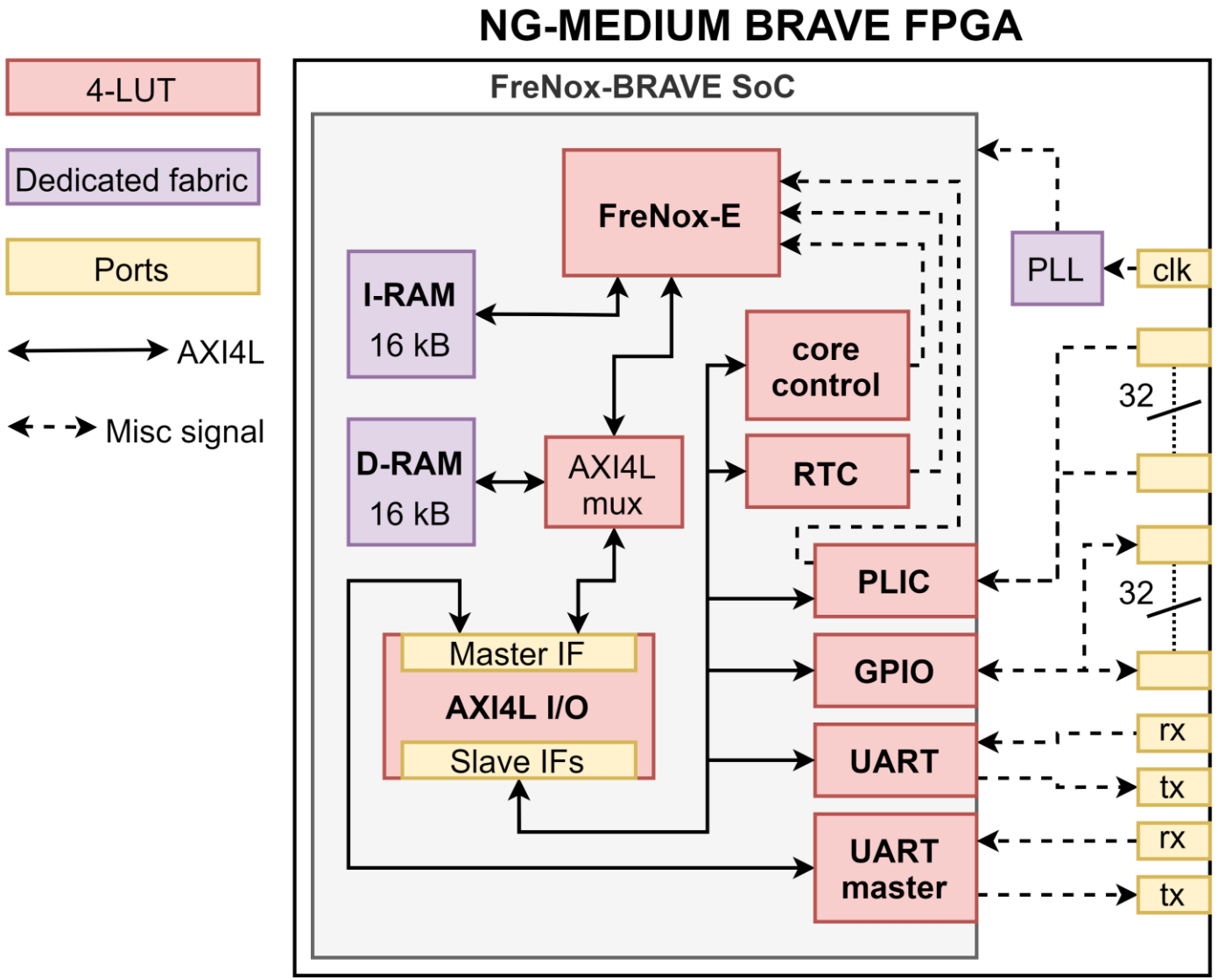
- Europe needs non-dependent access to critical space technologies
  - European radiation-hard FPGA

NanoXplore

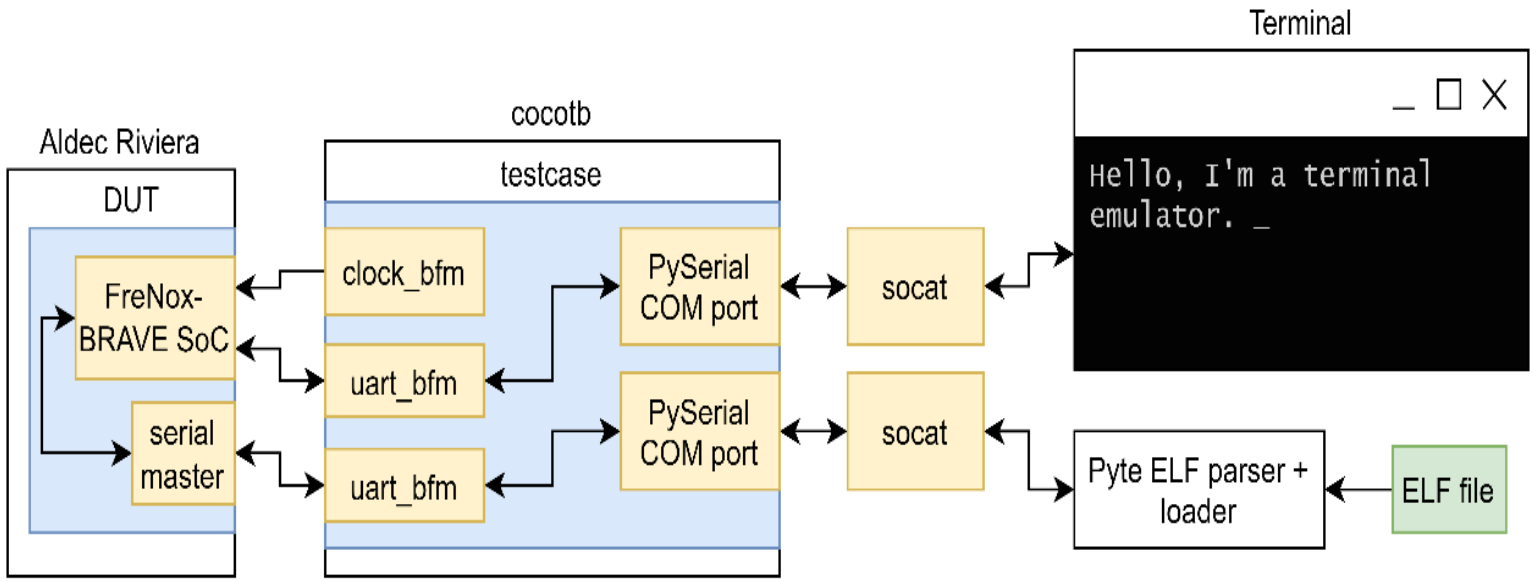
- **FreNox-E** SoC implemented and demonstrated in NG-Medium RH-FPGA



FreNox-E full System-on-Chip



FreNox-E verification & validation



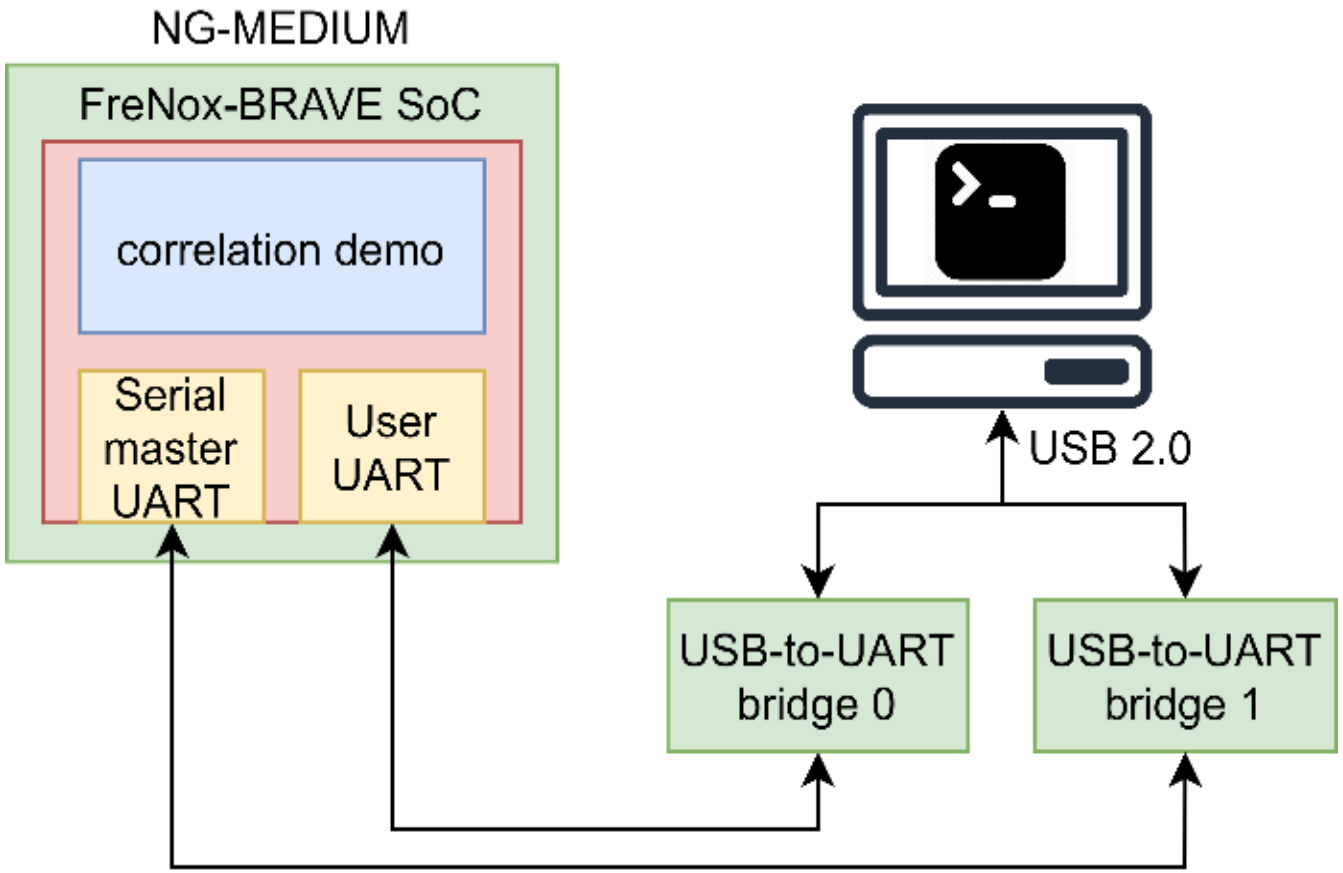
Verification by simulation

- Continuous Integration
  - Reliability, Repeatability, Predictability
  - Automated regression testing

Shift-left tested FPGA designs

Technolution webinar – click here

FreNox-E verification & validation



Validation by implementation

- NG-Medium RH-FPGA

FreNox-E benchmarks

	FreNox-E @25 MHz
Dhrystone iterations/s	42221
DMIPS	24
DMIPS/MHz	0.96
CoreMark iterations/s	46
CoreMark/MHz	1.84

NG-Medium

4-LUT	DFF	BRAM	Clock
4992	3204	583.168 bits	31.5 MHz

Intel Cyclone V

ALMs	Registers	BRAM	Clock
3313	3770	295.168 bits	97.5 MHz

How RISC-V Will Set You Free

- **FreNox** RISC-V softcore
  - RISC-V processor family, 100% developed by Technolution
  - No dependencies on open-source implementations
  - Implemented in

- Rich eco-system ⇒ wide adoption of tools & software
- Flexibility ⇒ application customization
- Portability ⇒ lifecycle management
- Transparency ⇒ verification, validation & certification

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