UFUK AVRUPA

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WORKSHOP NAME: Digital, Chips and 6G

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REPUBLIC OF TÜRKİYE MINISTRY OF INDUSTRY AND TECHNOLOGY

TÜBİTAK

Advanced Microelectronics in ever more Applications
Understand Chip – Package – Board/System

Klaus Pressel

April 10th, 2025

Today‘s 7 Messages (Session: Digital, Chips and 6G)

- Growing Importance of Microelectronics (Megatrends)
- System Integration Everywhere (Assembly & Packaging, Heterogeneous Integration, Chiplets)
- Coherent View of Chip-Package-Board/System (from nm on Chip level to mm/cm on Board/System level)
- Understanding of Customer Requirements (e.g. Reliability Constraints)
- New Opportunities of Computer and Data Science/Management
- Management of Complexity
- European and National Funding Opportunities for Micro/Nanoelectronics

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We need Knowledge Generation

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Global Megatrends
Increasing Importance of Semiconductors

- **Energy Efficiency**
- CO_2 Emission
- …

Climate change and resource scarcity

- Infrastructure and **Mobility**
- Energy Consumption
- …

Demographic and social change

- Mobile Technologies and Social Media
- **Security**
- …

Digital transformation

- **IoT and big data**
- Infrastructure
- …

Urbanization

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Increasing Importance of Semiconductors

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- CO_2 Emission
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Digital transformation

- **IoT and big data**
- Infrastructure
- …

Urbanization

We must consider sustainability (recycle, reuse, refurbish, reliability, ……)

Semiconductors
Key Building Block for Megatrends

Energy efficiency	▪ Power Generation (renewable) ▪ Energy Transmission ▪ Energy Storage	▪ Energy Usage ▪ Energy Distribution
Mobility	▪ Electro Mobility ▪ Automated Driving	▪ Charging Infrastructure ▪ Infotainment
Security	▪ Authentication for IoT ▪ Mobile Devices	▪ Smart Cards ▪ Connected Vehicles
IoT and big data	▪ Human-Machine Interaction ▪ Data & Communication Infrastructure	▪ Edge Computing

→ System Integration & deep knowledge about materials & interfaces are the toolkits

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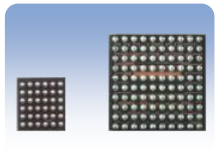
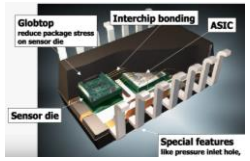
System in Package Integration Everywhere

(see also IEEE HIR roadmap https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html)

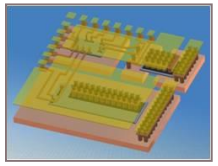
Communication and Computing



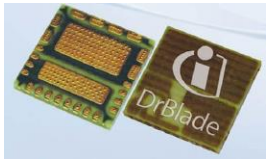
Automotive Electronics



Energy Generation and Energy distribution
(e.g. smart grid)



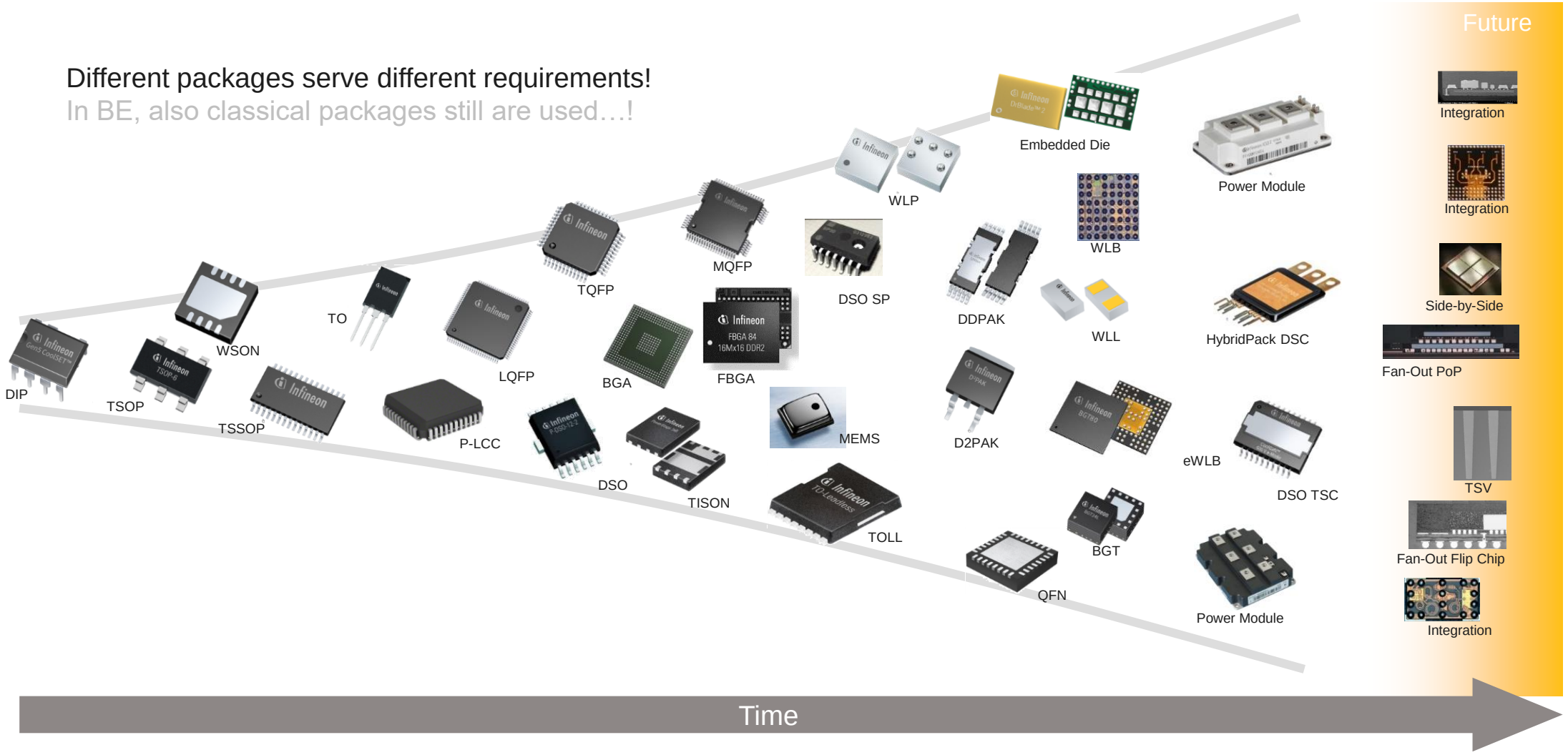
Industrial Electronics
(e.g. energy efficient driver, IoT, Industry 4.0)



Others
e.g. Solid State Lighting, medical, drones, …

Package Diversity is Growing Over Time
Infineon View

Different packages serve different requirements!
In BE, also classical packages still are used…!



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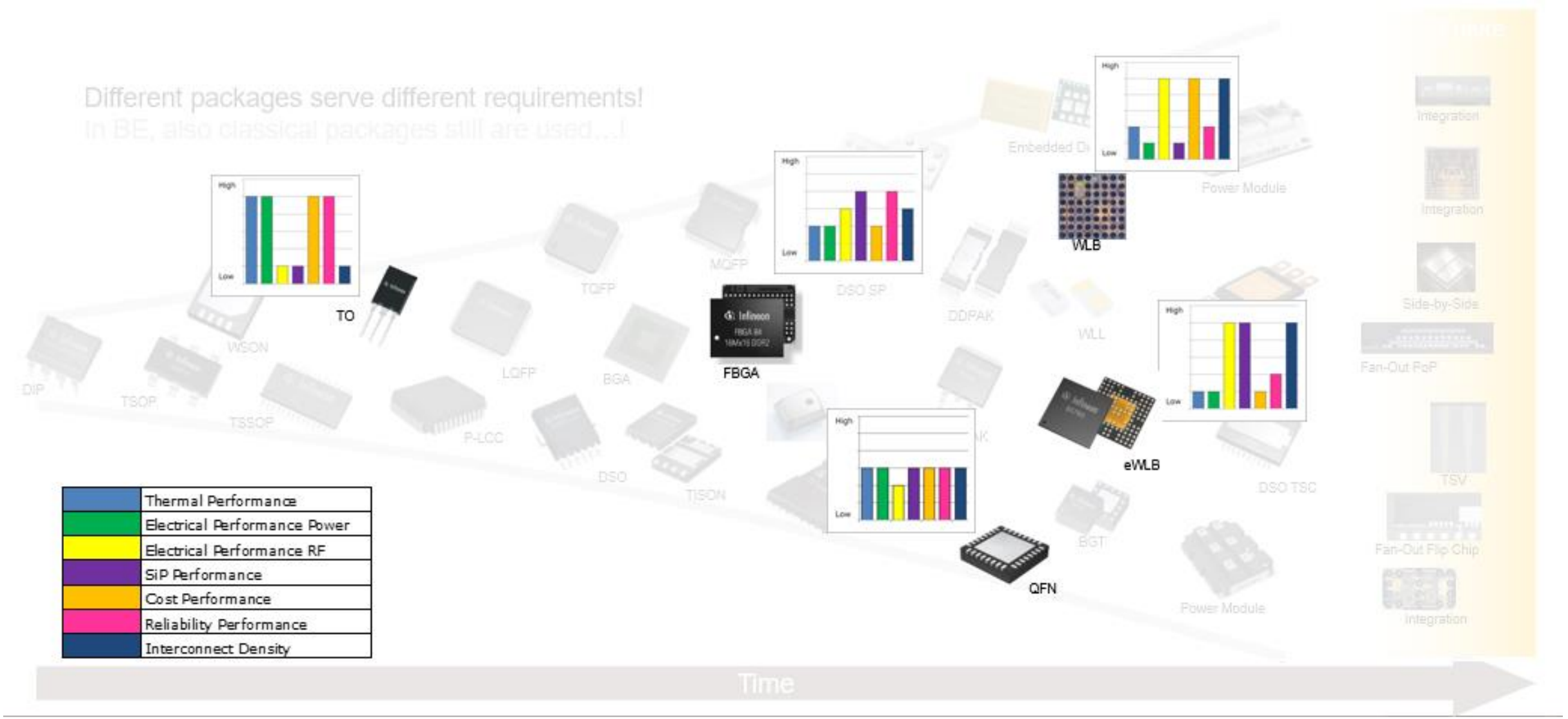

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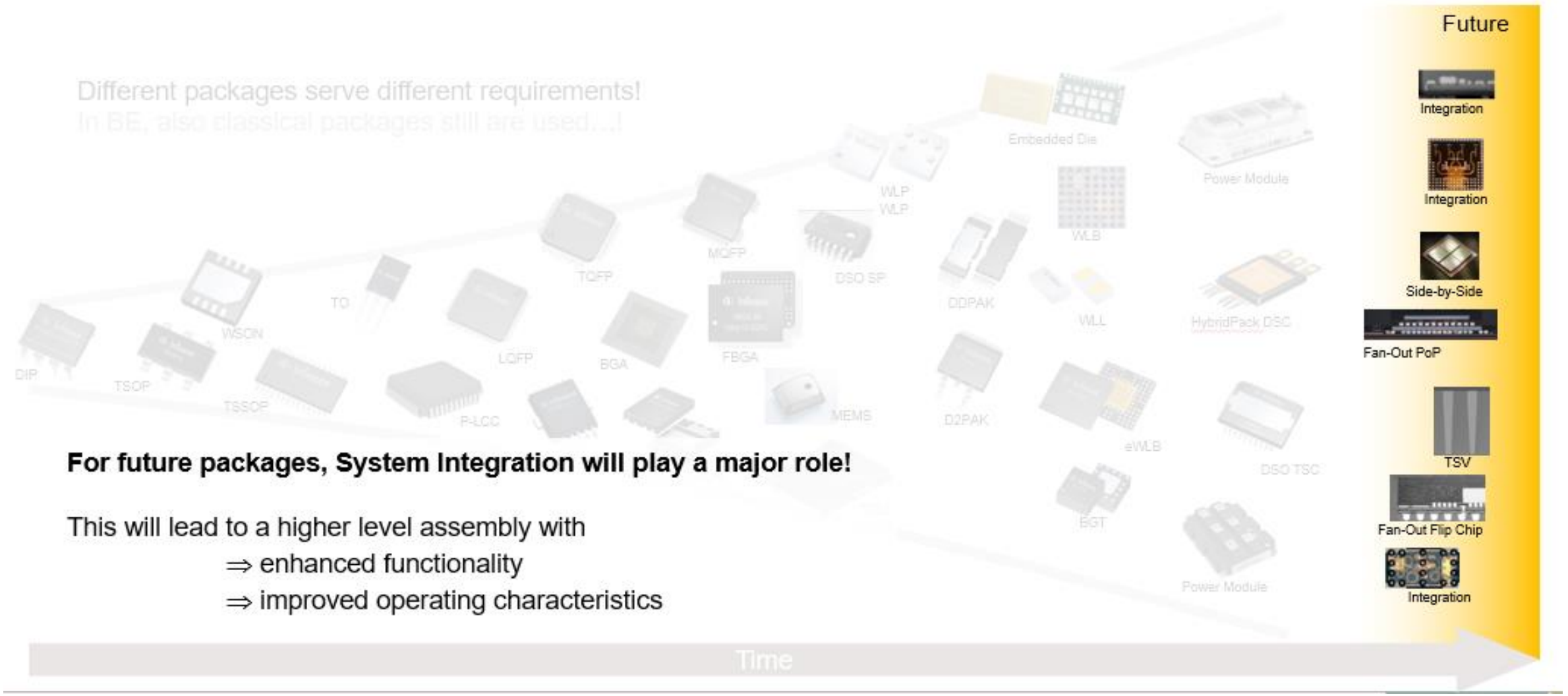


For future packages, System Integration will play a major role!

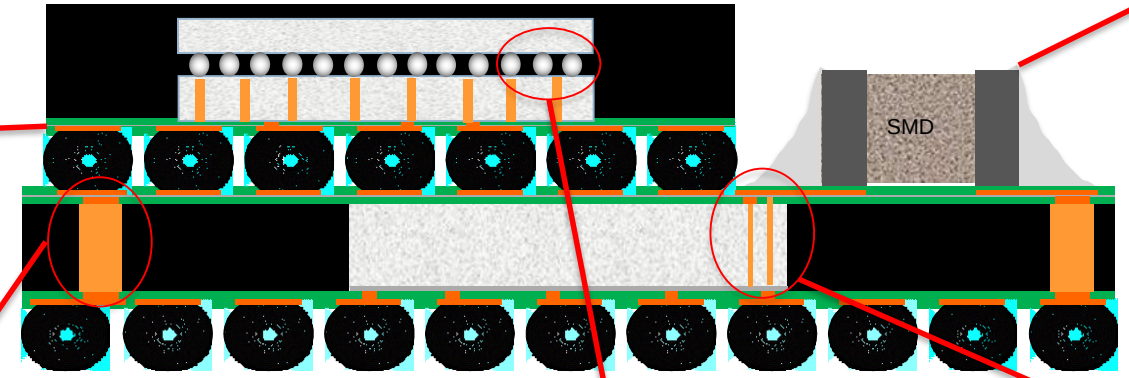
This will lead to a higher level assembly with

⇒ enhanced functionality

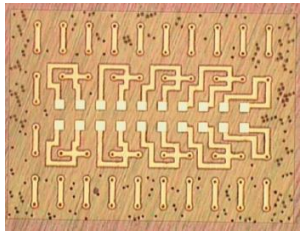
⇒ improved operating characteristics

3D Stacking Vision (Heterogeneous Integration RM)
Building Blocks and Materials

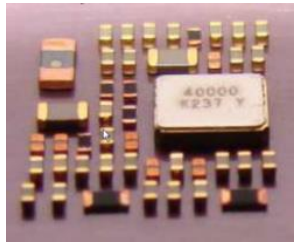
- Multiple functional elements in a visionary SiP example
- Provision of functional elements/ building blocks is crucial



Redistribution Layers (RDL)
(single-/ multi-layer)

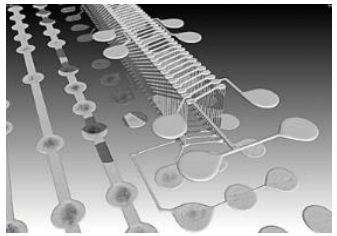


Passives
(SMD, IPD, thin-film)

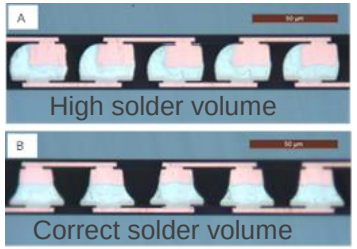


Source: Nanium

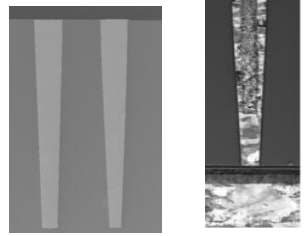
Vertical Interconnect
(TEV, Via Bar, TGV, TMV, EZL)



Fine Pitch Interconnect
(Micro bumps, Cu-pillars)

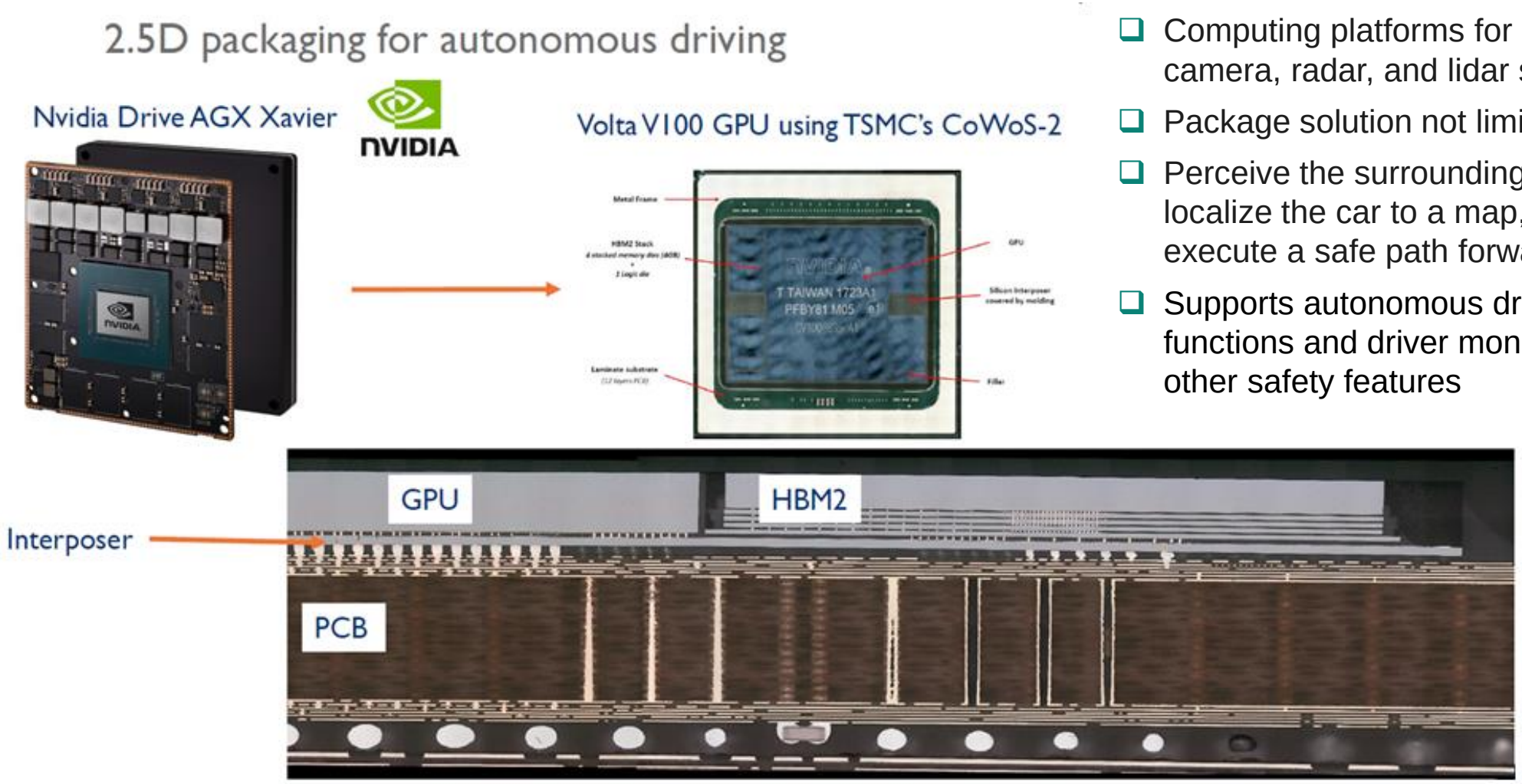


Vertical Interconnect
Through silicon via
(TSV)



Integration (in Automotive) <=> RISK V for processing

2.5D Package



- Computing platforms for data processing from camera, radar, and lidar sensors
- Package solution not limited to automotive
- Perceive the surrounding environment, localize the car to a map, and plan and execute a safe path forward
- Supports autonomous driving, in-cabin functions and driver monitoring, as well as other safety features

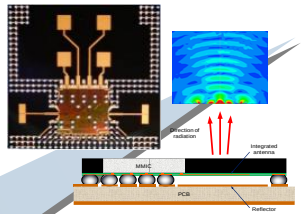
Source: Yole Development

Fan-out WLB (eWLB) - System Integration & 6G

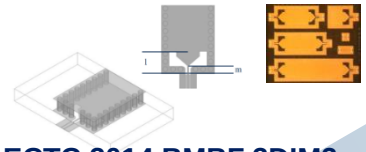
GEFÖRDERT VOM
Bundesministerium
für Bildung
und Forschung

Patch-, Vivaldi-, Dipole-, ...

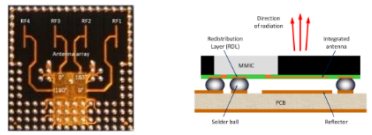
eWLB for > 300 GHz , and 6G



ECTC 2015: BMBF V3DIM
3D eWLB using EZL
Novel concept for
vertical interconnection

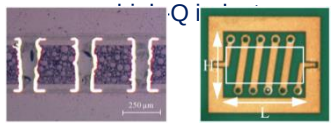


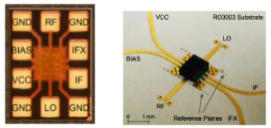
ECTC 2014 BMBF 3DIM3
Waveguide integration
in eWLB and
double sided eWLB



ECTC 2012 BMBF V3DIM3
77 GHz SiGe TRX with
integrated antennas in eWLB

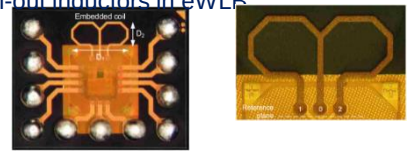
ECTC 2013 : BMBF V3DIM
3D eWLB using TEV
Low-loss transitions and
high-Q inductors

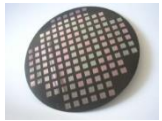


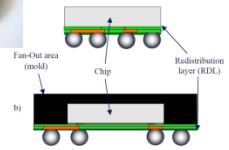


BMBF CoSiP, ECTC 2008
77 GHz SiGe mixer in eWLB

ECTC 2011
BMBF CoSiP
6 GHz CMOS VCO with high-Q
fan-out inductors in eWLB

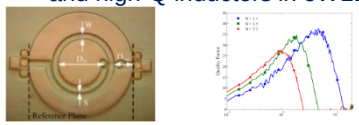






L2PC, BMBF SIPHA
BMBF, 2002 – 2008,
ECTC 2004, 2006
Beginning of eWLB

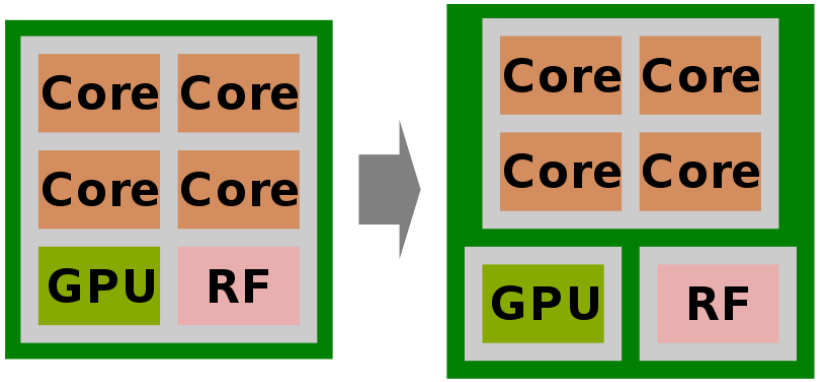
EPTC 2007 BMBF CoSiP
Low-loss transmission lines
and high-Q inductors in eWLB



Growing importance of chiplets - This is a design topic

A **chiplet** is an integrated circuit block that has been specifically designed to work with other similar chip-lets to form larger more complex chips.

In such chips, a system is subdivided into functional circuit blocks, called "chip-lets", that are often made of reusable IP blocks.



https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2024-edition.html

We need Knowledge Generation

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- **Coherent View Chip-Package-Board/System (from nm to mm)**
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We need a coherent view chip – package - board / system
=> no silo mentality / => new project opportunities over value chain

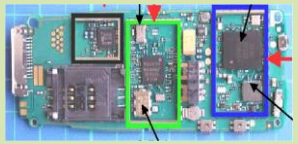
Chip (from nm to µm)

Process/materials
(from nm to µm)
clean rooms

Fan-Out PoP

Package (µm to mm)

Package Processes
Move to clean rooms

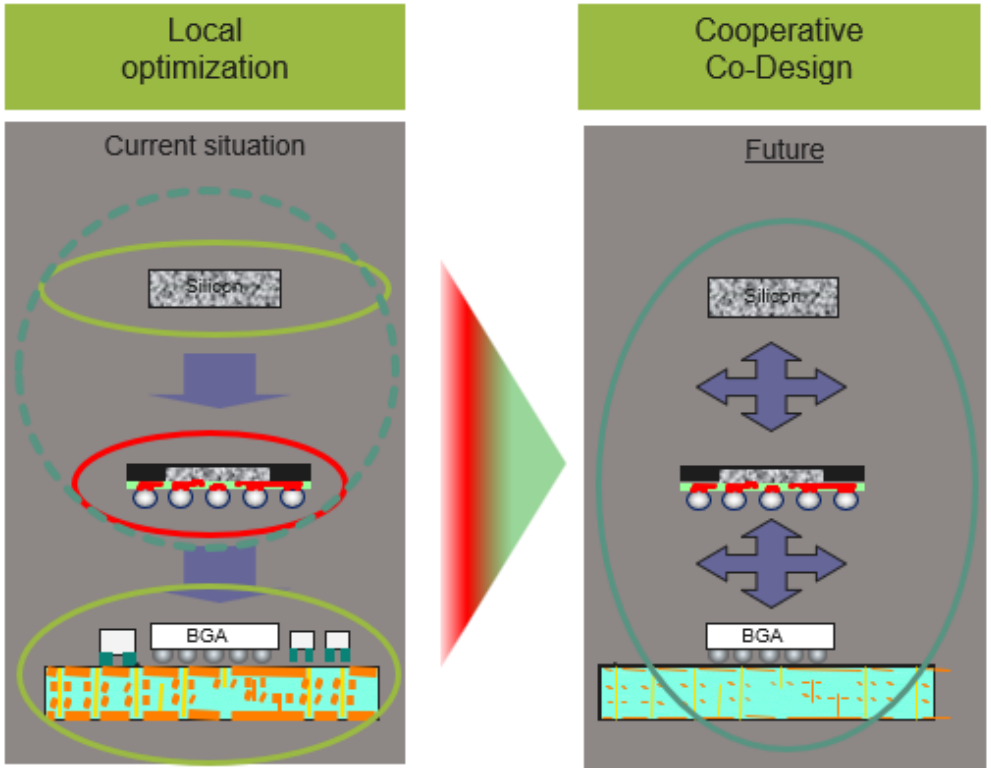


Board/Module/Subsystem (mm to cm)

Board/Module/Subsystem processes
(mm to cm) ***Move to somewhat clean rooms***

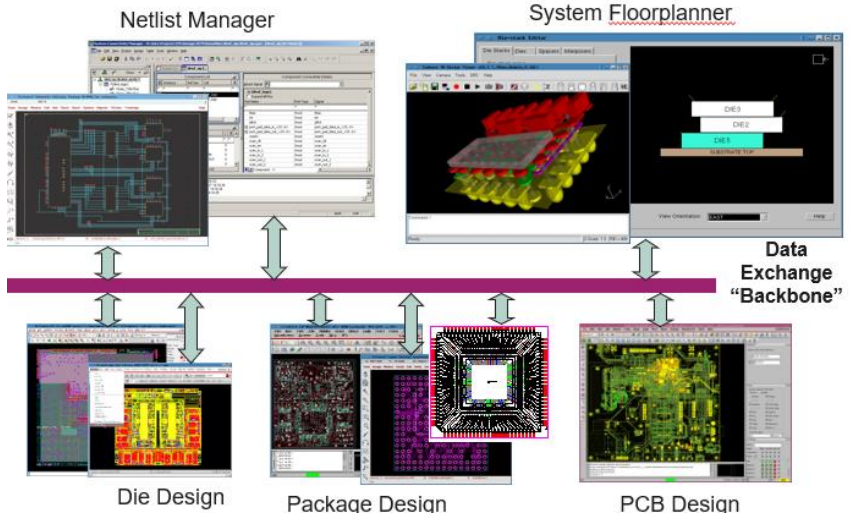
CoDesign	***Chip*** (from nm to µm)	Package (µm to mm)	Board/Module/Subsystem (mm to cm)
Reliability along the value chain	***Chip*** (from nm to µm)	Package (µm to mm)	Board/Module/Subsystem (mm to cm)
Failure analysis	***Chip*** (from nm to µm)	Package (µm to mm)	Board/Module/Subsystem (mm to cm)

Chip-Package-Board Co-Design: Cooperative Co-Design



Advantages of Co-design

- Package/ Board influence on system level
- Optimized performance
- Optimized matching
- Optimized system cost
  - Reduced layers
  - Less over-engineering
  - ….
- Better quality
- Shorter time to market

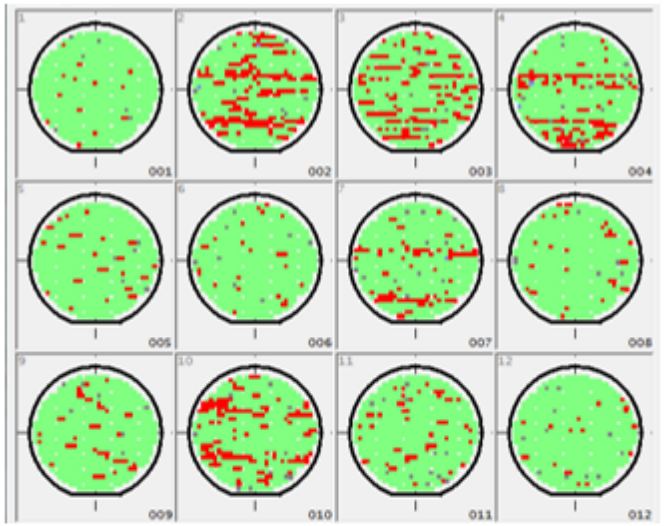


Research along value chain (www.irel40.eu)
Assembly and Packaging - a part of the Value Chain

Assembly and Packaging Device Tracking (ECSEL JU iRel40)

- Artificial intelligence
- Machine learning
- Digital twin technologies

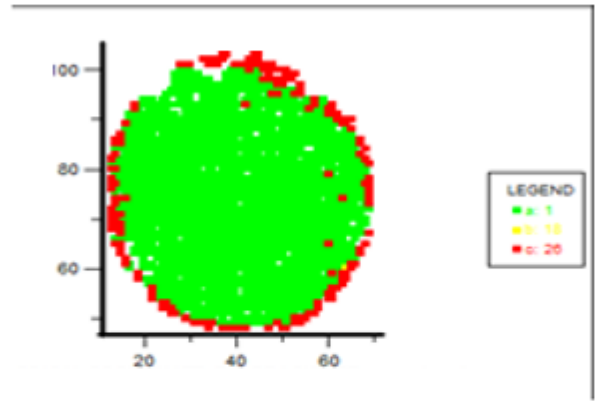
Package level (eWLB)



eWLB Wafermaps show stripes and random distributed fails

Wafer level (Chips)

Reconstructed Frontend map

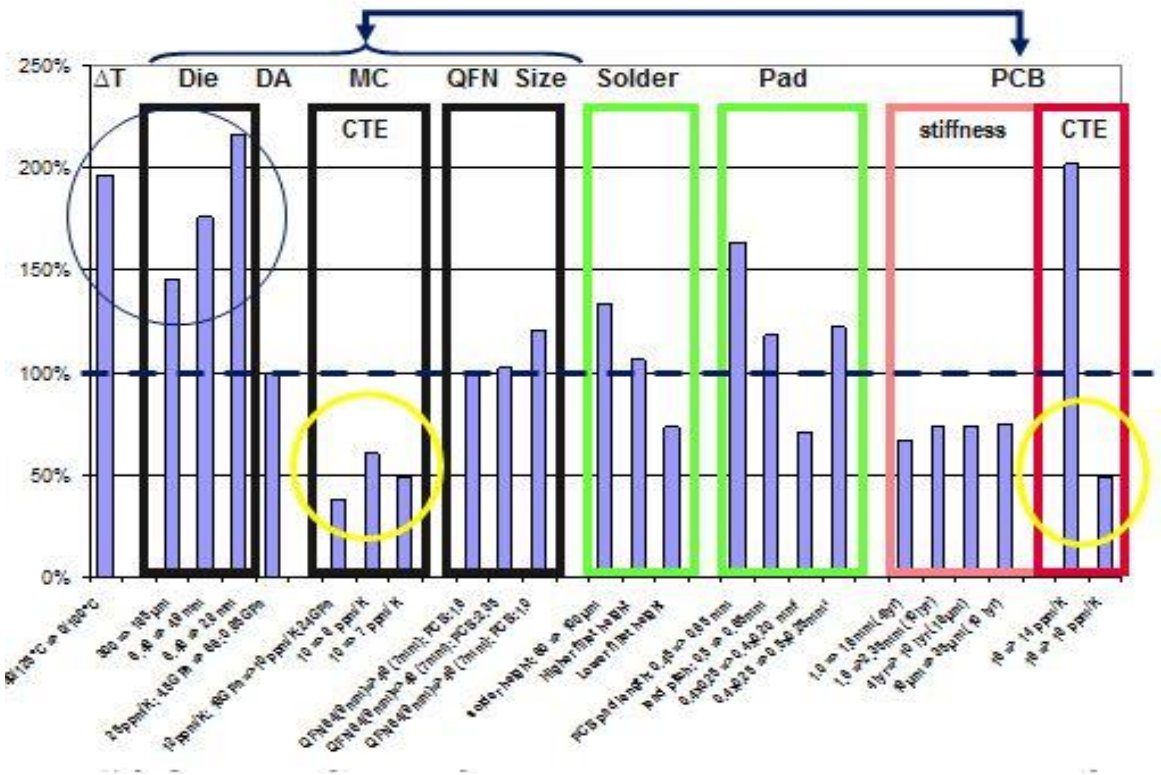


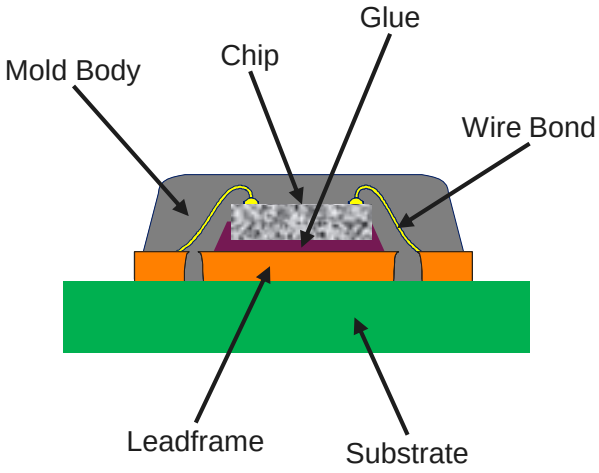
Tune VCO Fails mainly come from devices at the edge of Frontend Wafer

Benefit of SDT: proof that there is no package problem, but a test issue → Yield, cost

Combined Know-How Required (material knowhow)
Examples Chip-Package-Board

QFN example (we must understand Chip-Package-Board/System interaction)
CTE of the board is most relevant





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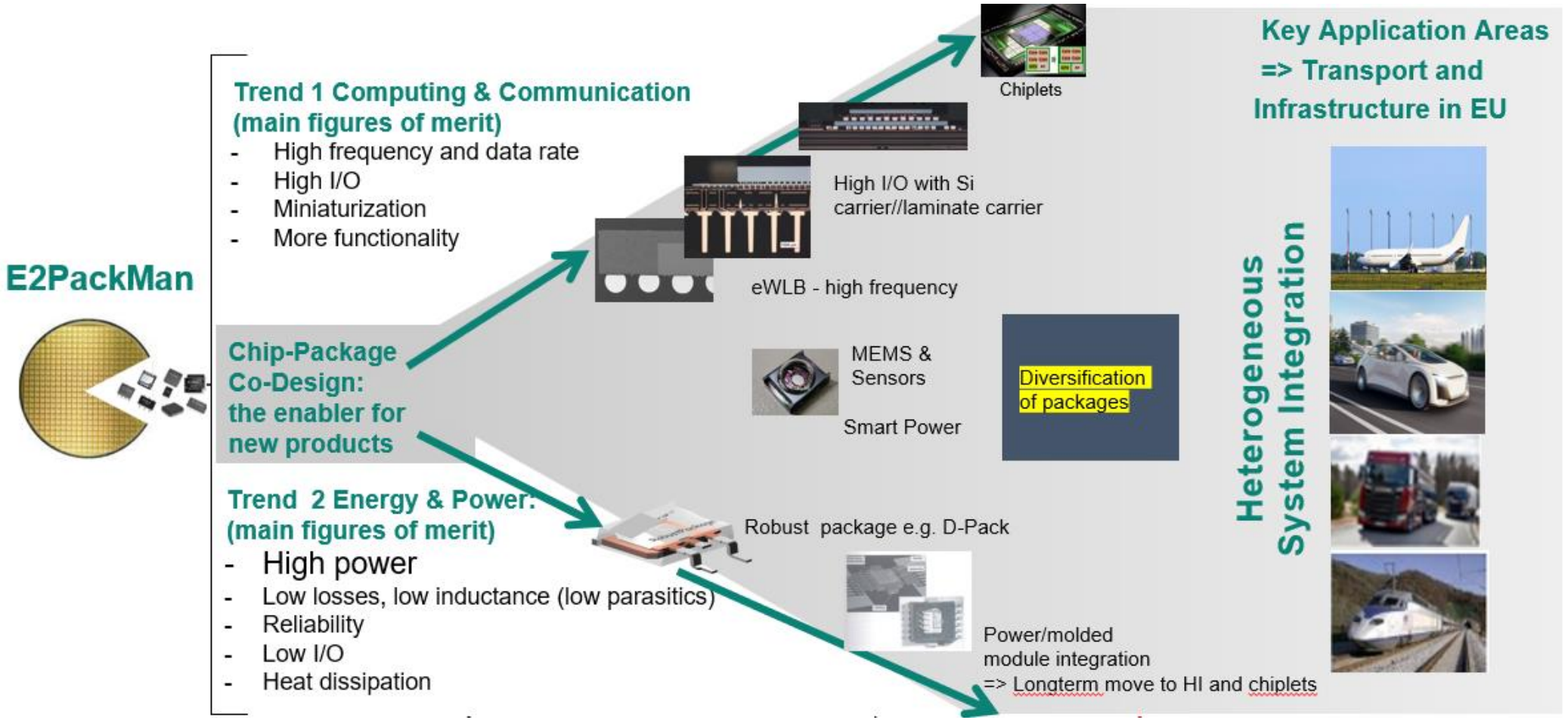
The two main packaging trends in microelectronics => see E2PACKMAN



Reliability
Understand applications and customer requirements

- Different applications have different reliability requirements, e.g. drop test vs. TCoB
- Understand application requirements e.g. checking of board thickness
- We need to better understand physics to avoid one chip in different packages
- Different packages have different failure modus; we need to detect and investigate unknown failure modus
- It is not guaranteed that the same package fits to different applications (example: automotive)

30 years of operation on sea

Autonomous driving
Today: 8.000 hours on-time
Tomorrow: 121.500 hours on-time

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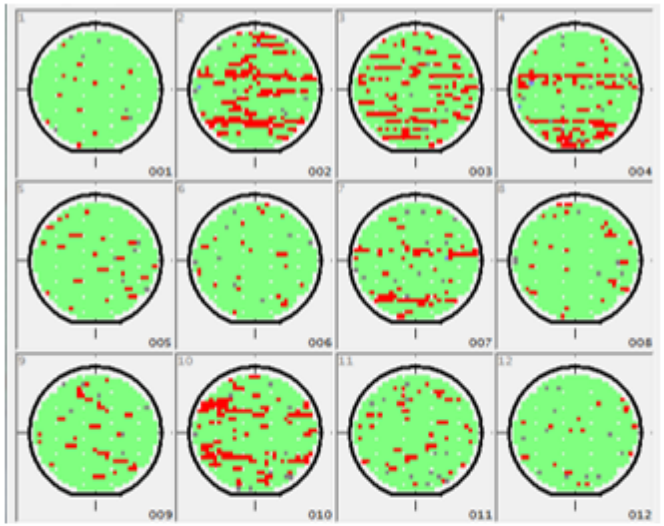
Package level (eWLB)



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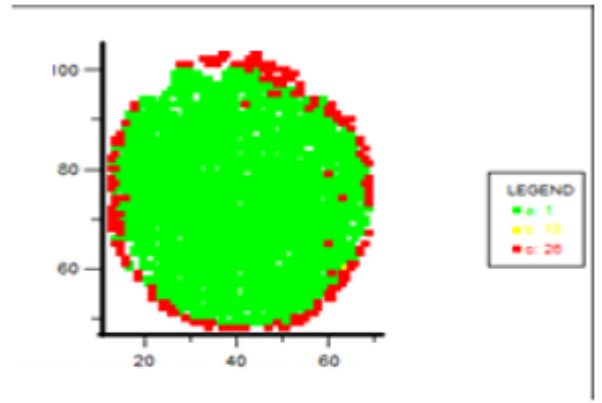

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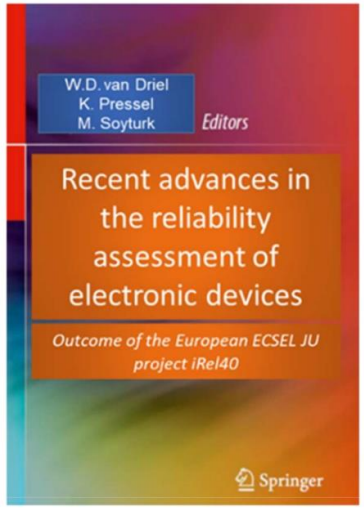
Intelligent Reliability (iRel40) – A Knowledge Generator (www.iRel40.eu)

iRel40 – a knowhow generator



A book was finalized recently
=> we identified 20 different chapters in the following areas

- *Multi-scale & multi-physics simulations for physics-of-degradation,*
- *AI based control systems in advanced production,*
- *Smart sensing and big data analysis,*
- *Reliable Materials, Reliability Testing and Di-agnostics,*
- *Prognostic and health management / digital twin / condition monitoring and*
- *Design.*

iRel40 – build bridges and generate networks

íRel40 builds bridges and understanding between domain:
=> During Social Event at Istanbul we prepared a laser show with the iRel40 image on the Bosporus bridge in Istanbul

=> generate personal networks

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Managing Complexity: Five Trends

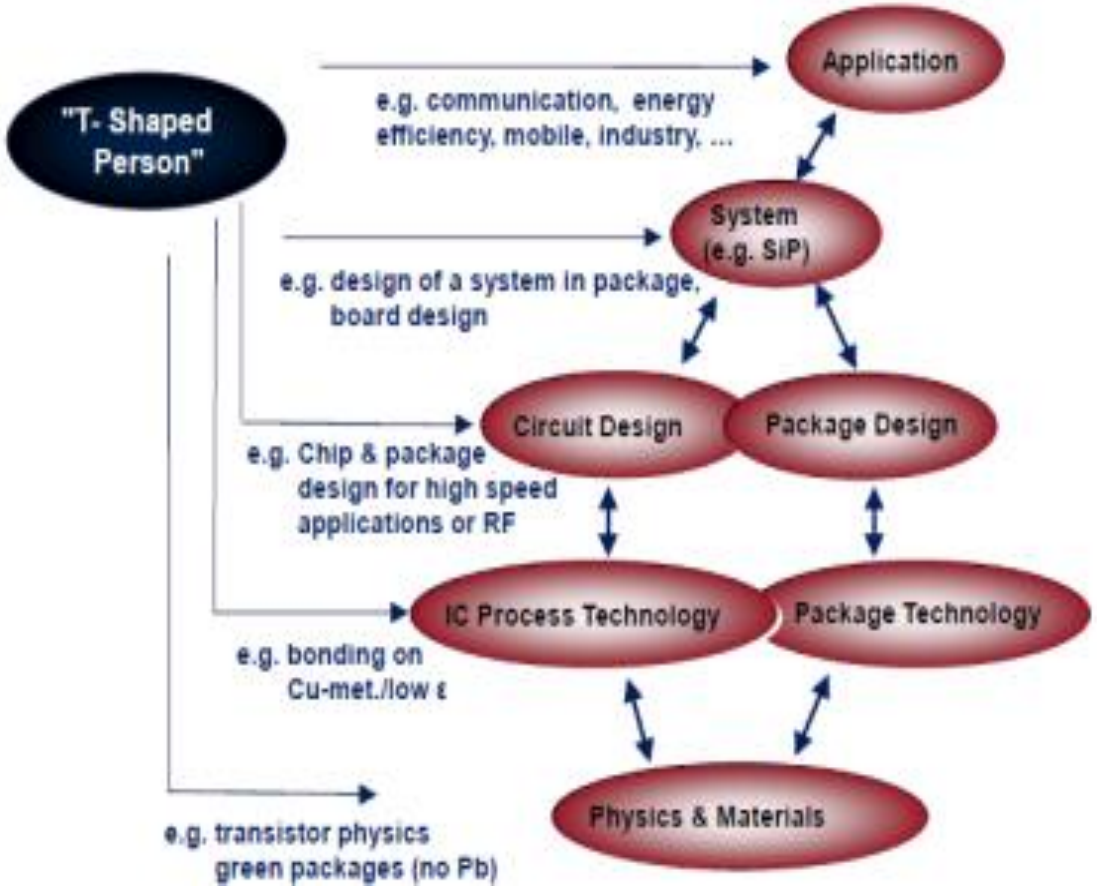
Demanding system reliability & thermal management		▪ Expansion towards high reliability applications (automotive, aviation power distribution, medical) ▪ High reliability of system requires even higher reliability of sub components!
Diversity of technology		▪ Various analog & digital specific IC technol. (memories, RF, processors, power…) ▪ MEMS (sensors, actuators…) ▪ Passives
Complex material mix		▪ Wide range of material properties (Si, metal, ceramics, polymers, composites etc.)
Convergence of IC/ Package/ PCB technology		▪ Wafer level packaging ▪ Chip embedding in laminate ▪ TSV & TEV ▪ Further shrink of interconnects (fine pitch wire bond, thin film techn., TSV) ▪ Integration of passives in RDL/TSV
3D designs		▪ Stacked die approaches ▪ Multiple stacks, interposers… ▪ PoP (package on package) ▪ MEMS

Set-up Know How and investigate standardization

Managing Complexity
What do we need?

- Understand your application requirements
- Understand your customer (price, performance, …)
- Understand trade-offs between technologies (TSV, TEV, …)
- Understand and develop the appropriate toolbox elements
- Understand physics of processes, failures, performance, …
- Understand your supply chain
- …

→ **We need T-shaped persons**



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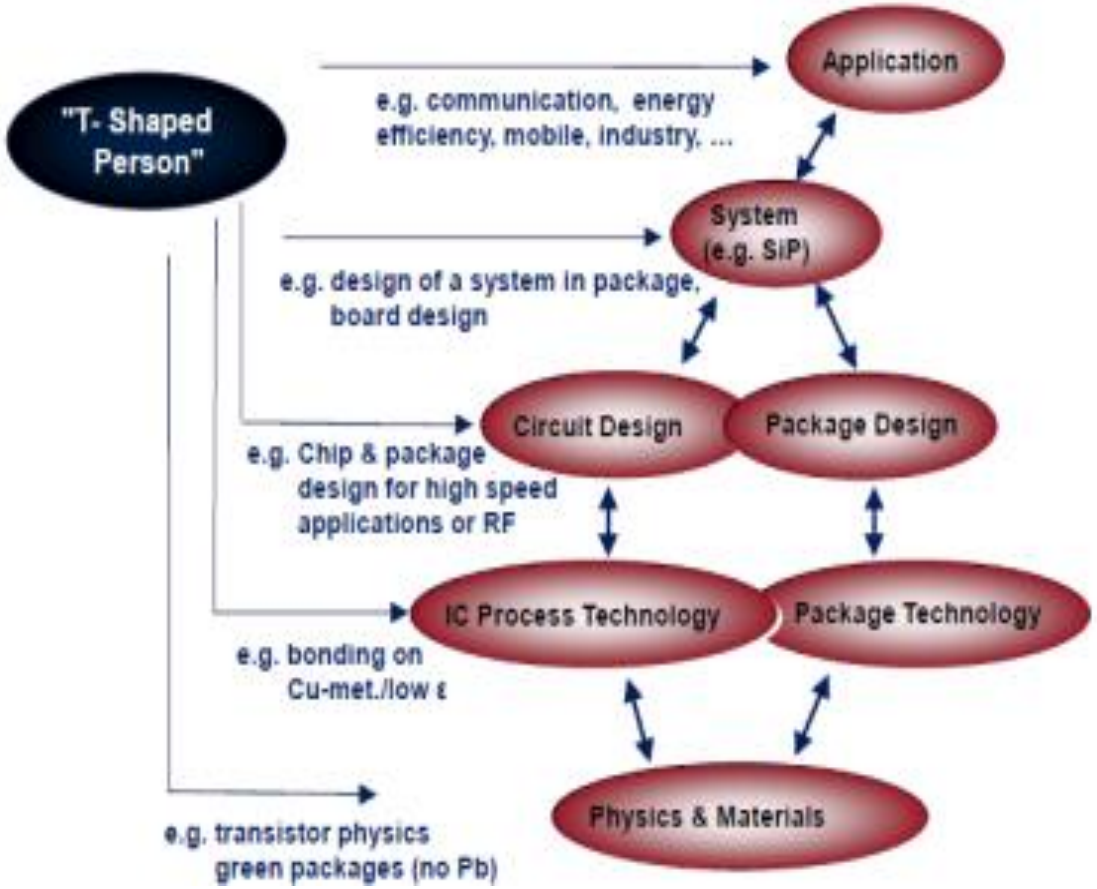
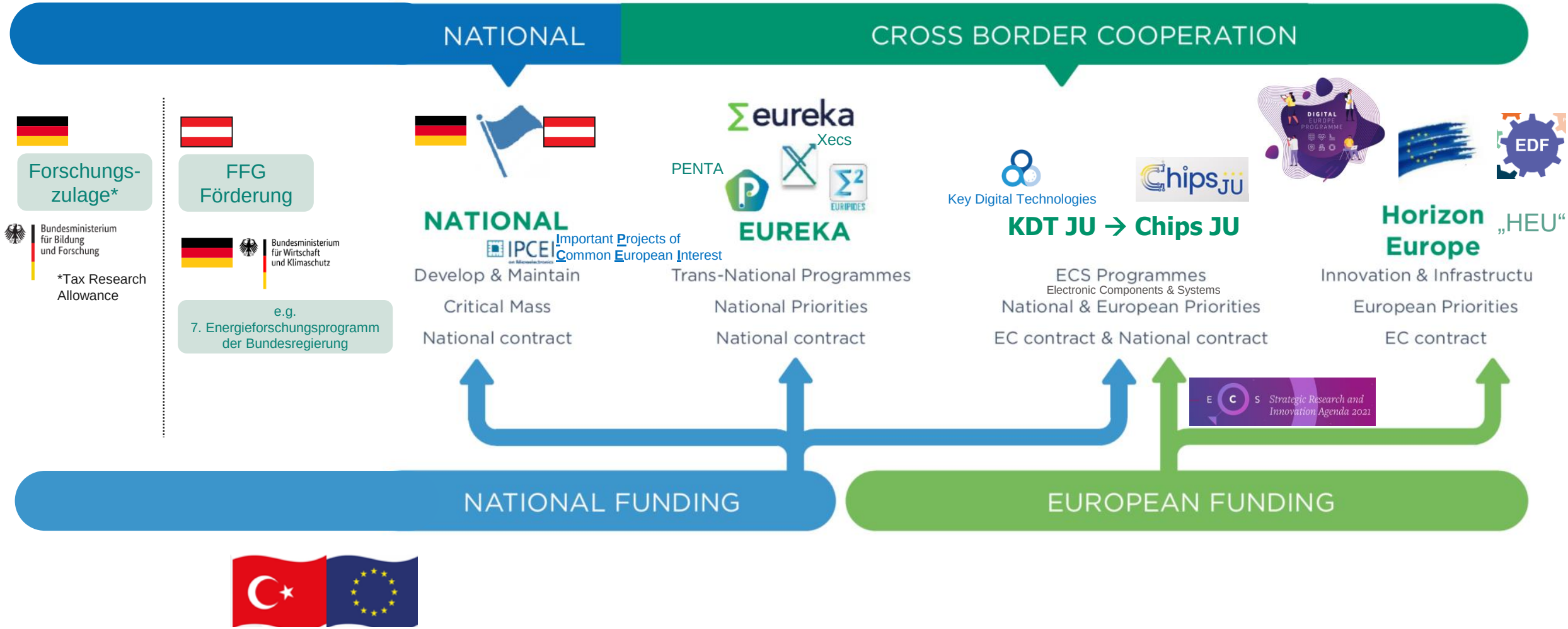


We need Knowledge Generation

Today‘s 7 Messages

- Growing Importance of Microelectronics (Megatrends)
- System Integration Everywhere (Assembly & Packaging, Heterogeneous Integration, Chiplets)
- Coherent View Chip-Package-Board/System (from nm to mm/cm)
- Understanding of Customer Requirements (e.g. Reliability Constraints)
- New Opportunities of Computer and Data science/management
- Management of Complexity
- **European and National Funding Opportunities for Micro/Nanoelectronics**

Funding instruments national & EU
Illustration from Infineon Germany & Austria Perspective



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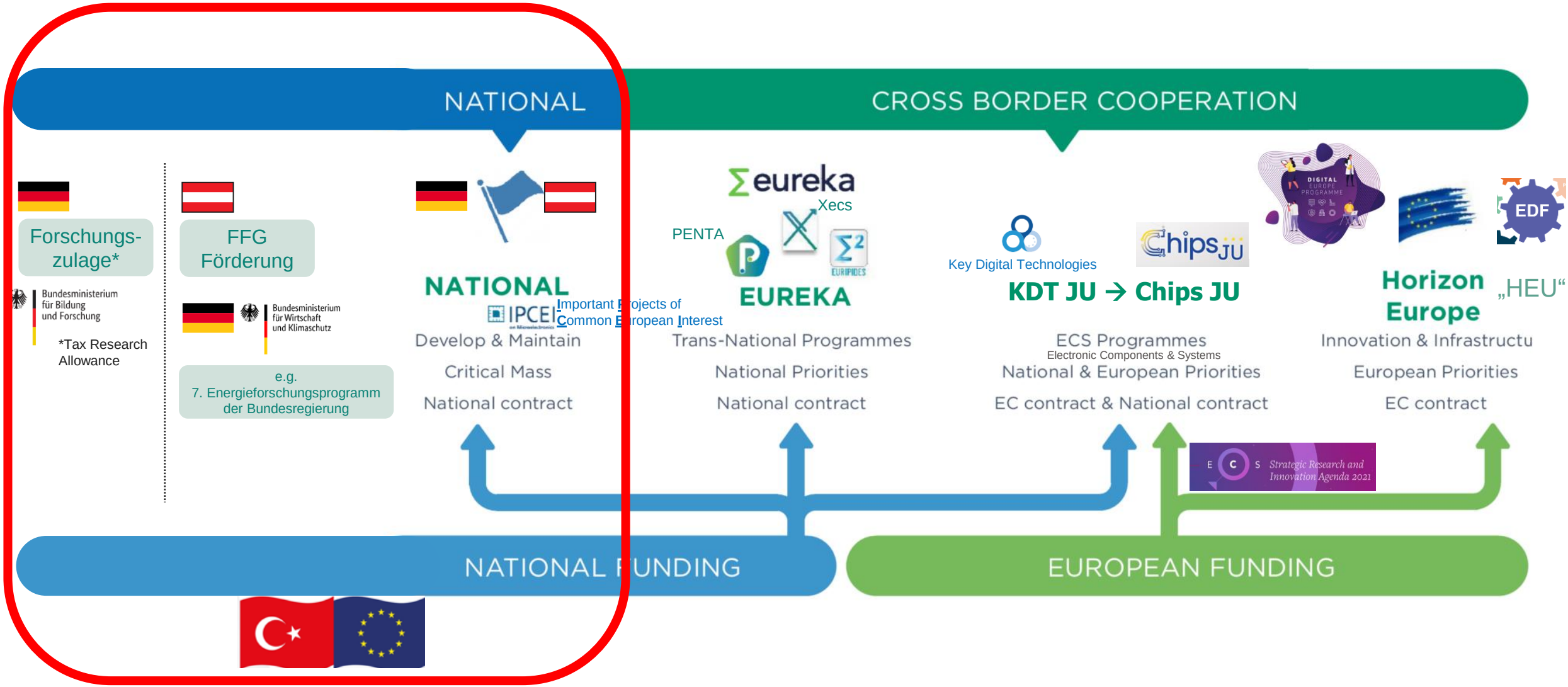

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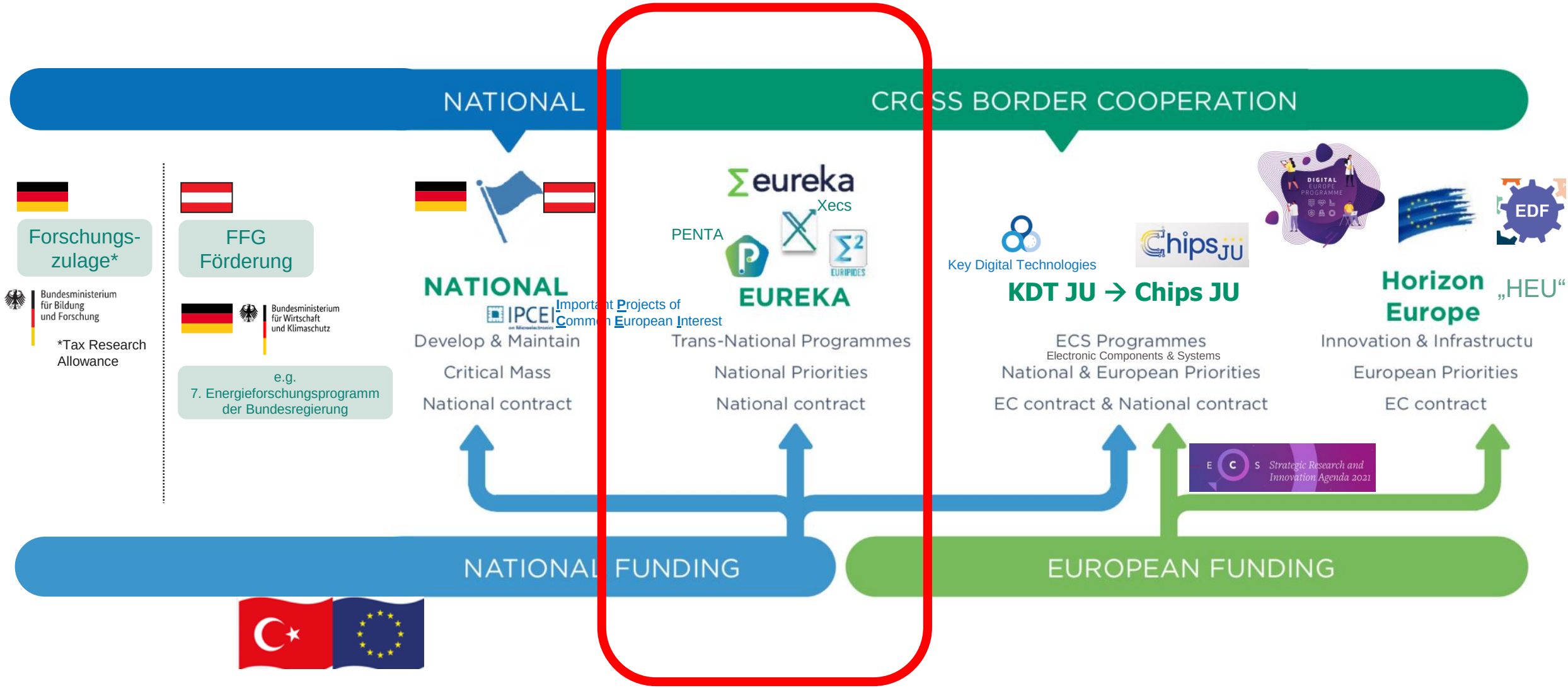

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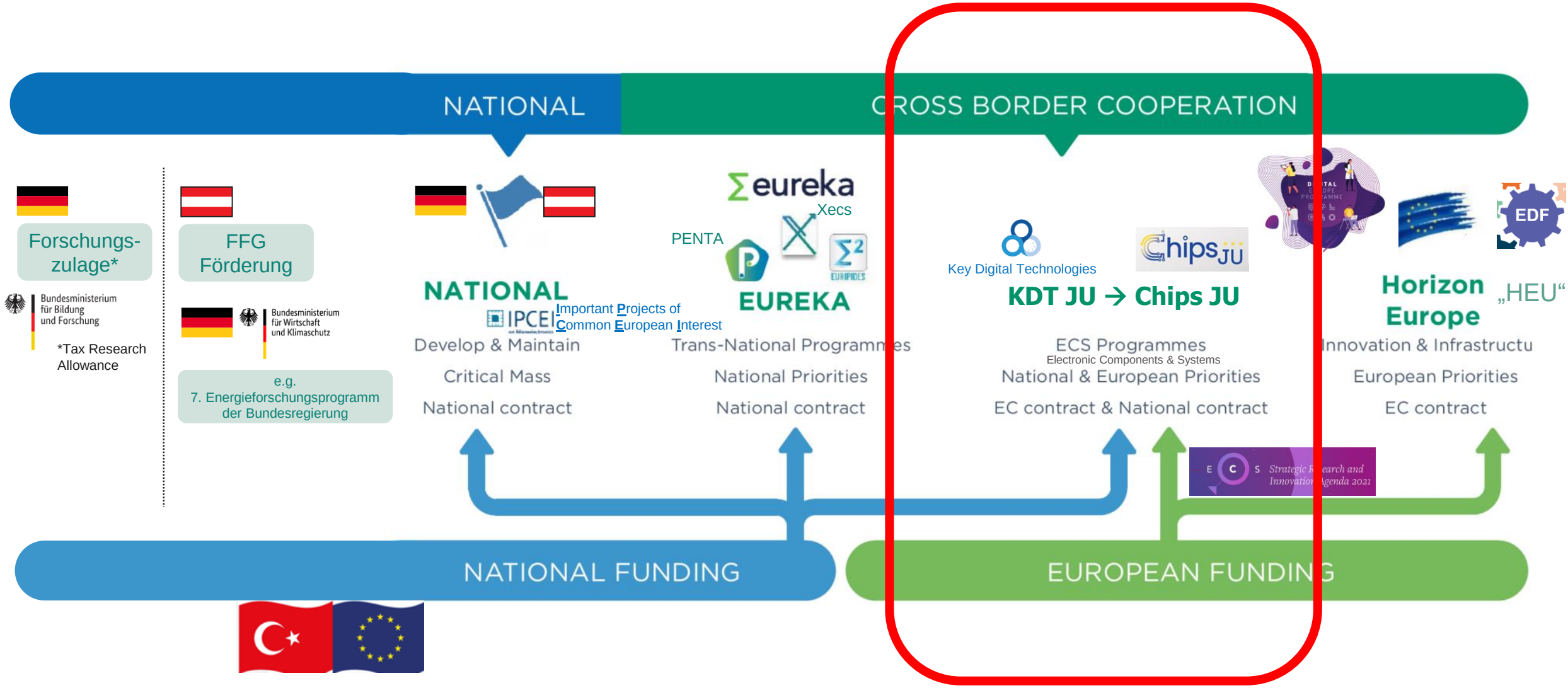

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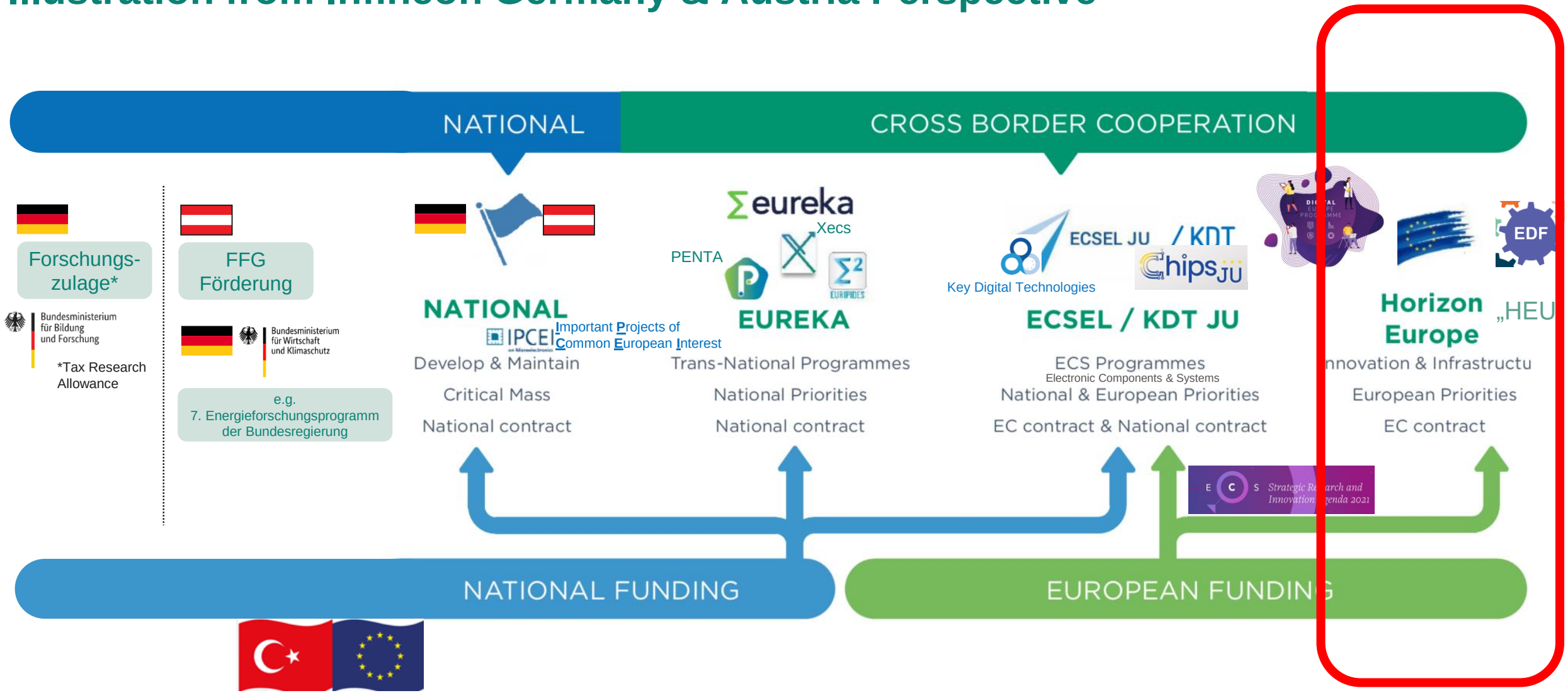

Today‘s 7 messages (Digital, Chips and 6G)

- Growing importance of microelectronics (more applications, Megatrends)
- System Integration Everywhere (Assembly & Packaging (A&P) for System Integration , Chiplets))
- Coherent View is required => Chip (from nm to um) – Package (um to mm) – Board (mm) (CoDesign)
- Understanding of customer requirements is a key (reliability)
- New opportunities of data science/management (in R&D, in production/device tracking)
- We need management of complexity (tackling of cost targets is a major challenge)
- Europe together with national bodies offer outstanding funding opportunities for Micro/Nanoelectronics

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We need Knowledge Generation over Domains, no Silo Mentality

Thank You
Questions