Samanyu Okade

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ABOUT

Result-oriented Microelectronics graduate from TU Delft with a strong analytic mindset to learn fast and deliver efficiently. My research focuses on fault-tolerant and high-performance hardware using FPGAs and SoCs. I work hands-on with Verilog, Vivado, and Python for simulation and automation. My long-term goal is to apply digital design to create resilient, high-impact intelligent hardware with efficient signal-processing and control loops for space and related systems.

EDUCATION

Delft University of Technology
Delft, Netherlands 2023-2025
MSc in Electrical Engineering – Microelectronics track, specialisation in Digital Systems
[Hardware for AI; Digital VLSI Design; Modern Computer Architecture; Hardware Dependability; Digital Design I&II]

Vellore Institute of Technology
Vellore, India 2019-2023
B.Tech in Electronics and Communication Engineering

KEY SKILLS

- Tools & Scripting: Python, TCL, Cadence Genus/Innovus, version control (Git)
- Digital Logic, SoC & FPGA Design: RTL design, Verilog, Vivado, Quartus, QuestaSim/ModelSim
- Verification: Testbench development, simulation, post-layout verification, documentation
- Other: RISC-V familiarity, hardware dependability, ECC, TMR, digital signal processing.
- Lab & Testing: Oscilloscope, logic analyser.
- Soft Skills: Creative thinking, Public-speaking, Effective Communication, Collaboration, Writing, Adaptability.

WORK EXPERIENCE AND INTERNSHIPS

TU Delft
Teaching Assistant ***Sept 2024- Apr 2025***
- In Introduction to Programming-3 (EE2L1), I guided students throughout a Python-based signal processing project for heart-sound localisation using multi-microphone data.
- In courses like Systems Engineering (EE4C11) and Introduction to Machine Learning (EEX01), I assisted undergraduate and graduate students in evaluation, project development, and mentoring across interdisciplinary topics in systems, programming and machine learning.

MKB Data Studio
ML engineer for client, Koninklijke van Twist (KVT) ***July 2025- Aug 2025***
- Built a Python pipeline to parse the power generator issues and multi-template service-report PDFs into normalised CSVs.
- Delivered a multilabel learning model with rule checks to flag incomplete fields.

Lunar Zebro
Comms Subsystem Lead ***Oct 2024- June 2025***
- Design and critical assessment of the digital communications PCB (Owned requirements → schematic upgrade → PCB and BOM with radiation-aware parts → board bring-up and test).
- Mentor & review the work of 2 undergraduate engineers, coaching them on Altium schematics.

RTips Technologies

Hardware intern ***Oct 2022- May 2023***

- Researched and improved a device that converts MODBUS and DALI communication protocols from the base design of the PCB to its integration on KiCAD.

Students for the Exploration and Development of Space (SEDS India)

Executive Director ***Nov 2021- Nov 2022***

- Mentored CubeSat, International Rover Competition and International Rover Design projects in cross-functional teams across 14 sub-chapters.

The Institution of Engineering and Technology (IET-VIT Vellore)

Hardware Head ***Dec 2020- Dec 2021***

- Sharpened hardware skills in embedded systems, fundamentals of communication, CMOS, and digital designs by mentoring 12 freshers and sophomores.
- Mentored three teams to victory in hardware tracks and open categories in hackathons, Equinox, and Hack4cause.

ACADEMIC PROJECTS

TIENOS: A Tool for Intensive Exploration of Neuromorphic Workloads for Outer Space ***Jan 2024 – Aug 2025***
(Poster presented at Neuromorphic Computing Netherlands, NCN2025)

- Designed a tool to map SNN training-layer protection and tinyODIN hardening targets, via intensive sweeps to improve robustness with zero to minimal overhead in hardware (vs 3x logic replication in TMR).
- Using Python+Vivado, TIENOS produces +15% accuracy in bit-flip noise conditions in an event-based resource-constrained image processing CubeSat system, with suggestions for further hardening when synthesised on a Zynq7000.

RISC-V SoC Pathfinding Accelerator (TU Delft – ET4351 Project) ***Mar 2025***

- Implemented a shortest-path accelerator integrated with a PicoRV32 RISC-V SoC using Verilog/SystemVerilog. Achieved x20 latency over baseline after RTL design and timing-clean post-layout verification in Genus/Innovus.

FPGA-based (hardware) decision-making for efficient satellite orientation and propulsion ***Oct 2022 – Apr 2023***
(Published in IEEE Xplore in June 2023)

- Devised a method for rockets or satellites to orient and align solar panels by rotating using FPGAs to make the most efficient positioning decisions using sensor-based information.
- Designed an amplified LDR network to drive actuation through servos using a Cyclone IV FPGA with Quartus.

A Robotic Solution for Internal Imperfection Detection in Industrial Machinery ***Sept 2021 – Nov 2021***
(Published in the AIP Conference Proceedings in March 2024)

- Prototyped "SensoRobot", a small, automated mobile robot by integrating flame, DHT-11, MO-26, and ultrasonic sensors to detect anomalies and conditions within tight industrial equipment spaces.

CERTIFICATIONS

- Bosch Spring School on AI in industry in 2025.
- Provisional discovery of the Main Belt asteroid 2021EM17.
- CMOS Digital VLSI Design-course certification offered by IIT Roorkee. (NPTEL)
- Linear Circuits 2:AC Analysis-course certification offered by Georgia Institute of Technology. (Coursera)
- Introduction to Electronics-course certification offered by Georgia Institute of Technology. (Coursera)
- National Science Olympiad (NSO) Zonal Gold medalist in 2015.
- Academic proficiency awards in 2013, 2015, and 2017.

CAMPUS & COMMUNITY INVOLVEMENT

- IP Coach and Orientation Day Mentor at the EEMCS faculty 2023-2025
- Alpha team member of VIT Dance club 2020-2023
- Flautist and musician in VIT Community Radio 2019-2023
- VIT Swim team 2019-2023