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FPGA Design and UVM Verification for Space Applications

Verification Capabilities

We specialise in verifying satellite platform designs and payloads, including:

- Power, processing, storage and data transmission systems
- IP blocks, subsystems and full SoC designs

We maintain an extensive library of UVM agents for:

Low-speed serial: UART, I2C, SPI, USB

High-speed: SpaceWire, SpaceFibre, Ethernet, CCSDS

Control: CAN, SpaceCAN

On-chip: APB, AHB, AXI

Proprietary protocols

Verification Stages

- RTL: Functional verification
- Netlist: Post-synthesis checks
- Post-Place and Route: Timing-accurate simulations

Devices Under Test

Power: PMUs, sequencing, BMS

Data: OBC, storage, handlers

Imaging: VIS-NIR, SWIR, camera drivers

Communication: Telemetry, high-speed downlinks

Control: Attitude, sensors, FDIR

Project Experience

- Sabiamar and Small GEO sats (INVAP)
- Ground station & radar gateways (Asterix, Eurocontrol)

Tools & Infrastructure

Vendors: Microchip, Xilinx, Altera

Languages: SystemVerilog (UVM), Verilog, VHDL, Bash, Python, Tcl

Simulators: ModelSim, QuestaSim

Toolchains: Vivado, Libero

System verification: Matlab

Infrastructure:

- GitLab with submodules for IP reuse
- Linux-based automation, Windows support
- DVT for doc/diagram generation
- Jira for full task visibility
- Secure VPN access, encrypted file exchange

Collaboration & Deliverables

Workflow:

1. Review specs and test requirements
2. Develop/review testplan
3. Create UVM testbench, simulate, verify
4. Traceability via Gitlab & Jira
5. Automated documentation with PASS/FAIL summaries

Security:

- Encrypted communication
- Secure repositories
- Full auditability via git

FPGA Design Services

We also provide FPGA design for satellite systems. Contact us for our capabilities document.