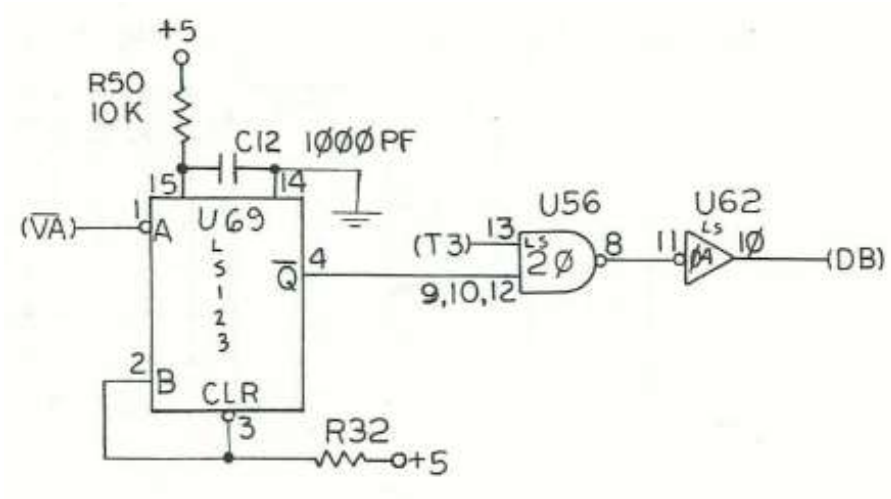
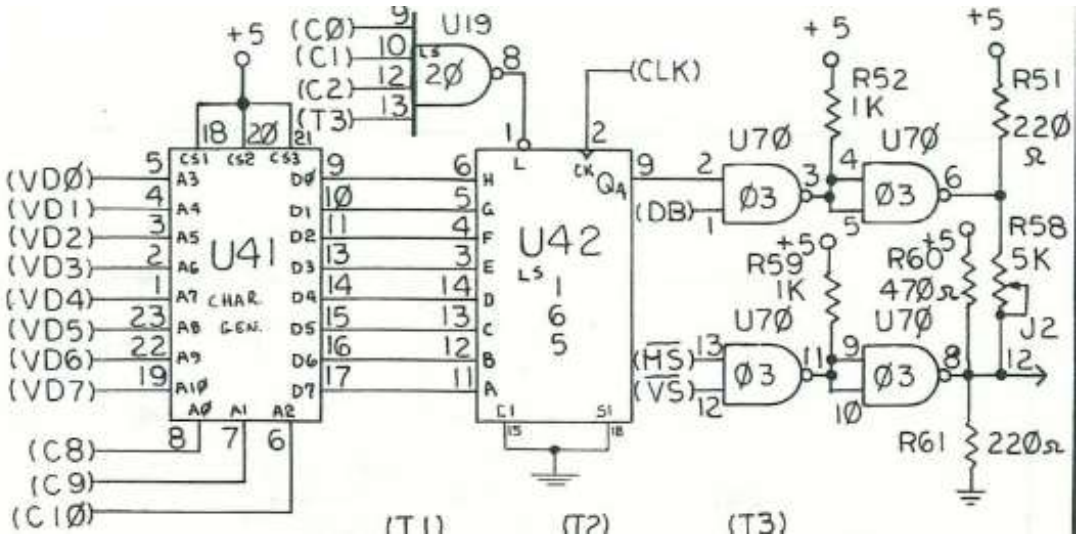
OSI 600 Rev B board aka Superboard II Flicker fixer

NOTE: You will need ≤250ns fast 2114 RAM(with the original character ROM) to get the desired effect

During access to the Video memory (VA), a display blank (DB) signal is generated. This blanks out the video pixel stream from the U42 shift register (see U70 pin 1). For example during text scrolling, you may have observed that characters are partially blanked and the whole screen seems annoyingly to flicker. The more access the video memory gets, the more flicker is visible.
The following “soft” modification will almost eliminate this kind of flicker. It works on 32x32 or 64x16 video memory configurations.



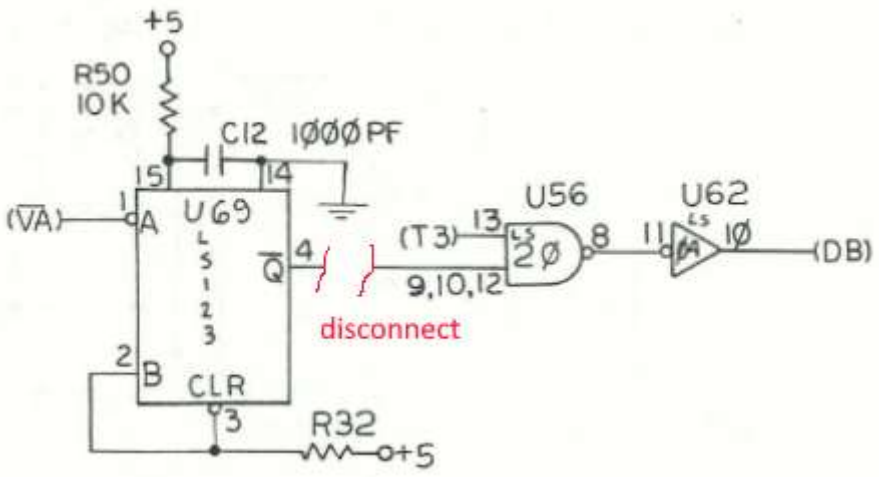


Reason for this behavior is the fact, that the VA encoder uses only address lines, so that VA is active over more that 2/3 of the CPU clock cycle. Also the CPU clock signal (Q0 and Q2) are synchro to the U42 Latch. So Q0 needs to be shifted behind the latch point.
The modification will invert Q0 to C1 and also eliminate the blacking signal DB going to U70.

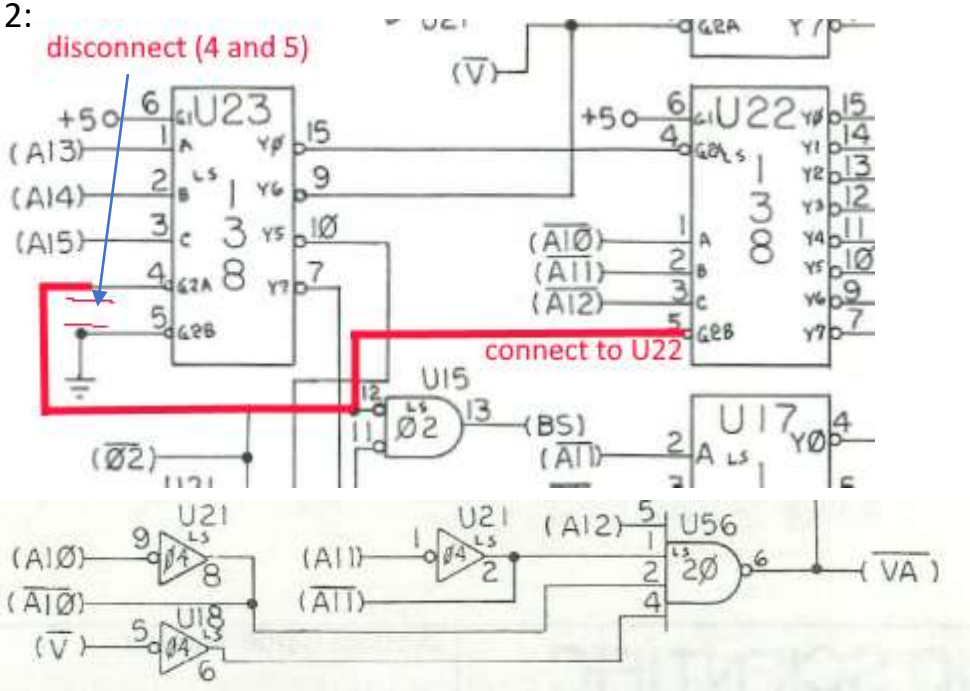
OSI 600 Rev B board aka Superboard II Flicker fixer

Starting with U69 (placed nearby the video connector). I most cases, this IC is socketed on most boards.
In case U69 is in a socked, lift the IC carefully out and bend pin 4 slightly to the outside. When placing the IC back, make sure the pin stays outside the socket connector. In case U69 is soldered to the board, you have to cut the trace coming out of pin 4.

Step 1:



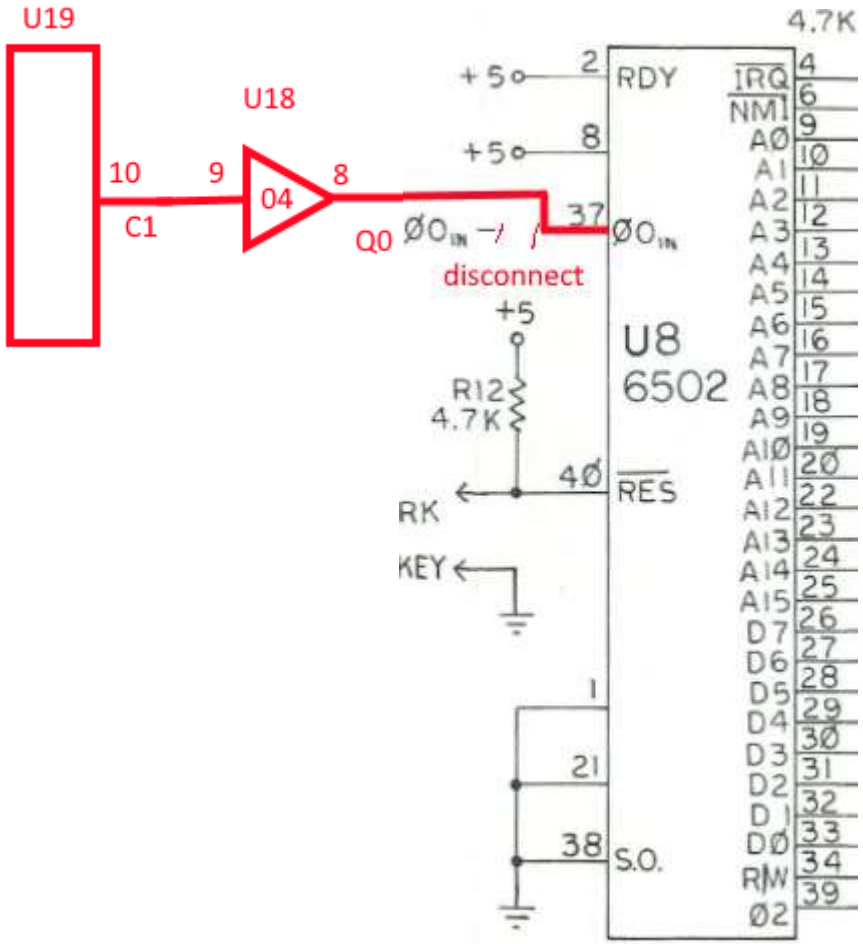
Step 2:



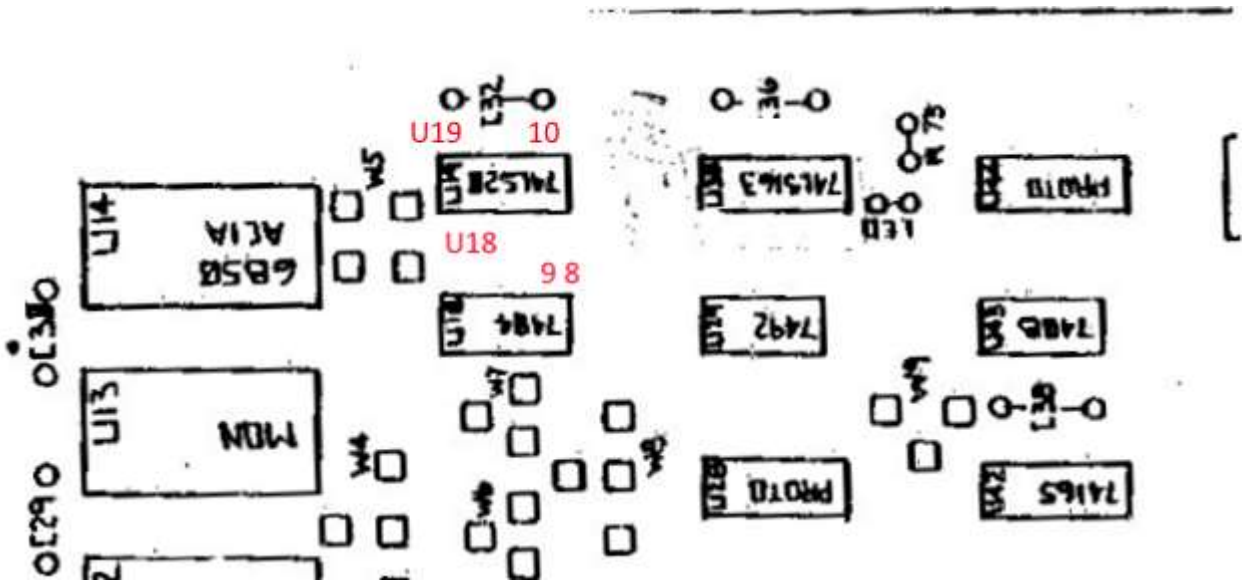
In the next step, we have to modify VA, so that is only valid during the active Q2 clock phase. VA is driven by V and several address lines. V is encoded by U23 by address lines A13..A15. Here we have to modify pin 4 (U23) by disconnecting from ground (just cut the small trace between pin 4 & 5 on the bottom side) and connecting afterwards to pin 4 of the nearby U22 pin 5.
This will gate V by the active Q2 clock phase.

OSI 600 Rev B board aka Superboard II Flicker fixer

Step 3:



Finally, we have to inverse the Q0 input of the CPU compared to C0.
To do this, we have to use an unused 7404 inverter on the board located in U18. Pin 9 is input and pin 8 output of the inverter.
The CPU Q0 clock signal is coming from U30 and also pin 10 U19.



You may find the trace going pin 37 to the CPU, disconnect this trace and wire the inverter U18 pin 8 in between (see to the left)

NOTE: before doing step 3, you may test the computer for proper completion of Step1 & 2. The video output should work normally and during scrolling, white artifacts are visible on the screen. They will disappear, when Step 3 is completed.