

## Pressure Sensor Interface and Signal Conditioning IC with Polynomial Signal Compensation and Advanced Diagnostics

### FEATURES AND BENEFITS

- Directly interfaces with strain gauge or other transducer in Wheatstone bridge configuration for low noise and high accuracy measurements
- On-chip Poly(4,4) compensation for improved accuracy over temperature, compensating both IC and bridge
- Offering from Poly(1,1) to Poly(4,4) polynomial compensation including any possible degree between 0 and 4 like Poly(2,4) and Poly(3,3).
- Ratiometric analog output for legacy applications
- High bandwidth option to support fast response time applications
- PWM (Pulse Width Modulated) output with optional diagnostics to identify fault conditions
- SENT (Single Edge Nibble Transmission) output configurable for temperature or diagnostic reporting in addition to pressure data
- Fast SENT provides increased data rates to support fast response time applications
- Manchester interface for programming through single OUT pin
- Internal device temperature available on output via SENT protocol (or volatile registers)
- Suite of diagnostics to allow for safety-critical systems fault detection
  - Broken wire detection
  - Under- and overvoltage detection
  - Under- and overtemperature detection

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### DESCRIPTION

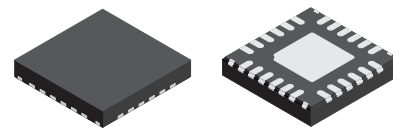
The A17700 is a sensor interface IC designed to connect directly to a strain gauge or other sensor in a Wheatstone bridge configuration. The A17700 amplifies and converts the analog input from the bridge to the digital domain, low-pass filters the signal, and outputs a ratiometric analog signal or a digital SENT/PWM protocol. Digital signal processing functions, including temperature compensation and gain/offset trim, provide an accurate and linear output. A Manchester programming interface for configurations is also available. It includes on-chip EEPROM technology capable of supporting up to 100 read/write cycles for programming of calibration parameters.

The A17700 incorporates advanced diagnostic functions to support safety-critical application designs.

The A17700 is available in a 24-pin 4 mm × 4 mm QFN package with wettable flank and exposed thermal pad.

### PACKAGE:

24-pin wettable flank QFN with exposed thermal pad (suffix ES)



Not to scale

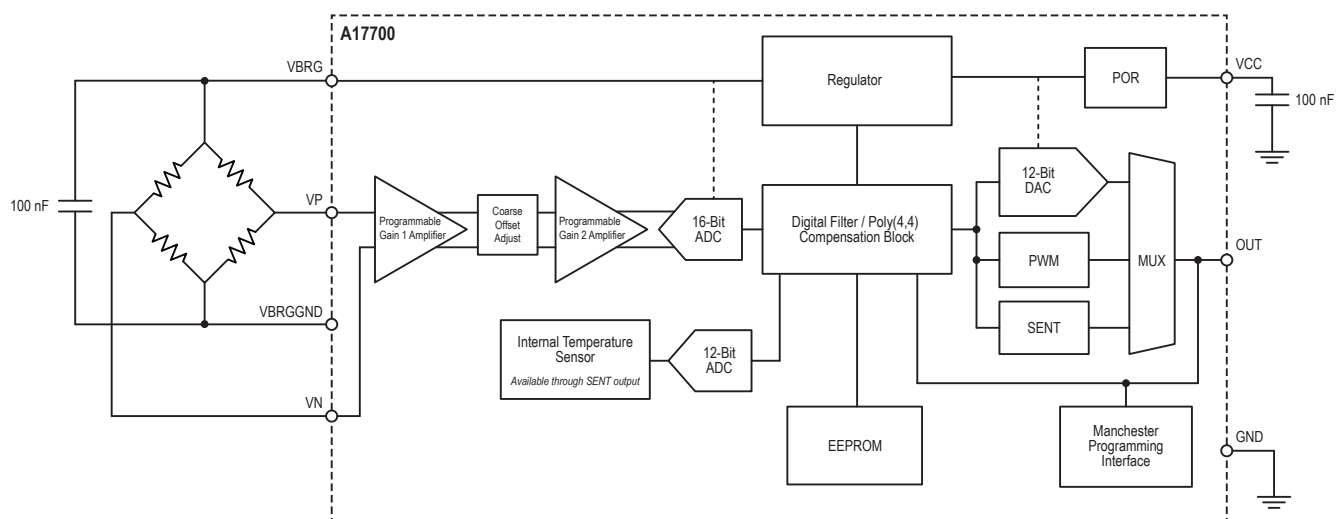


Figure 1: Functional Block Diagram

### FEATURES AND BENEFITS (continued)

- Bridge diagnostics
- Input signal Out-of-Range detection
- EEPROM with Error Correction Control (ECC) for trimming capability and product traceability
- AEC-Q100 Grade 0
- Wide operating temperature range:  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$
- QFN package with redundant bridge supply pins for PCB board space optimization
- Wettable flanks enabling visual inspection of solder joints



### SELECTION GUIDE

Part Number	Output	Packing	Packing
A17700LESBTR-AO	Analog Output	24-pin QFN with wettable flank and exposed thermal pad	1500 pieces per 7-inch reel
A17700LESBTR-DO	Digital Output (SENT/PWM)	24-pin QFN with wettable flank and exposed thermal pad	1500 pieces per 7-inch reel

### ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	$V_{CC}$		24	V
Reverse Supply Voltage	$V_{RCC}$	Voltage delta between supply and output must not exceed 24 V	-18	V
Output Pin Forward Voltage	$V_{OUT}$	Voltage delta between supply and output must not exceed 24 V	24	V
All Other Pins Forward Voltage [2]	$V_{IN}$		3.6	V
Output and All Other Pins Reverse Voltage [2]	$V_R$		-0.5	V
Operating Ambient Temperature	$T_A$	L range	-40 to 150	$^{\circ}\text{C}$
Maximum Junction Temperature	$T_{J(max)}$		165	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$		-65 to 170	$^{\circ}\text{C}$

[1] Stresses beyond the Absolute Maximum Ratings may result in permanent device damage.

[2] "All Other Pins" refer to the pins that are driven by the device and should not be connected to external supplies.

### THERMAL CHARACTERISTICS: May require derating at maximum conditions, see application information

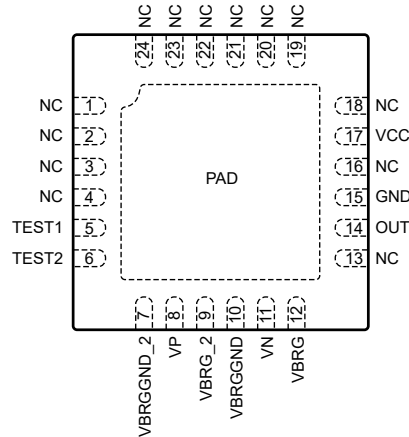
Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB based on JEDEC standard	136	$^{\circ}\text{C}/\text{W}$
		Four-layer PCB based JEDEC standard	37	$^{\circ}\text{C}/\text{W}$

[3] Additional thermal information available on the Allegro website.

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### PINOUT DIAGRAMS AND TERMINAL LIST



Package ES, 24-Pin QFN Pinout Diagram

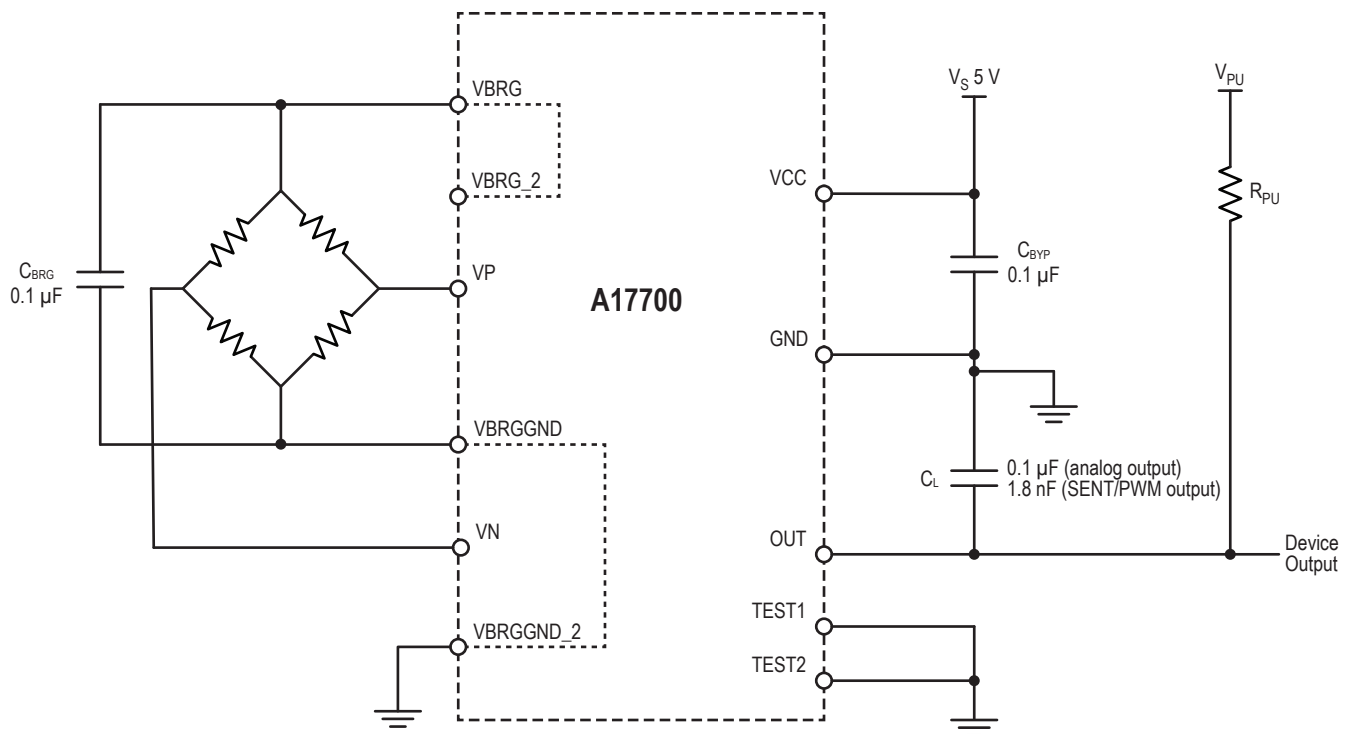
#### Terminal List Table

Number	Name	Function
1 to 4	NC	No internal connection <sup>[1]</sup>
5	TEST1	Factory Test Pin 1; connect to GND
6	TEST2	Factory Test Pin 2; connect to GND
7	VBRGGND_2	2nd GND pin for the bridge <sup>[2]</sup>
8	VP	Positive bridge output
9	VBRG_2	2nd bridge supply pin <sup>[3]</sup>
10	VBRGGND	GND pin for the bridge
11	VN	Negative bridge output
12	VBRG	Bridge supply
13	NC	No internal connection <sup>[1]</sup>
14	OUT	Analog / open drain output
15	GND	Ground
16	NC	No internal connection <sup>[1]</sup>
17	VCC	Supply voltage
18 to 24	NC	No internal connection <sup>[1]</sup>
–	PAD	Exposed thermal pad

<sup>[1]</sup> For increased ESD performance, connect NC (no connection) pins to GND.

<sup>[2]</sup> This is a second ground pin for the bridge intended for single layer PCB design. Internally connected to VBRGGND. Connect to GND if not used.

<sup>[3]</sup> This is a second bridge supply pin intended for single layer PCB design. Internally connected to VBRG. Leave floating if not used.



**Figure 2: Typical Application Circuit**

Note: VBRG and VCC decoupling caps must be mounted as close as possible to device package.  
For increased ESD performances, connect NC (no connection) pins to GND.

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