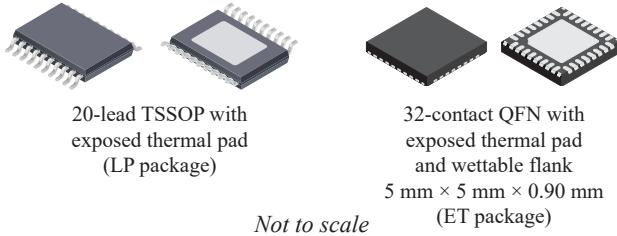


Three-Phase Sensorless Pump Driver IC

FEATURES AND BENEFITS

- AEC-Q100 qualified
- I²C serial port control
- Fast startup features
- Trapezoidal drive
- Sensorless (no Hall sensors required)
- Low R_{DS(ON)} power MOSFETs
- FG speed output
- Lock detection
- Soft start
- Overcurrent protection
- Overtoltage protection
- Diagnostic outputs
- Small form factor automotive pump

PACKAGES:



DESCRIPTION

The A89303 three-phase motor driver incorporates sensorless drive intended to drive low power automotive BLDC motors. A trapezoidal drive algorithm is implemented to minimize time to ramp up to maximum speed.

The device can be operated by PWM duty or I²C interface. The I²C serial port can be used to customize the startup and running operation via EEPROM.

The A89303 is available in a 20-lead TSSOP with exposed power pad (suffix LP) and a 32-contact 5 mm × 5 mm QFN with exposed thermal pad and wettable flank (suffix ET).

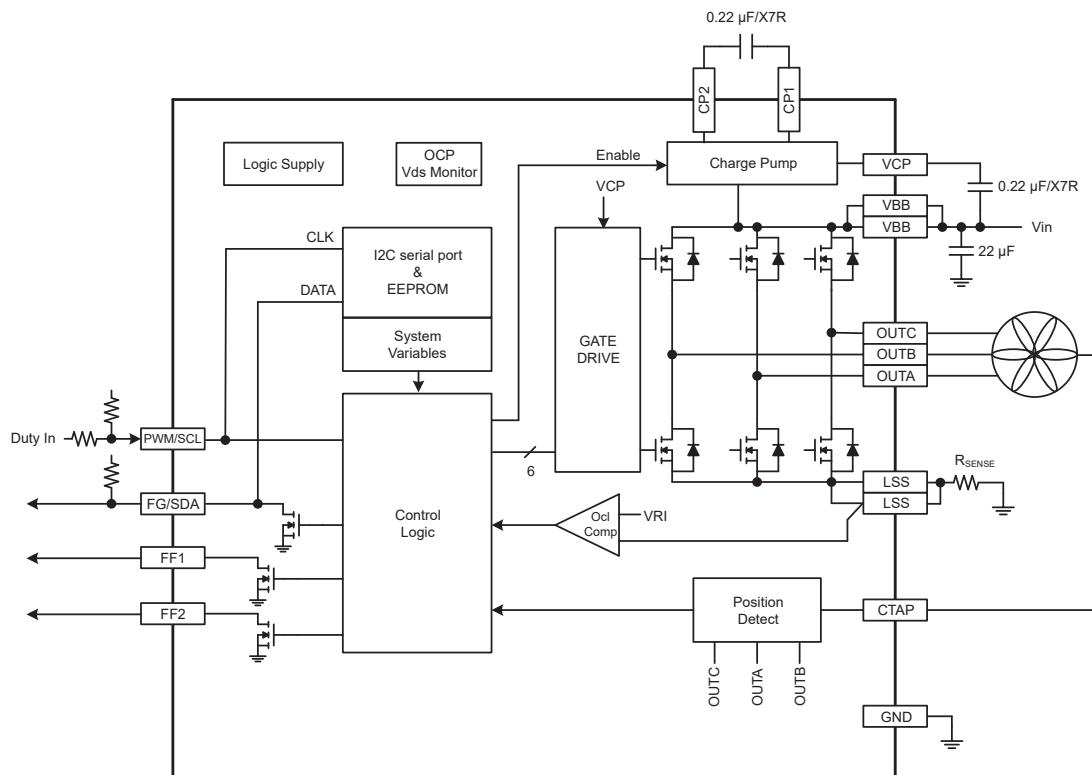


Figure 1: Typical Application

SPECIFICATIONS

SELECTION GUIDE

Part Number	Operating Temperature Range (T_A) (°C)	Packaging	Packing
A89303KLPTR-T	-40 to 125	20-lead TSSOP with exposed thermal pad	4000 pieces per 13-inch reel
A89303KETSR-J	-40 to 125	32-contact QFN with exposed thermal pad and wettable flank	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		-0.3 to 40	V
Logic Input Voltage Range	V_{IN}	PWM	-0.3 to 6	V
Logic Output	V_O	FG, FF1, FF2	-0.3 to 6	V
Output Current	I_{OUT}		3.6	A
LSS	V_{LSS}	DC	±0.36	V
		$t < 200$ ns	±2.5	V
Output Voltage	V_{OUT}	OUTA, OUTB, OUTC	-1.5 to $V_{BB} + 1$	V
CTAP			-0.6 to $V_{BB} + 0.6$	V
VCP			$V_{BB} - 0.3$ to $V_{BB} + 8$	V
CP1			-0.3 to $V_{BB} + 0.3$	V
CP2			$V_{BB} - 0.3$ to $V_{CP} + 0.3$	V
Maximum EEPROM write cycles	EEPROM _{W(MAX)}		1000	cycles
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		-55 to 150	°C
Operating Temperature Range	T_A		-40 to 125	°C

THERMAL CHARACTERISTICS

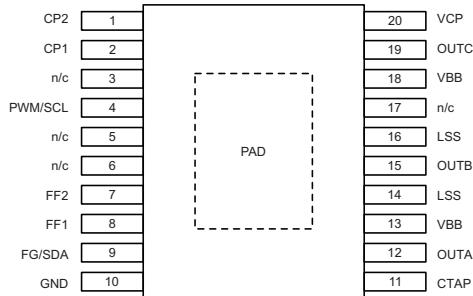
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	20-lead TSSOP (package LP), on 2-sided PCB 1-in. ² copper	35	°C/W
		32-contact QFN (package ET), on 2-sided PCB 1-in. ² copper	40	°C/W

*Additional thermal information available on the Allegro website.

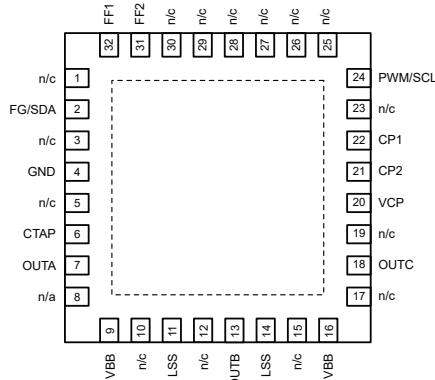
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PINOUT DIAGRAMS AND TERMINAL LIST TABLE



LP Package Pinout



ET Package Pinout

Terminal List Table

Name	Number		Description
	LP	ET	
CP2	1	21	Charge pump capacitor
CP1	2	22	Charge pump capacitor
n/c	3	23	
PWM/SCL	4	24	Logic input – PWM duty or I2C clock
n/c	5	25, 26, 27	
n/c	6	28, 29, 30	
FF2	7	31	Logic output signal
FF1	8	32	Logic output signal
n/c	–	1	
FG/SDA	9	2	I/O – Speed output signal or I2C data
n/c	–	3	
GND	10	4	Ground
n/c	–	5	
CTAP	11	6	Motor common
OUTA	12	7	Motor terminal
n/c	–	8	
VBB	13	9	Input supply
n/c	–	10	
LSS	14	11	Low-side source connection
n/c	–	12	
OUTB	15	13	Motor terminal
LSS	16	14	Low-side source connection
n/c	17	15	
VBB	18	16	Input supply
n/c	–	17	
OUTC	19	18	Motor terminal
n/c	–	19	
VCP	20	20	Charge pump capacitor
PAD	–	–	Exposed pad for enhanced thermal dissipation; connect to GND pin

ELECTRICAL CHARACTERISTICS: Valid for $T_J = -40^{\circ}\text{C}$ to 125°C and $V_{\text{BB}} = 5.5$ to 40 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Load Supply Operating Range	V_{BB}	Driving	5.5	–	V_{BBOV}	V
		Operating	5.5	–	40	V
V _{BB} Supply Current	I_{BB}	Active mode (PWM duty < DC_ON)	–	8.5	12	mA
Charge Pump	V_{CP}	Relative to V_{BB} , $V_{\text{BB}} = 8$ V	6.5	7	7.7	V
		Relative to V_{BB} , $V_{\text{BB}} = 5.5$ V	4	5	–	V
POWER DRIVER						
Total Driver On-Resistance (Sink + Source)	$R_{\text{DS(ON)}}$	$I_{\text{OUT}} = 1.5$ A, $T_J = 25^{\circ}\text{C}$, $V_{\text{BB}} = 12$ V	–	300	–	mΩ
		$I_{\text{OUT}} = 1.5$ A, $T_J = 125^{\circ}\text{C}$, $V_{\text{BB}} = 12$ V	–	450	520	mΩ
		Source Driver, $T_J = 25^{\circ}\text{C}$, $V_{\text{BB}} = 12$ V	–	150	–	mΩ
		Sink Driver, $T_J = 25^{\circ}\text{C}$, $V_{\text{BB}} = 12$ V	–	150	–	mΩ
Motor PWM Frequency	f_{PWM}		23.3	24.5	25.7	kHz
MOTOR CONTROL LOGIC						
PWM Input Frequency Range	f_{PWMIN}		2.1	–	45	kHz
Duty Cycle On Threshold	DC_{ON}		9.5	10	10.5	%
Duty Cycle Off Threshold	DC_{OFF}		7	7.4	8	%
External PWM Delay ON	$t_{\text{PWM_ON}}$		494	520	546	μs
External PWM Delay OFF	$t_{\text{PWM_OFF}}$		494	520	546	μs
PROTECTION CIRCUITS						
V _{BB} Undervoltage Threshold	V_{BBUVLO}	V_{BB} rising	4.7	4.85	5	V
V _{BB} Undervoltage Hysteresis	V_{BBHYS}		400	500	600	mV
V _{BB} Overvoltage	V_{BBOV}	V_{BB} rising	29	–	31.5	V
V _{BB} Overvoltage Hysteresis	V_{BBOVHYS}		1.5	2	2.5	V
V _{CP} UVLO	V_{CPUVLO}	V_{CP} rising	3.6	3.85	4.1	V
V _{CP} UVLO Hysteresis	V_{CPUVHYS}		200	–	400	mV
Charge Pump Power Up Time [2]	t_{VCPUV}		–	80	400	μs
POR Delay Time [2]	$t_{\text{POR_DELAY}}$		–	80	90	μs
Overcurrent Threshold	V_{OCL}	$V_{\text{RI}} = 160$ mV	–5	0	5	%
Overcurrent Protection	I_{OCP}		5	–	–	A
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	165	175	185	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{\text{JTSD}} - \Delta T_J$	–	20	–	°C

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

[2] Ensured by design and characterization, not production tested

Continued on next page...

ELECTRICAL CHARACTERISTICS (continued): Valid for $T_J = -40^{\circ}\text{C}$ to 125°C and $V_{BB} = 5.5$ to 40 V , unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC/INPUT OUTPUT/I²C						
Input Current (PWM, FG)	I_{IN}	$V_{IN} = 0$ to 5.5 V	-5	<1	5	μA
Logic Input Low Level	V_{IL}		0	-	0.8	V
Logic Input High Level	V_{IH}		2	-	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Saturation Voltage	V_{SAT}	$I = 5\text{ mA}$	-	-	0.3	V
Logic Output Leakage (FG, FF1, FF2)	I_{FG}	$V = 5.5\text{ V}$, switch OFF	-	-	5	μA
I²C TIMING						
SCL Clock Frequency	f_{CLK}		8	-	400	kHz
Bus Free-Time Between Stop/Start	t_{BUF}		1.3	-	-	μs
Hold Time Start Condition	$t_{HD:STA}$		0.6	-	-	μs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	-	-	μs
SCL Low Time	t_{LOW}		1.3	-	-	μs
SCL High Time	t_{HIGH}		0.6	-	-	μs
Data Setup Time	$t_{SU:DAT}$		100	-	-	ns
Data Hold Time	$t_{HD:DAT}$		0	-	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	-	-	μs

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

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