



Three-Phase MOSFET Driver System IC

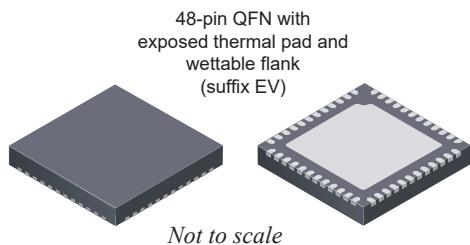
FEATURES AND BENEFITS

- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low supply voltage operation
- Programmable gate drive voltage and strength
- 5.5 to 50 V supply voltage operating range
- Integrated logic supply
- Current sense amplifier with programmable gain and offset
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Integrated bemf state comparators
- LIN/PWM physical interface with Wake
- Programmable logic supply regulator with current limit
- MCU Window watchdog and reset
- Ignition switch interface
- Diagnostics, status, voltage, and temperature feedback
- Developed in accordance with ISO 26262:2011

APPLICATIONS

- Automotive fuel, oil, and urea pumps
- Automotive fans and blowers

PACKAGES:



DESCRIPTION

The AMT49105 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads such as BLDC motors. Full control over all six power MOSFETs in the three-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation.

The AMT49105 is designed to provide the gate drive, supply, and peripheral functions in a system where a small microcontroller provides the motor control, communication interface to a central ECU and intelligent fault and status handling. The AMT49105 provides the supply and watchdog for the microcontroller and the high voltage interfaces between the microcontroller and the central ECU and ignition switch. An ISO17987 (LIN 2.0) and SAE J2602 compliant physical interface is provided for systems using LIN bus communications. This can also operate as a PWM interface for PWM communication systems.

A unique charge pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 7 V and allows the AMT49105 to operate with a reduced gate drive down to 5.5 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

A single sense amplifier with programmable gain and offset provides current sensing using a single low-side resistive shunt.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults and can protect the power switches under most short-circuit conditions.

The AMT49105 is supplied in a 48-terminal wettable flank QFN package (suffix EV). This package is lead (Pb) free with 100% matte-tin leadframe plating.

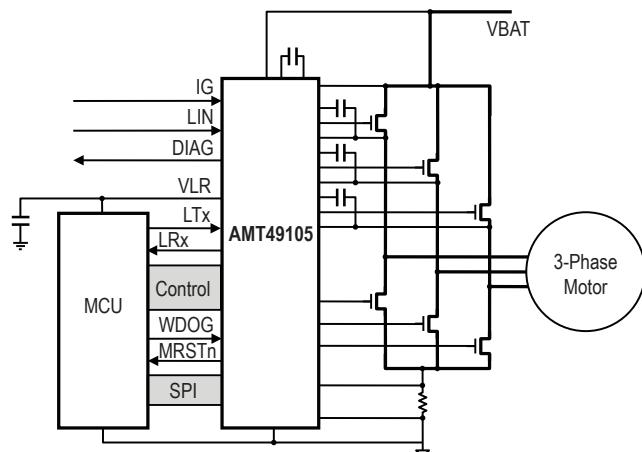


Figure 1: Typical Application

SELECTION GUIDE

| Part Number | Packing | Package |
|-----------------|--------------------------------|---|
| AMT49105KEVTR-J | 1000 pieces per 7-inch reel | 7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank |

**Table of Contents**

| | | | |
|---|----|---|----|
| Features and Benefits..... | 1 | Serial Status Register | 35 |
| Description | 1 | Diagnostics Registers | 35 |
| Package | 1 | DIAG Diagnostic Output..... | 35 |
| Selection Guide | 2 | Chip-Level Diagnostics | 36 |
| Absolute Maximum Ratings | 3 | Chip Fault State: Internal Logic Undervoltage (POR) | 36 |
| Thermal Characteristics | 3 | Chip Fault State: Overtemperature | 36 |
| Pinout Diagram and Terminal List | 4 | Chip Fault State: Serial Error | 37 |
| Functional Block Diagram | 5 | Chip Fault State: EEPROM..... | 37 |
| Electrical Characteristics | 6 | Operational Monitors | 37 |
| Sense Amplifier Voltage Definitions | 15 | Monitor: V_{BB} Supply Undervoltage..... | 37 |
| Timing Diagrams..... | 15 | Monitor: V_{REG} Undervoltage | 37 |
| Logic Truth Tables | 17 | Monitor: V_{LR} Undervoltage..... | 38 |
| Functional Description | 18 | Monitor: V_{IO} Undervoltage | 38 |
| Input and Output Terminal Functions | 19 | Monitor: Temperature Warning | 38 |
| Supplies and Regulators..... | 20 | Monitor: Microcontroller Watchdog..... | 38 |
| Main Power Supply..... | 20 | Monitor: ENABLE Timeout..... | 38 |
| VLR Regulator | 20 | Monitor: IG Input | 39 |
| Pump Regulator | 21 | Power Bridge Faults | 40 |
| Operating Modes | 22 | Bridge: Overcurrent Detect | 40 |
| LIN Mode | 22 | Bridge: Bootstrap Capacitor Undervoltage Fault..... | 40 |
| PWM Mode | 22 | Bridge: MOSFET V_{DS} Overvoltage Fault | 41 |
| Programming Mode | 22 | Fault Action | 42 |
| Low Power Sleep State..... | 22 | Fault Masks | 43 |
| Microcontroller Reset and Watchdog | 23 | Diagnostic and System Verification | 44 |
| Microcontroller Reset | 23 | On-Line Verification | 44 |
| Microcontroller Watchdog | 23 | System Clock Frequency Verification | 44 |
| LIN Physical Interface..... | 25 | System Clock Operation Verification | 44 |
| Gate Drives | 27 | Off-Line Verification | 44 |
| Gate Drive Voltage Regulation..... | 27 | All Gate Drives Off..... | 44 |
| Bootstrap Supply | 27 | MOSFET Active Monitor | 44 |
| Bootstrap Charge Management | 27 | Motor Direction | 45 |
| Top-Off Charge Pump..... | 27 | Serial Interface | 46 |
| High-Side Gate Drive..... | 28 | Configuration and Control Registers | 49 |
| Low-Side Gate Drive | 28 | Mask Registers..... | 50 |
| Gate Drive Passive Pull-Down..... | 28 | Verification Register | 50 |
| Gate Drive Control | 28 | Status and Diagnostic Registers | 50 |
| Dead Time | 30 | Diagnostic Registers | 50 |
| Logic Control Inputs | 31 | Status Register | 51 |
| Output Enable / Disable | 31 | Readback Register..... | 52 |
| Bridge Switch | 32 | Nonvolatile Memory | 52 |
| BEMF Zero Crossing Multiplex Output..... | 32 | Input/Output Structures | 70 |
| Current Sense Amplifiers | 34 | Layout Recommendations..... | 71 |
| Diagnostics | 35 | Package Outline Drawing..... | 72 |

ABSOLUTE MAXIMUM RATINGS [1][2]

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---------------------|---|---|------|
| Supply Voltage | V _{BB} | V _{BB} | -0.3 to 50 | V |
| Between Ground Terminals | - | Connect GND terminals together at package | -0.1 to 0.1 | V |
| Pumped Regulator Terminal | V _{REG} | V _{REG} | -0.3 to 16 | V |
| Charge Pump Capacitor Terminal | V _{CP1} | CP1 | -0.3 to 16 | V |
| Charge Pump Capacitor Terminal | V _{CP2} | CP2 | -0.3 to 16 | V |
| Logic Regulator Output | V _{LR} | V _{LR} | -0.3 to 6 | V |
| LIN Bus Interface | V _{LIN} | LIN | -40 to 50 | V |
| Logic Inputs | - | All logic inputs except IG | -0.3 to 6 | V |
| Logic Input | V _{IG} | IG | -4 to 50 | V |
| Logic Outputs | - | All logic outputs except DIAG | -0.3 to 6 | V |
| Logic Output | V _{DIAG} | DIAG | -0.3 to 50 | V |
| Bridge Drain Monitor Terminals | V _{BRG} | V _{BRG} | -5 to 55 | V |
| Switched Bridge Terminal | V _{BRS} | BRSW | -0.3 to 55 | V |
| Bootstrap Supply Terminals | V _{Cx} | CA, CB, CC | -0.3 to V _{REG} +50 | V |
| High-Side Gate Drive Output Terminals | V _{GHx} | GHA, GHB, GHC | V _{CX} - 16 to V _{CX} + 0.3 | V |
| | | GHA, GHB, GHC (Transient) | -18 to V _{CX} + 0.3 | V |
| Motor phase terminals | V _{Sx} | SA, SB, SC | V _{CX} - 16 to V _{CX} + 0.3 | V |
| | | SA, SB, SC (Transient) | -18 to V _{CX} + 0.3 | V |
| Low-side gate drive output terminals | V _{GLx} | GLA, GLB, GLC | V _{REG} - 16 to 18 | V |
| | | GLA, GLB, GLC (Transient) | -18 to V _{CX} + 0.3 | V |
| Bridge low-side source terminals | V _{LSS} | LSSA, LSSB, LSSC | V _{REG} - 16 to 18 | V |
| | | LSSA, LSSB, LSSC (Transient) | -8 to 18 | V |
| Sense Amplifier Inputs | V _{CSI} | CSP, CSM | -4 to 6.5 | V |
| Sense Amplifier Output | V _{CSI} | CSO | -0.3 to 6.5 | V |
| Ambient Operating Temperature Range | T _A | | -40 to 150 | °C |
| Maximum Continuous Junction Temperature | T _{J(max)} | | 165 | °C |
| Transient Junction Temperature | T _{Jt} | Over temperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization. | 180 | °C |
| Storage Temperature Range | T _{stg} | | -55 to 150 | °C |

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.

[2] Lowercase "x" in terminal names and symbols indicates a variable sequence character.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

| Characteristic | Symbol | Test Conditions [4] | Value | Unit |
|-------------------------------|------------------|--|-------|------|
| EV Package Thermal Resistance | R _{θJA} | 4-layer PCB based on JEDEC standard | 24 | °C/W |
| | | 2-layer PCB with 3.8 in. ² of copper area each side | 44 | °C/W |
| | R _{θJP} | | 2 | °C/W |

[4] Additional thermal information available on the Allegro website.

Per visualizzare il catalogo completo siete invitati ad effettuare il login sul sito oppure ad effettuare la registrazione gratuita.