

Three-Phase Sensorless Fan Driver IC

FEATURES AND BENEFITS

- AEC-Q100 qualified
- Speed curve configuration via EEPROM
- I²C serial port
- Sinusoidal modulation for reduced audible noise and low vibration
- Sensorless (no Hall sensors required)
- Low R_{DS(ON)} power MOSFETs
- 3.3 V / 20 mA linear regulator
- PWM or analog speed input
- FG speed output
- Slew rate control
- Lock detection
- Soft start
- Low power standby mode
- Overcurrent protection
- Overvoltage protection

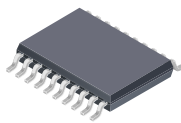
DESCRIPTION

The A5947-B three phase motor driver IC incorporates sensorless sinusoidal drive to minimize vibration for a wide variety of fan applications. Sensorless control eliminates the requirement for Hall sensors.

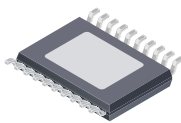
A flexible closed-loop speed control system is integrated into the IC. EEPROM is used to tailor the common functions of the fan speed curve to a specific application. This eliminates the requirement for a microprocessor-based system and minimizes programming requirements.

The A5947-B is available in a 28-contact 5 mm × 5 mm QFN with exposed thermal pad (suffix ET) and a 20-lead TSSOP with exposed thermal pad (suffix LP).

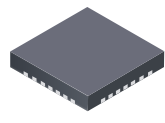
PACKAGES:



20-lead TSSOP
with exposed thermal pad
(LP package)



Not to scale



28-contact QFN
with exposed thermal pad
5 mm × 5 mm × 0.90 mm
(ET package)

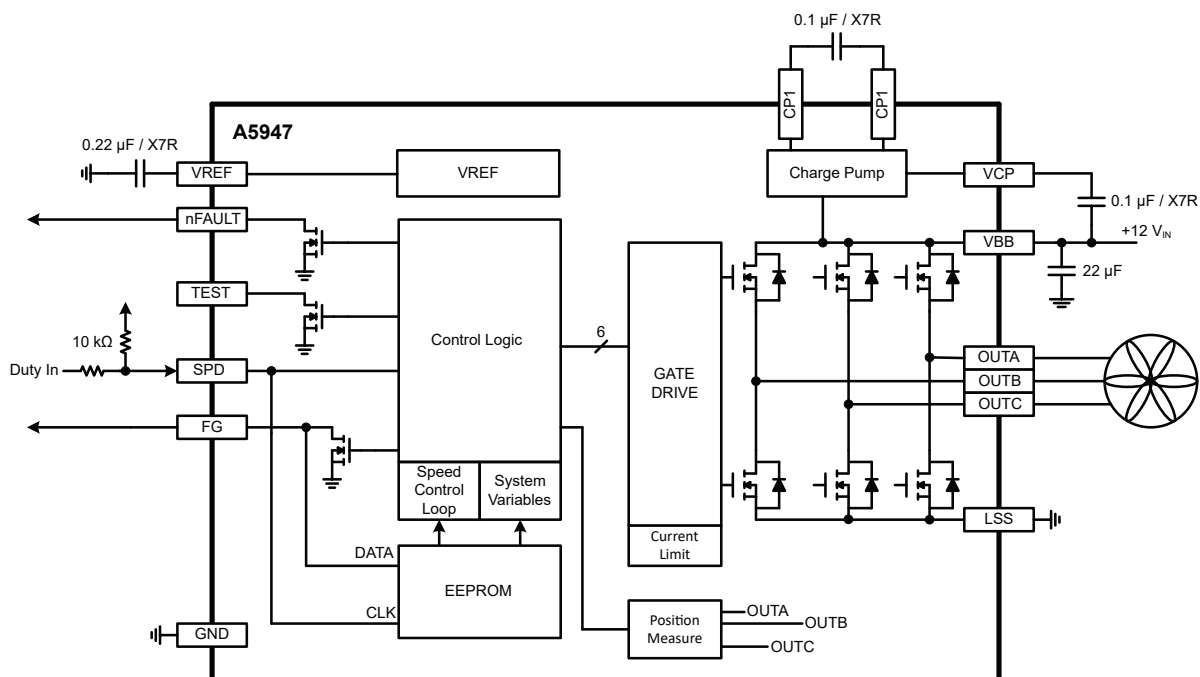


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Operating Temperature Range (T _A) (°C)	Packaging	Packing
A5947KLPTR-B-T	-40 to 125	20-lead TSSOP with exposed power pad	4000 pieces per 13-inch reel



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V _{BB}		-0.7 to 40	V
Logic Input Voltage Range	V _{IN}	SPD	-0.3 to 6	V
Logic Output	V _O	FG, nFAULT, TEST	-0.3 to 6	V
Output Current	I _{OUT}		3.6	A
Output Voltage	V _{OUT}	OUTA, OUTB, OUTC	V _{BB} + 1	V
VCP	V _{CP}		V _{BB} - 0.3 to V _{BB} + 8	V
CP1	V _{CP1}		-0.3 to V _{BB} + 0.3	V
CP2	V _{CP2}		V _{BB} - 0.3 to V _{CP} + 0.3	V
Maximum EEPROM write cycles	EEPROM _{W(MAX)}		1000	cycles
Junction Temperature	T _J		150	°C
Storage Temperature Range	T _{stg}		-55 to 150	°C
Operating Temperature Range	T _A	Range G	-40 to 105	°C
		Range K	-40 to 125	°C

THERMAL CHARACTERISTICS

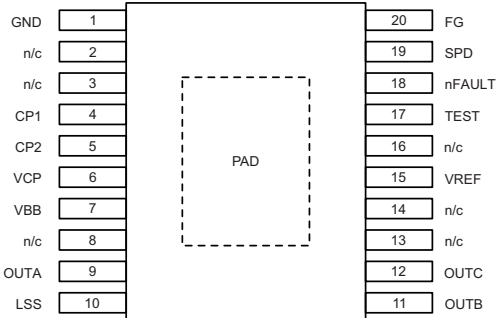
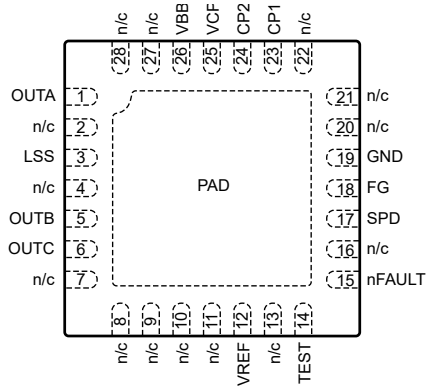
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	R _{θJA}	28-contact QFN (package ET), on 2-sided PCB 1-in. ² copper	40	°C/W
		20-lead TSSOP (package LP), on 2-sided PCB 1-in. ² copper	34	°C/W

*Additional thermal information available on the Allegro website.

Table of Contents

Features and Benefits.....	1	Basic Operation	6
Description	1	Flexible Speed Curve Options	8
Packages	1	EEPROM Map	11
Typical Application.....	1	Serial Port Control Option	13
Specifications	2	Serial Port	15
Selection Guide	2	I ² C Timing Diagrams	15
Absolute Maximum Ratings.....	2	Write Command.....	16
Thermal Characteristics	2	Read Command	16
Pinout Diagram and Terminal List Table	3	Programming EEPROM.....	17
Electrical Characteristics	4	Pin Diagrams.....	19
Functional Description	6	Package Outline Drawings	20

PINOUT DIAGRAMS AND TERMINAL LIST TABLE



ET Package Pinouts

LP Package Pinouts

Terminal List Table

Terminal Number		Name	Function
ET Package	LP Package		
19	1	GND	Ground
20,21,22	2,3	n/c	No connect
23	4	CP1	Charge pump capacitor
24	5	CP2	Charge pump capacitor
25	6	VCP	Charge pump capacitor
26	7	VBB	Input supply
27,28	8	n/c	No connect
1	9	OUTA	Motor terminal
2		n/c	No connect
3	10	LSS	Low side source connection
4		n/c	No connect
5	11	OUTB	Motor terminal
6	12	OUTC	Motor terminal
7,8,9,10,11	13,14	n/c	No connect
12	15	VREF	Reference voltage output
13	16	n/c	No connect
14	17	TEST	Logic output signal
15	18	nFAULT	Logic output signal
16		n/c	No connect
17	19	SPD	Logic input – speed demand
18	20	FG	Logic output signal
–	–	PAD	Exposed pad for enhanced thermal dissipation

ELECTRICAL CHARACTERISTICS [1]: Valid for $T_A = 25^\circ\text{C}$ (G version) or $T_A = -40^\circ\text{C}$ to 125°C (K version); $V_{BB} = 4$ to 40 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Supply Current	I_{BB}	Active mode (PWM duty < DC_ON)	–	13.5	15	mA
	I_{BBS}	$V_{BB} = 34$ V, standby mode	–	10	40	μA
Reference Voltage	V_{REF}	$I = 0$ to 20 mA, $V_{BB} = 6$ to 40 V	3.15	3.3	3.45	V
Charge Pump	V_{CP}	Relative to V_{BB} , $V_{BB} = 8$ V	6.5	7.2	7.7	V
		Relative to V_{BB} , $V_{BB} = 4$ V	3.5	3.7	–	V
POWER DRIVER						
Total Driver On-Resistance (Sink + Source)	$R_{DS(ON)}$	$I = 1.5$ A, $T_J = 25^\circ\text{C}$, $V_{BB} = 12$ V	–	510	–	m Ω
		$I = 1.5$ A, $T_J = 125^\circ\text{C}$, $V_{BB} = 12$ V	–	760	860	m Ω
		$I = 1.5$ A, $T_J = 25^\circ\text{C}$, $V_{BB} = 4$ V	–	680	–	m Ω
		$I = 1.5$ A, $T_J = 125^\circ\text{C}$, $V_{BB} = 4$ V	–	950	1200	m Ω
Source Driver On-Resistance	$R_{DS(ON)SRC}$	$T_J = 125^\circ\text{C}$, $V_{BB} = 12$ V	–	380	–	m Ω
Sink Driver On-Resistance	$R_{DS(ON)SNK}$	$T_J = 125^\circ\text{C}$, $V_{BB} = 12$ V	–	380	–	m Ω
Motor PWM Frequency	f_{PWM}	$T_A = 25^\circ\text{C}$	23.52	24.5	25.48	kHz
		$T_A = -40^\circ\text{C}$ to 125°C	23.03	–	25.97	kHz
SPEED CONTROL						
PWM Input Frequency Range	f_{PWHMIN}		34	–	65000	Hz
Duty Cycle On Threshold	DC_{ON}	Relative to target	–0.5	–	0.5	%
Duty Cycle Off Threshold	DC_{OFF}	Relative to target	–0.5	–	0.5	%
SPD Standby Threshold (Analog)	V_{SPDTH}		0.43	0.7	1	V
SPD On Threshold	V_{SPDON}	$DC_{ON} = 10\%$	210	240	270	mV
SPD Off Threshold	V_{SPDOFF}	$DC_{OFF} = 8\%$	160	190	220	mV
SPD Max	V_{SPDMAX}		–	2.49	–	V
SPD ADC Resolution	V_{SPDLSB}		–	4.892	–	mV
SPD ADC Accuracy	SPD_{ACC}	$V_{BB} = 12$ V, $V_{SPD} = 0.2$ V to V_{SPDMAX}	–10	–	10	LSB
Speed Setpoint	f_{SPD}	Duty cycle input; $T_A = 25^\circ\text{C}$	–5	–	5	%
		Duty cycle input; $T_A = -40^\circ\text{C}$ to 125°C	–7	–	7	%

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid for $T_A = 25^\circ\text{C}$ (G version) or $T_A = -40^\circ\text{C}$ to 125°C (K version);
 $V_{BB} = 4$ to 40 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION CIRCUITS						
Lock Timing	t_{LOCK}	Relative to target	-5	-	5	%
VBB Undervoltage Threshold	V_{BBUVLO}	UVLO = 0, V_{BB} rising	3.7	3.85	4	V
		UVLO = 1, V_{BB} rising	8.4	8.65	9.02	V
VBB Undervoltage Hysteresis	V_{BBHYS}	UVLO = 0	160	300	480	mV
		UVLO = 1	1.8	2	2.2	V
Overcurrent Limit	I_{OCL}	$V_{\text{BB}} = 8$ V	2.5	3	3.5	A
Overcurrent Protection	I_{OCP}		3.94	7	-	A
VBB Overvoltage	V_{BBOV}	VBBOV = 0, V_{BB} rising	18.2	19	19.8	V
		VBBOV = 1, V_{BB} rising	36.8	37.5	39.3	V
VBB Overvoltage Hysteresis	V_{BBOVHYS}		1.5	2	2.5	V
VREF UVLO	V_{REFUVLO}	V_{REF} rising	2.9	3	3.15	V
VREF UVLO Hysteresis	V_{REFHYS}		150	250	350	mV
VREF Overcurrent Limit	V_{REFOCL}	$V_{\text{BB}} = 12$ V	30	65	120	mA
VCP UVLO	V_{CPUVLO}	V_{CP} rising	2.5	2.75	3.0	V
VCP UVLO HYS	$V_{\text{CPUVLOHYS}}$		-	110	-	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	$^\circ\text{C}$
Thermal Shutdown Hysteresis	ΔT_{J}	Recovery = $T_{\text{JTSD}} - \Delta T_{\text{J}}$	-	20	-	$^\circ\text{C}$
LOGIC/INPUT OUTPUT/I²C						
Logic Input Current (SPD, FG)	I_{IN}	$V_{\text{IN}} = 0$ to 5.5 V	-5	<1	5	μA
Logic Input Low Level	V_{IL}		0	-	0.8	V
Logic Input High Level	V_{IH}		2	-	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Saturation Voltage (FG, RD)	V_{SAT}	$I = 5$ mA	-	-	0.3	V
Output Leakage	I_{OUT}	$V = 5.5$ V, switch OFF	-	-	5	μA
I²C TIMING						
SCL Clock Frequency	f_{CLK}		3	-	400	kHz
Bus Free-Time Between Stop/Start	t_{BUF}		1.3	-	-	μs
Hold Time Start Condition	$t_{\text{HD:STA}}$		0.6	-	-	μs
Setup Time for Start Condition	$t_{\text{SU:STA}}$		0.6	-	-	μs
SCL Low Time	t_{LOW}		1.3	-	-	μs
SCL High Time	t_{HIGH}		0.6	-	-	μs
Data Setup Time	$t_{\text{SU:DAT}}$		100	-	-	ns
Data Hold Time	$t_{\text{HD:DAT}}$		0	-	900	ns
Setup Time for Stop Condition	$t_{\text{SU:STO}}$		0.6	-	-	μs

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

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