50 V Ultra Low Noise FOC Motor Controller

FEATURES AND BENEFITS

- Code-free sensorless field-oriented control (FOC)
- I²C interface for speed control and status readback
- Ultra-quiet low speed operation
- Proprietary non-reverse fast startup
- Soft-On Soft-Off (SOSO) for quiet operation
- Analog / PWM / Clock mode speed control
- Closed-loop speed control
- Configurable current limit
- Windmill startup operation
- Lock detection
- Short-circuit protection (OCP)
- Brake and direction inputs
- Adjustable gate drive

APPLICATIONS

- Ceiling fans
- Pedestal fans
- Bathroom exhaust fans
- Home appliance fans and pumps

DESCRIPTION

The A89301 is a 3-phase, sensorless, brushless DC (BLDC) motor driver (gate driver) which can operate from 5.5 to 50 V.

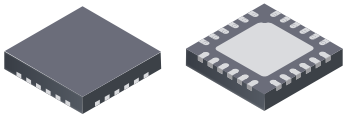
A field-oriented control (FOC) algorithm is fully integrated to achieve the best efficiency and acoustic noise performance. The device optimizes the motor startup performance in a stationary condition, a windmill condition, and even in a reverse windmill condition.

Motor speed is controlled through analog, PWM, or CLOCK input. Closed-loop speed control is optional, and RPM-to-clock frequency ratio is programmable.

A simple I²C interface is provided for setting motor-rated voltage, rated current, rated speed, resistance, and startup profiles. The I²C interface is also used for on/off control, speed control, and speed readback.

The A89301 is available in a 24-contact 4 mm × 4 mm QFN with exposed thermal pad (suffix ES). The package is lead (Pb) free, with 100% matte-tin leadframe plating.

PACKAGE



Not to scale

24-contact QFN
with exposed thermal pad
4 mm × 4 mm × 0.75 mm
(ES package)

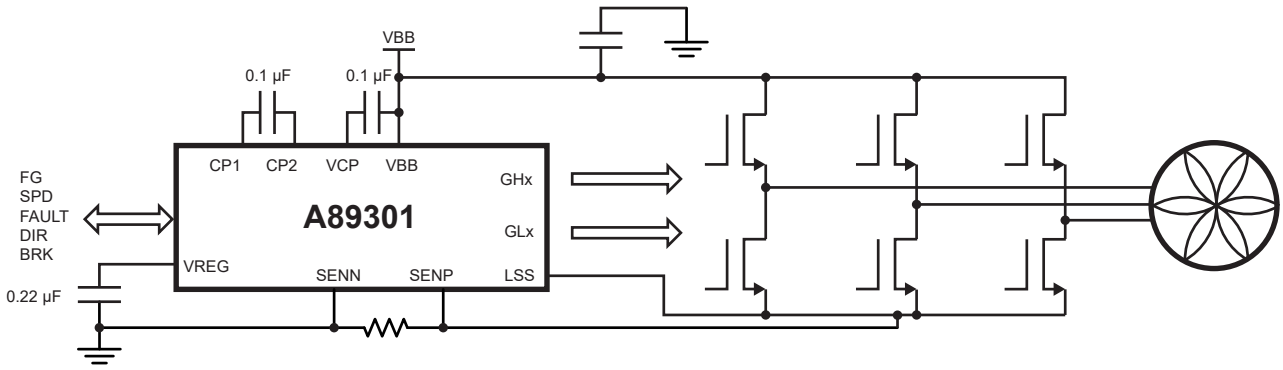


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Ambient Temperature Range (T_A) (°C)	Packaging	Packing
A89301GESSR	–40 to 105	24-contact QFN with exposed thermal pad	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		50	V
Logic Input Voltage Range	V_{IN}	SPD, BRAKE, DIR	–0.3 to 6	V
Logic Output	V_O	FG, FAULT (I < 5 mA)	6	V
LSS	V_{LSS}	DC	±500	mV
		t_W < 500 ns	±4	V
VREG	V_{REG}		0 to 4	V
SENN, SENP	V_{SENN}, V_{SENP}	DC	±500	mV
		t_W < 500 ns	±4	V
Output Voltage	V_{OUT}	SA, SB, SC	–2 to V_{BB}+2	V
		SA, SB, SC, t_w < 50 ns	–4 to V_{BB}+4	V
GHx	V_{GHx}		V_{Sx}–0.3 to V_{CP}+0.3	V
GLx	V_{GLx}		V_{LSS}–0.3 to 8.5	V
VCP	V_{CP}		V_{BB}–0.3 to V_{BB}+8	V
CP1	V_{CP1}		–0.3 to V_{BB}+0.3	V
CP2	V_{CP2}		V_{BB}–0.3 to V_{CP}+0.3	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	24-contact QFN (package ES), on 2-sided PCB 1-in.^{2} copper	45	°C/W

*Additional thermal information available on the Allegro website.

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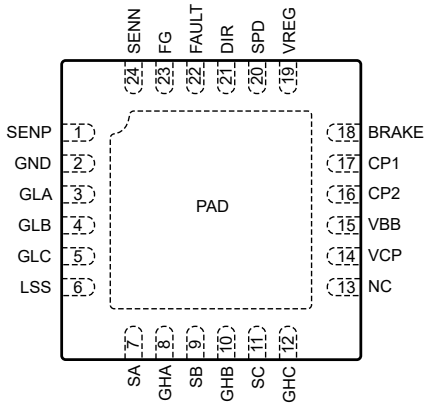
PINOUT DIAGRAM AND TERMINAL LIST



ES Package Pinouts

Terminal List Table

Terminal Number	Name	Function
16	CP2	Charge pump
17	CP1	Charge pump
18	BRAKE	Logic input
19	VREG	2.8 V regulator voltage
20	SPD	PWM or clock mode speed control
21	DIR	Direction control
22	FAULT	Fault indicator output
23	FG	Motor speed output
24	SENN	Current sense negative terminal
1	SENP	Current sense positive terminal
2	GND	Ground
3	GLA	Low-side gate drive output
4	GLB	Low-side gate drive output
5	GLC	Low-side gate drive output
6	LSS	Low-side source
7	SA	Motor output
8	GHA	High-side gate drive output
9	SB	Motor output
10	GHB	High-side gate drive output
11	SC	Motor output
12	GHC	High-side gate drive output
13	NC	No connect
14	VCP	Charge pump
15	VBB	Power supply
PAD	PAD	Exposed pad for enhanced thermal dissipation

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FUNCTIONAL BLOCK DIAGRAM

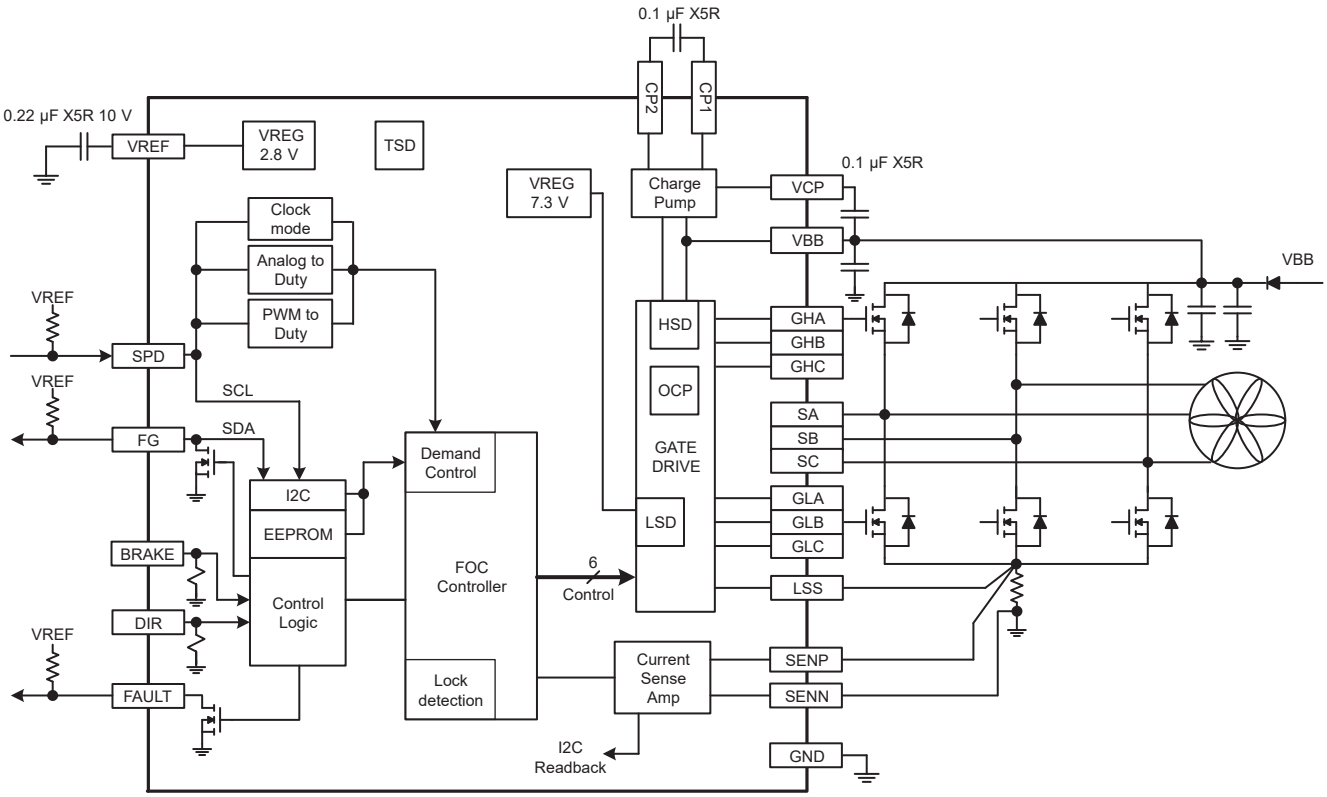

Figure 2: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS [1]: Valid over operating ambient temperature range and operating voltage range, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Supply Voltage Range	V_{BB}	Driving	5.5	–	48	V
		Operating	5.5	–	50	V
VBB Supply Current	I_{BB}	I_{VREG} = 0 mA	–	8	12	mA
		Standby mode	–	10	20	µA
Reference Voltage	V_{REG}	I_{OUT} = 10 mA	2.7	2.86	2.95	V
GATE DRIVE						
High Side Gate Drive Output	V_{GH}	V_{BB} = 8 V	6.5	6.8	–	V
		V_{BB} = 24 V	6.5	6.8	–	V
Low Side Gate Drive Output	V_{GL}	V_{BB} = 8 V	6.5	7.3	–	V
		V_{BB} = 24 V	6.5	7.3	–	V
Gate Drive Source Current	I_{SO}	V_{BB} = 8 V; level 0	–	15	–	mA
		V_{BB} = 8 V; level 1	–	30	–	mA
		V_{BB} = 8 V; level 2	–	55	–	mA
Gate Drive Sink Current	I_{SI}	V_{BB} = 8 V; level 0	–	30	–	mA
		V_{BB} = 8 V; level 1	–	60	–	mA
		V_{BB} = 8 V; level 2	–	105	–	mA
VDS SENSING FOR OCP						
VDS Comparator Threshold	V_{DS_THR}	level 0	–	1	–	V
		level 1	–	2	–	V
MOTOR DRIVE						
PWM Duty On Threshold	PWM_{ON}	Relative to target	–0.5	–	0.5	%
PWM Duty Off Threshold	PWM_{OFF}	Relative to target	–0.5	–	0.5	%
PWM Input Frequency Range	$f_{PWM(MIN)}$	PWM input frequency setting = 0	2.5	–	100	kHz
		PWM input frequency setting = 1	80	–	3200	Hz
Clock Input Frequency Range	f_{CLOCK}	CLOCK mode	1	–	2000	Hz
SPD Standby Threshold (Analog Enter)	$V_{SPD(TH_ENT)}$		50	100	150	mV
SPD Standby Threshold (Analog Exit)	$V_{SPD(TH_EXIT)}$		0.4	0.75	1	V
SPD On Threshold	$V_{SPD(ON)}$	ON/OFF setting = 10%	210	250	290	mV
SPD Max	$V_{SPD(MAX)}$		–	2.5	–	V
SPD ADC Resolution	$V_{SPDADC(RES)}$		–	9.78	–	mV
SPD ADC Accuracy	$V_{SPDADC(ACC)}$	V_{SPD} = 0.2 to 2.5 V	–40	–	40	mV
Speed Closed Loop Accuracy	$f_{SPD(ACC)}$	PWM mode or Analog mode	–5	–	5	%
		Clock mode	–0.1	–	0.1	rpm
Dead Time	t_{DT}	Code = 9	–	400	–	ns
Motor PWM Frequency	f_{PWM}	T_A = 25°C	23.3	24.4	25.3	kHz

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