Click here to ask about the production status of specific part numbers.

MAX77831

2.5V to 16V Input, 18W Output High-Efficiency Buck-Boost Converter

General Description

The MAX77831 is a high-efficiency, high-performance buck-boost converter targeted for systems requiring wide input voltage range (2.5V to 16V). It can supply 18W of continuous output power (for example, up to 2A at 9V (V_{IN} ≥ 4V)).

The IC is available in 5V default output voltage when using internal feedback resistors. The IC can also be configured to any default output voltages between 3V and 15V when using external feedback resistors. The output voltage is adjustable dynamically through the I^2C serial interface (see the *Output Voltage Configuration* section). The IC only operates in forced-PWM (FPWM) mode.

The SEL pin allows a single external resistor to program four different I^2C interface slave addresses, four different switching-current limit thresholds, and selection between external/internal feedback resistors. The different switching-current limit thresholds allow the use of lower profile and smaller external components that are optimized for a particular application. The use of external feedback resistors allows for a wider output voltage range and customizable output voltages at startup.

An optional I^2C serial interface allows dynamically controlling the output voltage, slew rate of the output voltage change, switching-current limit threshold, and switching frequency. The I^2C-programmed settings have priority over the R_{SEL} decoded settings.

The MAX77831 is available in a 2.86mm x 2.06mm 35-bump wafer level package (WLP).

Applications

- Non-Battery Powered Applications up to 16V Input
- Battery Powered Applications up to 16V Input with EN Control

Benefits and Features

- Wide Input Voltage Range: 2.5V to 16V
- Default Output Voltage
  - 5V with Internal Feedback Resistors
  - 3V to 15V with External Feedback Resistors
- Default 1.8MHz Switching Frequency
  - 1.5MHz and 1.2MHz Selectable through the I^2C Interface
- Forced-PWM (FPWM) Mode Operation Only
- I^2C-Programmable Output Voltage After Startup
  - 4.5V to 15V (Internal Feedback Resistors)
  - 3V to 15V (External Feedback Resistors, See Table 1)
- 18W of Continuous Output Power (V_{IN} ≥ 4V, V_{OUT} ≥ 5V)
- R_{SEL} Configuration
  - I^2C Interface Slave Address
  - Switching Current Limit Threshold
  - Internal/External Feedback Resistors
- I^2C Programming
  - Output Voltage (DVS)
  - Slew Rate of Output Voltage Change
  - Switching Current Limit Threshold
  - Switching Frequency
  - Power-OK (POK) Status and Fault Interrupt Masks
  - Internal Compensation
- Soft-Start
- Output Active Discharge
- Open-Drain Power-OK (POK) Monitor/Fault Condition Interrupt
- Protection Features
  - Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Overvoltage Protection (OVP)
  - Thermal Shutdown (THS)
- High Density Interconnect (HDI) PCB Not Required (See the *PCB Layout Guideline* Section)
- Available in 2.86mm x 2.06mm 35 WLP

Ordering Information appears at end of data sheet.

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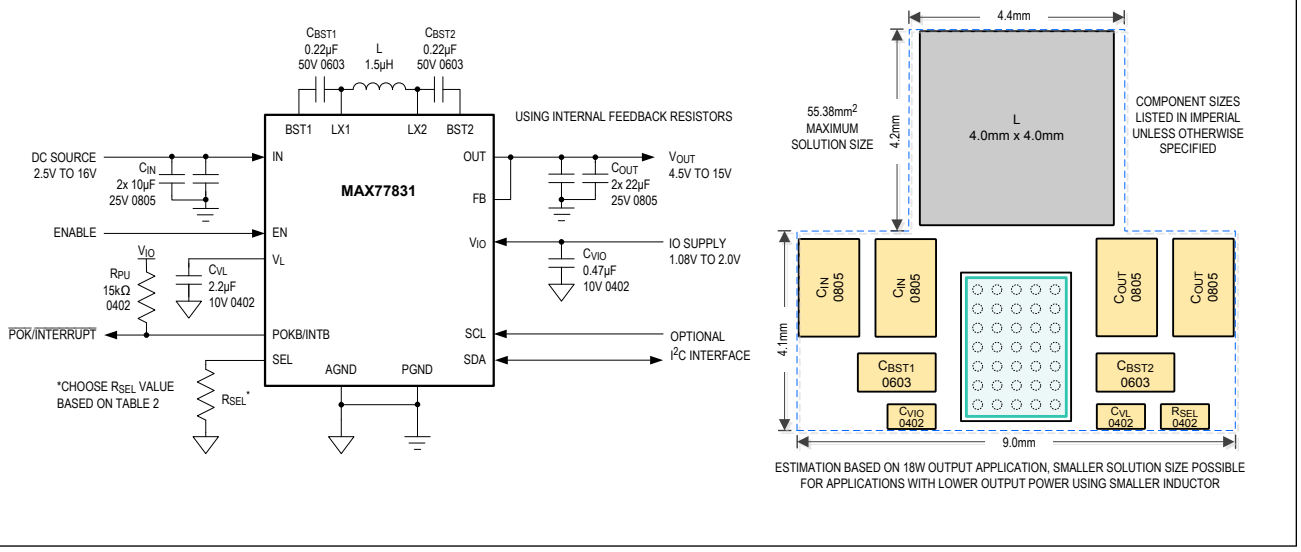
Simplified Block Diagram



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Absolute Maximum Ratings

IN, LX1, LX2, OUT, FB to PGND ..... -0.3V to +17.6V
BST1 to GND ..... -0.3V to +20V
BST1 to LX1 ..... -0.3V to +2.2V
BST2 to GND ..... -0.3V to +20V
BST2 to LX2 ..... -0.3V to +2.2V
EN, POK, SCL, SDA to AGND, PGND.....-0.3V to V_{IO} + 0.3V
V_L, V_{IO}, SEL to AGND, PGND ..... -0.3V to +2.0V
PGND to AGND ..... -0.3V to +0.3V
Continuous Power Dissipation
WLP Package (T_A = +70°C, derate 20.4mW/°C above +70°C (Note 1)) 1633mW
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C

Note 1: Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

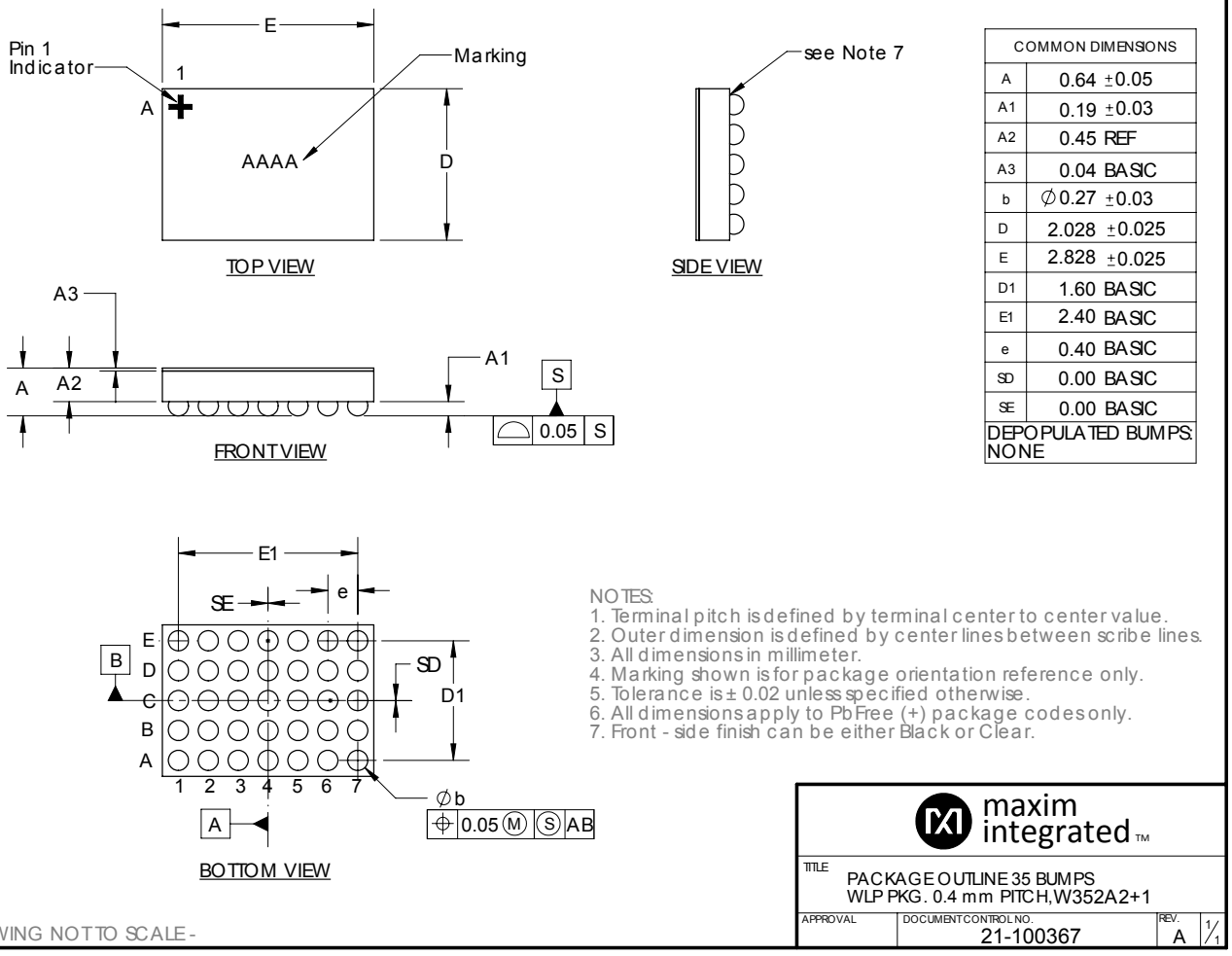
PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Operating Input Voltage Range	V_{IN}		2.5 to 16	V
Operating Junction Temperature	T_J		-40 to +125	ºC
Operating Ambient Temperature	T_A		-40 to +85	ºC

Note: These limits are not guaranteed.

Package Information

35 WLP

Package Code	W352A2+1
Outline Number	21-100367
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	∅0.27 ±0.03
D	2.028 ±0.025
E	2.828 ±0.025
D1	1.60 BASIC
E1	2.40 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to Pb Free (+) package codes only.
7. Front - side finish can be either Black or Clear.

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TITLE: PACKAGE OUTLINE 35 BUMPS WLP PKG. 0.4 mm PITCH, W352A2+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100367	A	1/1

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT VOLTAGE AND SUPPLY CURRENT							
Input Voltage Range	V_{IN}			2.5		16	V
Input Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{IN} rising		2.3	2.4	2.5	V
Input Undervoltage Lockout (UVLO) Hysteresis	V_{UVLO_HYS}	V_{UVLO_R} - V_{UVLO_F}			150		mV
Shutdown Supply Current	I_{SHDN}	EN = LOW, T_J = -40ºC to +85ºC			2	6	µA
Quiescent Supply Current	I_Q	EN = HIGH, R_{SEL}= short to GND, no switching			5		mA
OUTPUT VOLTAGE							
Output Voltage Regulation Range	V_{OUT}	Using internal feedback resistors		4.5		15	V
		Using external feedback resistors		3.0		15	
Output Voltage Accuracy	V_{OUT}	I_{OUT} = 0mA, using internal feedback resistors	V_{IN} = 2.5V to 16V, V_{OUT} = 4.5V to 15V, T_J = -40°C to +125ºC	-2.0		+1.5	%
V_L INTERNAL SUPPLY							
V_L Regulator Voltage	V_{VL}			1.65	1.8	1.89	V
V_{IO} SUPPLY							
V_{IO} Voltage Range	V_{VIO}			1.08		2.0	V
V_{IO} Valid Threshold	$V_{VIO\_VALID\_R}$	V_{IO} rising		0.965	1.02	1.08	V
	$V_{VIO\_VALID\_F}$	V_{IO} falling		0.85	0.9	0.955	
V_{IO} Bias Current	I_{VIO}	No I^2C interface (SDA and SCL unconnected)				2.0	µA
		f_{SCL} = f_{SDA} = 1MHz			50		
EN, POK							
EN Input LOW Voltage	V_{EN_IL}					0.3 x V_{VIO}	V
EN Input HIGH Voltage	V_{EN_IH}			0.7 x V_{VIO}			V
EN Internal Pulldown Resistance	R_{EN_PD}				800		kΩ
POK Output LOW Voltage	V_{POK_OL}	I_{POK} = 1mA				0.3	V
POK Rising Threshold	V_{POK_R}	V_{OUT} rising, expressed as percentage of target V_{OUT} voltage		90	95		%
POK Falling Threshold	V_{POK_F}	V_{OUT} falling, expressed as percentage of target V_{OUT} voltage			85		%

Electrical Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL PROTECTION							
Thermal Shutdown Threshold	T_{SHDN_R}	T_J rising (Note 3)			150		ºC
Thermal Shutdown Hysteresis	T_{SHDN_HYS}	T_{SHDN_R} - T_{SHDN_F} (Note 3)			15		ºC
BUCK-BOOST REGULATOR							
Switching Frequency	f_{SW}	I_{OUT} = 0mA	FREQ[1:0] = 00	1.128	1.20	1.272	MHz
			FREQ[1:0] = 01	1.41	1.50	1.59	
			FREQ[1:0] = 10 (default)	1.692	1.80	1.908	
Startup Delay Time	t_{SUDLY}	(Note 2)			100		µs
Soft-Start Time	t_{SS}	Measured from OUT start ramping to stop ramping during startup, C_{OUT} = 44µF, I_{OUT} = 0mA (Note 2)			2.0		ms
High-Side Switching Current Limit	I_{LIM}	ILIM[2:0] = 000 (Note 3)			7.00		A
		ILIM[2:0] = 001 (I^2C only, not available with R_{SEL}) (Note 3)			6.20		
		ILIM[2:0] = 010 (Note 3)			5.60		
		ILIM[2:0] = 011 (I^2C only, not available with R_{SEL}) (Note 3)			4.60		
		ILIM[2:0] = 100 (Note 3)			3.80		
		ILIM[2:0] = 101 (I^2C only, not available with R_{SEL})			2.73		
		ILIM[1:0] = 110			1.72		
		ILIM[2:0] = 111 (I^2C only, not available with R_{SEL})			0.98		
Skip Mode Switching Current Limit	I_{LIM_SKIP}				1.4		A
Line Regulation	$\Delta V/V_{IN}$	V_{IN} = 2.5V to 16V, V_{OUT} = 5V, I_{OUT} = 0mA and 1A			±0.3		%/V
Load Regulation	$\Delta V/I_{OUT}$	$V_{IN} \geq$ 4V, V_{OUT} = 5V, I_{OUT} = 0mA to 3A			±0.6		%/A
Internal Reference Voltage	V_{REF}	VREF[7:0] = 0x3D, code clamped below this level			0.299		V
		VREF[7:0] = 0x44, default value			0.333		
		VREF[7:0] = 0xCC, code clamped above this level			1.000		
Internal Reference Voltage Programmable Range	V_{REF}	VREF[7:0] = 0x3D to 0xCC		0.299		1.000	V

Electrical Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Reference DVS Ramp Rate	$\Delta V_{REF}/\Delta t$	SLEW_RATE[1:0] = 00, FREQ[1:0] = 10		4/3		mV/µs
		SLEW_RATE[1:0] = 00, FREQ[1:0] = 00 or 01		7/6		
		SLEW_RATE[1:0] = 01		2/3		
		SLEW_RATE[1:0] = 10		1/3		
		SLEW_RATE[1:0] = 11, FREQ[1:0] = 10		17/75		
		SLEW_RATE[1:0] = 11, FREQ[1:0] = 00 or 01		1/6		
FB Input Leakage Current	I_{FB_LK}		-1		+1	µA
High-Side MOSFET On Resistance	R_{DSON_HS}	IN to LX1, LX2 to OUT		20	35	mΩ
Low-Side MOSFET On Resistance	R_{DSON_LS}	LX1 to PGND, LX2 to PGND		20	35	mΩ
Overvoltage Limit Threshold	V_{OVP}		15.6	15.9	16.3	V
Overvoltage Release Threshold	V_{OVP_REL}			15		V
Output Active Discharge Current	I_{DISCHG}	EN = LOW or $V_{IN} < V_{UVLO\_F}$, V_{OUT} = 15V		5		mA

Note 2: Guaranteed by design. Not production tested.

Note 3: Characterized by ATE or Bench test, not production tested.

Electrical Characteristics—I²C Serial Interface

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input HIGH Voltage	V_{IH}		0.7 x V_{VIO}			V
SCL, SDA Input LOW Voltage	V_{IL}				0.3 x V_{VIO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{VIO}		V
SCL, SDA Input Hysteresis in HS Mode	V_{HYS_HS}			0.1 x V_{VIO}		V
SDA Output LOW Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V

Electrical Characteristics—I²C Serial Interface (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL, SDA Input Capacitance	C_I			10		pF
SCL, SDA Input Leakage Current	I_{LK}	T_J = +25°C	-1	0.001	+1	µA
		T_J = +85°C		0.1		
TIMING (STANDARD, FAST, AND FAST-MODE PLUS)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		0.5			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.26			µs
SCL LOW Period	t_{LOW}		0.5			µs
SCL HIGH Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.26			µs
DATA Hold Time	t_{HD_DATA}	Transmit mode		500		ns
DATA Setup Time	t_{SU_DATA}		50			ns
SCL, SDA Receiving Rise Time	t_{R_REV}			120		ns
SCL, SDA Receiving Fall Time	t_{F_REV}			120		ns
SCL, SDA Transmitting Fall Time	t_{F_TRA}			120		ns
Setup Time for STOP Condition	t_{SU_STOP}		0.26			µs
Data Valid Time	t_{VD_DATA}			450		ns
Data Valid Acknowledge Time	t_{VD_ACK}			450		ns
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spikes	t_{SP}			150		ns
TIMING (HIGH-SPEED MODE, BUS CAPACITANCE = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Hold Time (REPEATED) START Condition	t_{HD_START}		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Setup Time REPEATED START Condition	t_{SU_START}		160			ns
DATA Hold Time	t_{HD_DATA}			150		ns

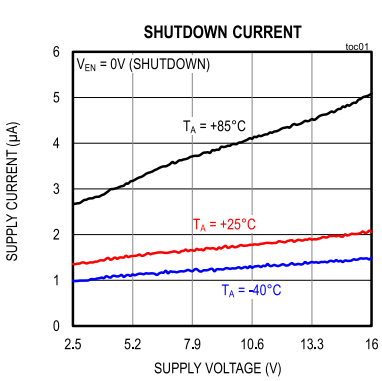
Electrical Characteristics—I²C Serial Interface (continued)

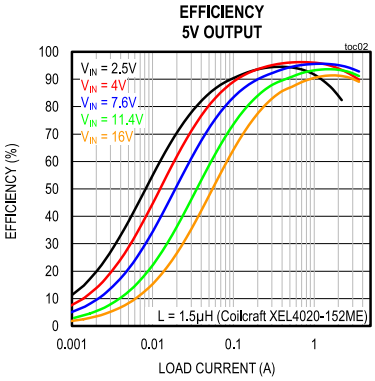
(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

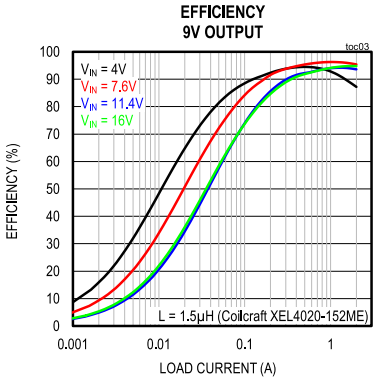
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA Setup Time	t_{SU_DATA}		10			ns
SCL Rise Time	t_{R_SCL}	T_J = +25°C	10		40	ns
SCL Rise Time After REPEATED START Condition and After Acknowledge Bit	t_{R_SCL1}	T_J = +25°C	10		40	ns
SCL Fall Time	t_{F_SCL}	T_J = +25°C	10		40	ns
SDA Rise Time	t_{R_SDA}	T_J = +25°C	10		40	ns
SDA Fall Time	t_{F_SDA}	T_J = +25°C			40	ns
Setup Time for STOP Condition	t_{SU_STOP}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}			40		ns
TIMING (HIGH-SPEED MODE, BUS CAPACITANCE = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Hold Time (REPEATED) START Condition	t_{HD_START}		160			ns
SCL LOW Period	t_{LOW}		320			ns
SCL HIGH Period	t_{HIGH}		120			ns
Setup Time REPEATED START Condition	t_{SU_START}		160			ns
DATA Hold Time	t_{HD_DATA}			150		ns
DATA Setup Time	t_{SU_DATA}		10			ns
SCL Rise Time	t_{R_SCL}	T_J = +25°C	20		80	ns
SCL Rise Time After REPEATED START Condition and After Acknowledge Bit	t_{R_SCL1}	T_J = +25°C	20		80	ns
SCL Fall Time	t_{F_SCL}	T_J = +25°C	20		80	ns
SDA Rise Time	t_{R_SDA}	TJ = +25°C	20		80	ns
SDA Fall Time	t_{F_SDA}	T_J = +25°C			80	ns
Setup Time for STOP Condition	t_{SU_STOP}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}			40		ns

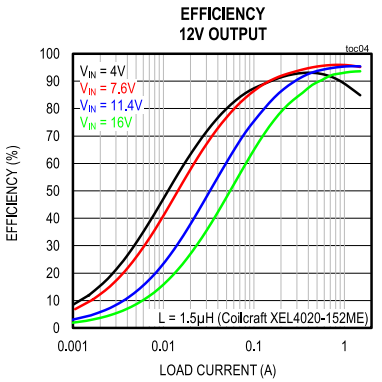
Typical Operating Characteristics

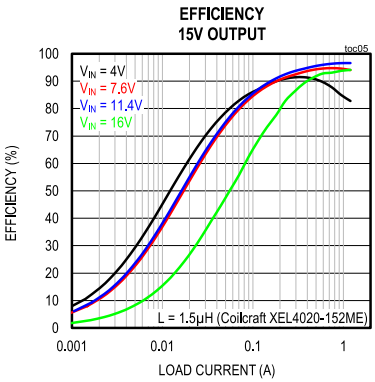
(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted.)

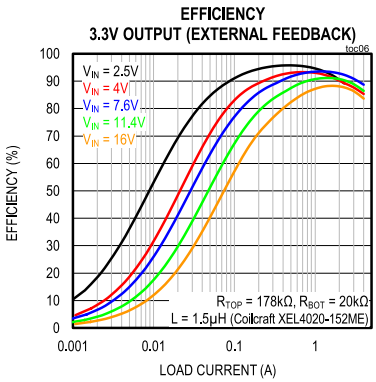


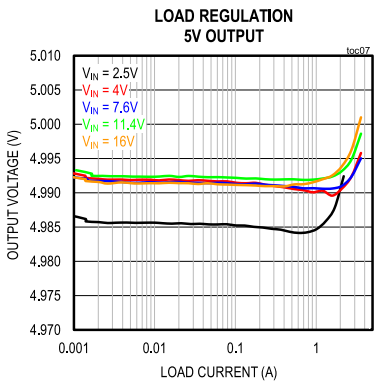


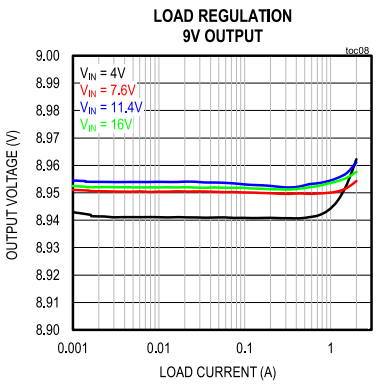








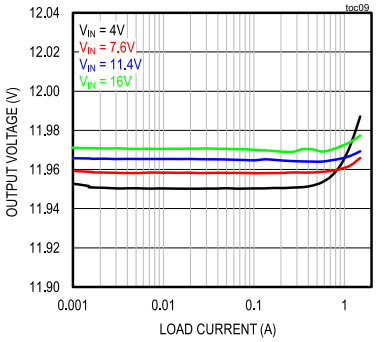




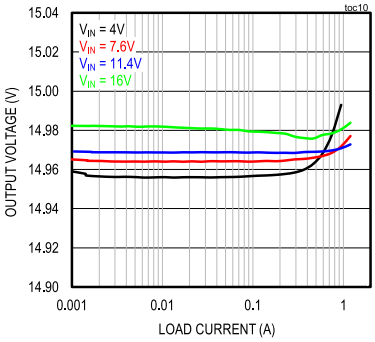
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted.)

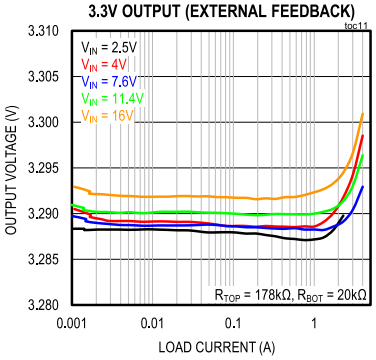
LOAD REGULATION
12V OUTPUT



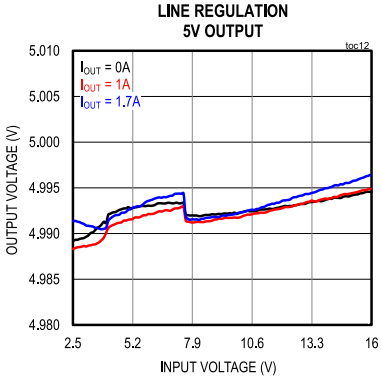
LOAD REGULATION
15V OUTPUT



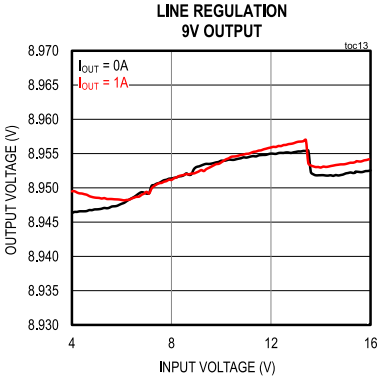
LOAD REGULATION
3.3V OUTPUT (EXTERNAL FEEDBACK)



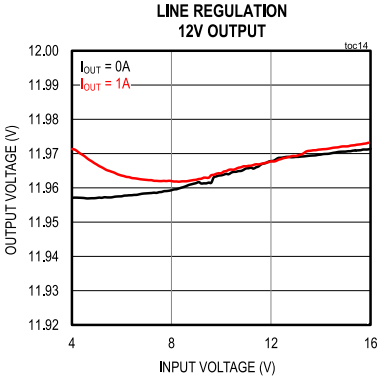
LINE REGULATION
5V OUTPUT



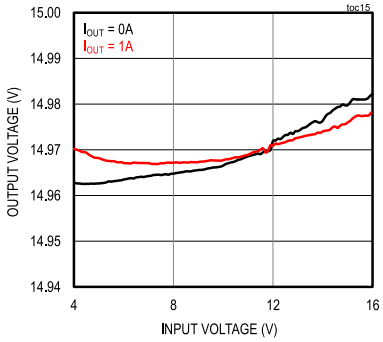
LINE REGULATION
9V OUTPUT



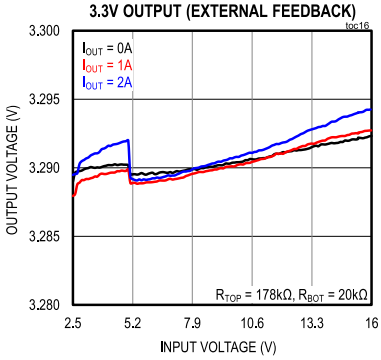
LINE REGULATION
12V OUTPUT



LINE REGULATION
15V OUTPUT



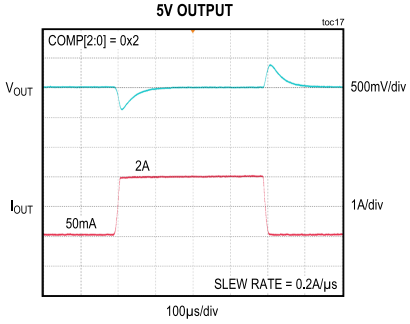
LINE REGULATION
3.3V OUTPUT (EXTERNAL FEEDBACK)



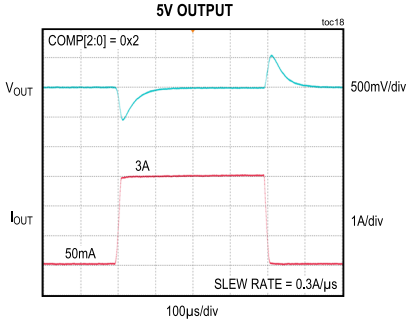
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted.)

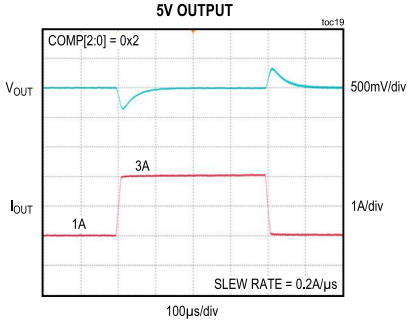
LOAD TRANSIENT RESPONSE
5V OUTPUT



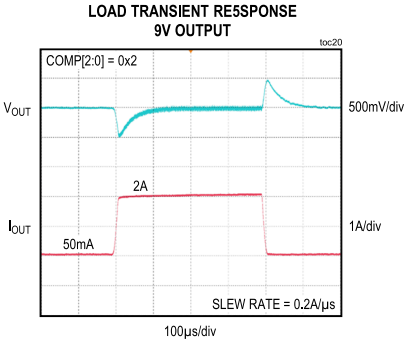
LOAD TRANSIENT RESPONSE
5V OUTPUT



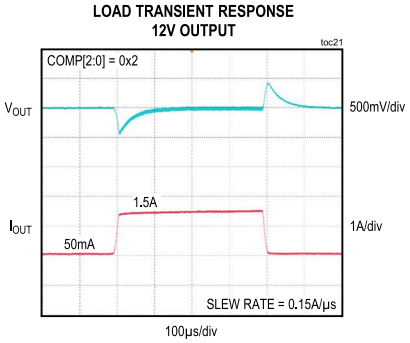
LOAD TRANSIENT RESPONSE
5V OUTPUT



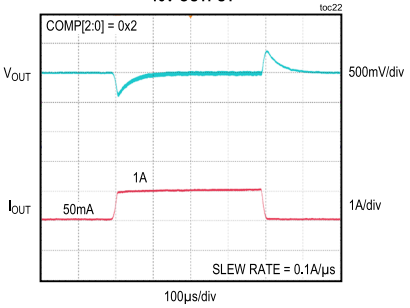
LOAD TRANSIENT RE5SPONSE
9V OUTPUT



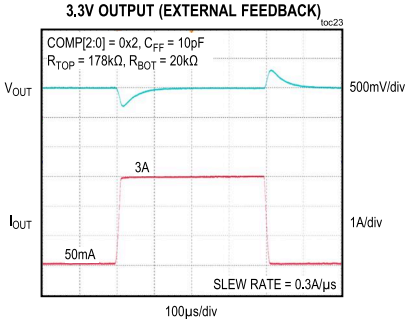
LOAD TRANSIENT RESPONSE
12V OUTPUT



LOAD TRANSIENT RESPONSE
15V OUTPUT



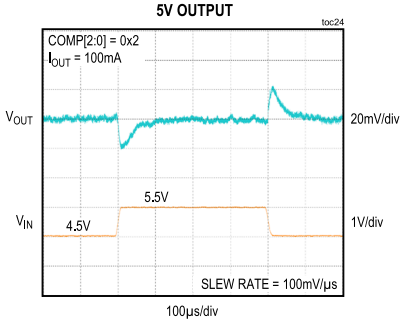
LOAD TRANSIENT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



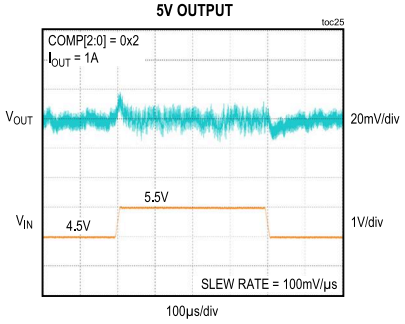
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted.)

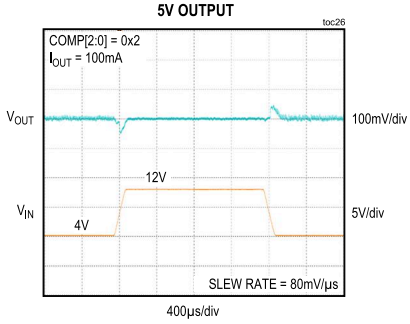
LINE TRANSIENT RESPONSE
5V OUTPUT



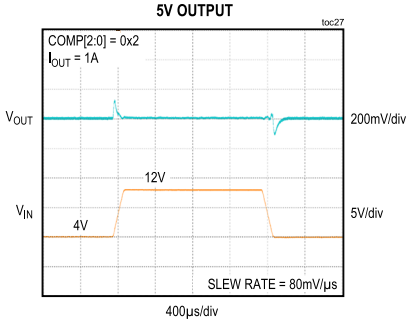
LINE TRANSIENT RESPONSE
5V OUTPUT



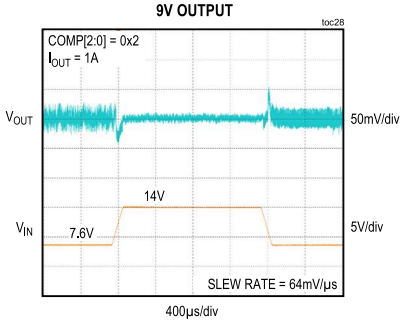
LINE TRANSIENT RESPONSE
5V OUTPUT



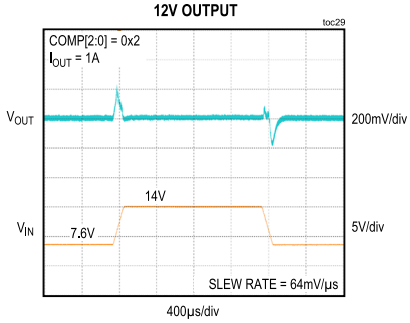
LINE TRANSIENT RESPONSE
5V OUTPUT



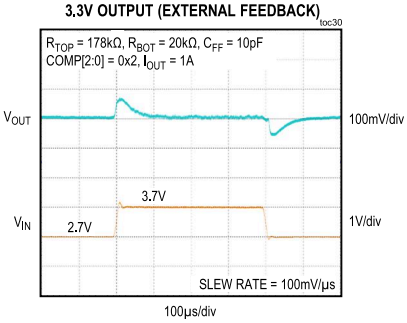
LINE TRANSIENT RESPONSE
9V OUTPUT



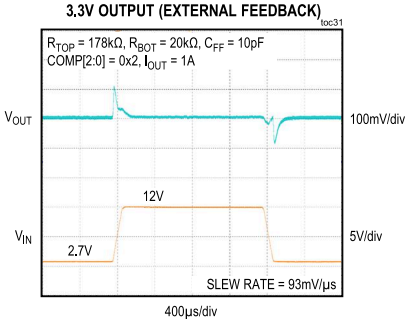
LINE TRANSIENT RESPONSE
12V OUTPUT



LINE TRANSIENT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



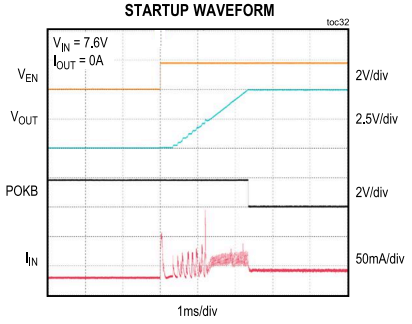
LINE TRANSIENT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



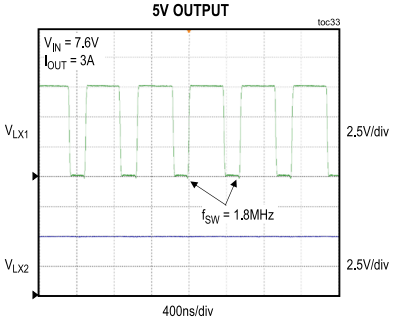
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted.)

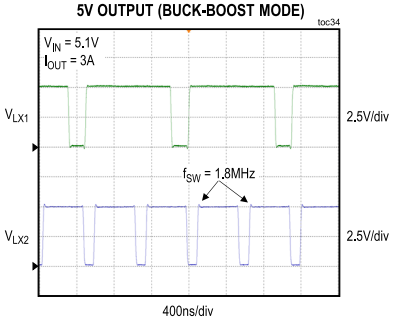
STARTUP WAVEFORM



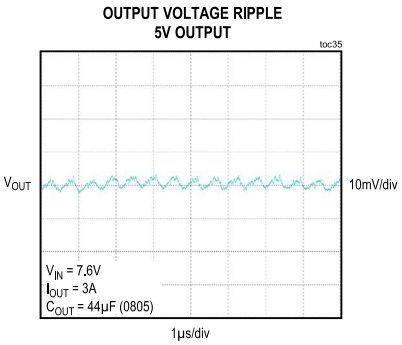
SWITCHING WAVEFORM
5V OUTPUT



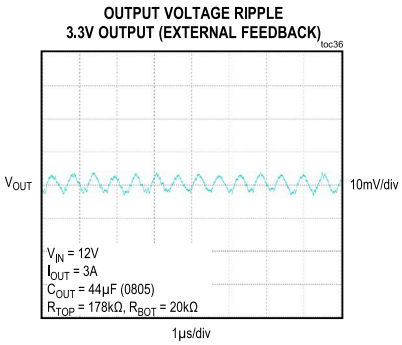
SWITCHING WAVEFORM
5V OUTPUT (BUCK-BOOST MODE)



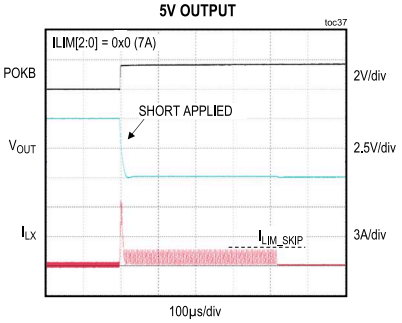
OUTPUT VOLTAGE RIPPLE
5V OUTPUT



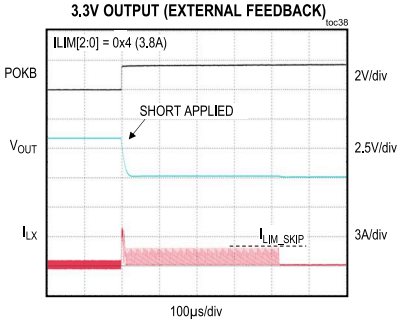
OUTPUT VOLTAGE RIPPLE
3.3V OUTPUT (EXTERNAL FEEDBACK)



SHORT-CIRCUIT RESPONSE
5V OUTPUT



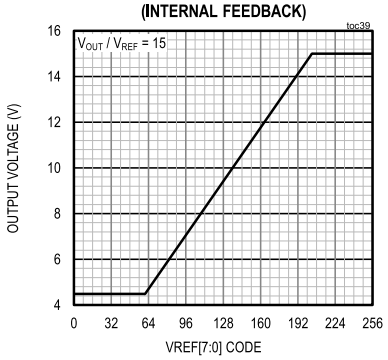
SHORT-CIRCUIT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



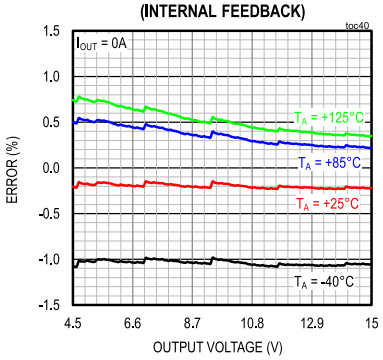
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted.)

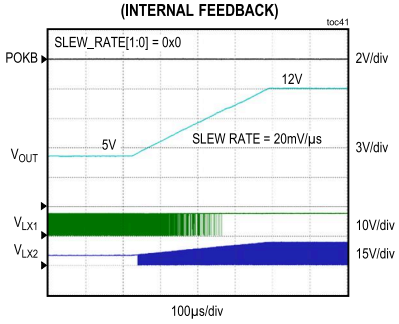
OUTPUT VOLTAGE vs. VREF CODE (INTERNAL FEEDBACK)



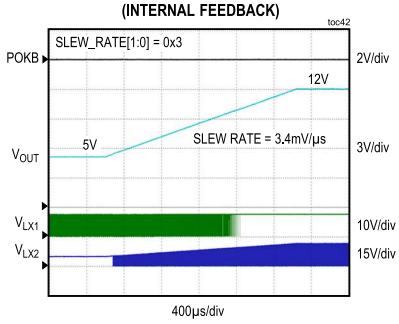
OUTPUT VOLTAGE ACCURACY (INTERNAL FEEDBACK)



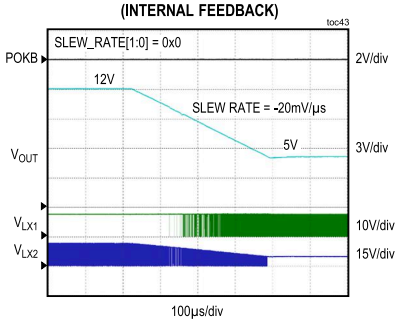
DYNAMIC VOLTAGE SCALING (INTERNAL FEEDBACK)



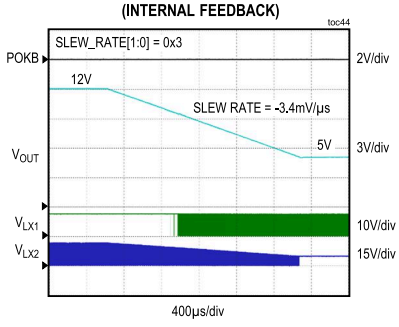
DYNAMIC VOLTAGE SCALING (INTERNAL FEEDBACK)



DYNAMIC VOLTAGE SCALING (INTERNAL FEEDBACK)

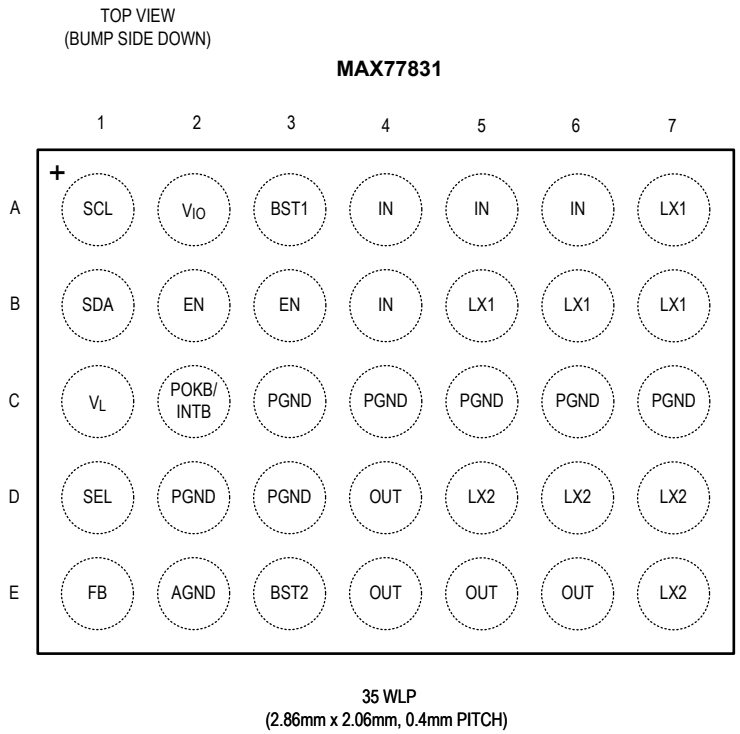


DYNAMIC VOLTAGE SCALING (INTERNAL FEEDBACK)



Pin Configuration

35 WLP



35 WLP
(2.86mm x 2.06mm, 0.4mm PITCH)

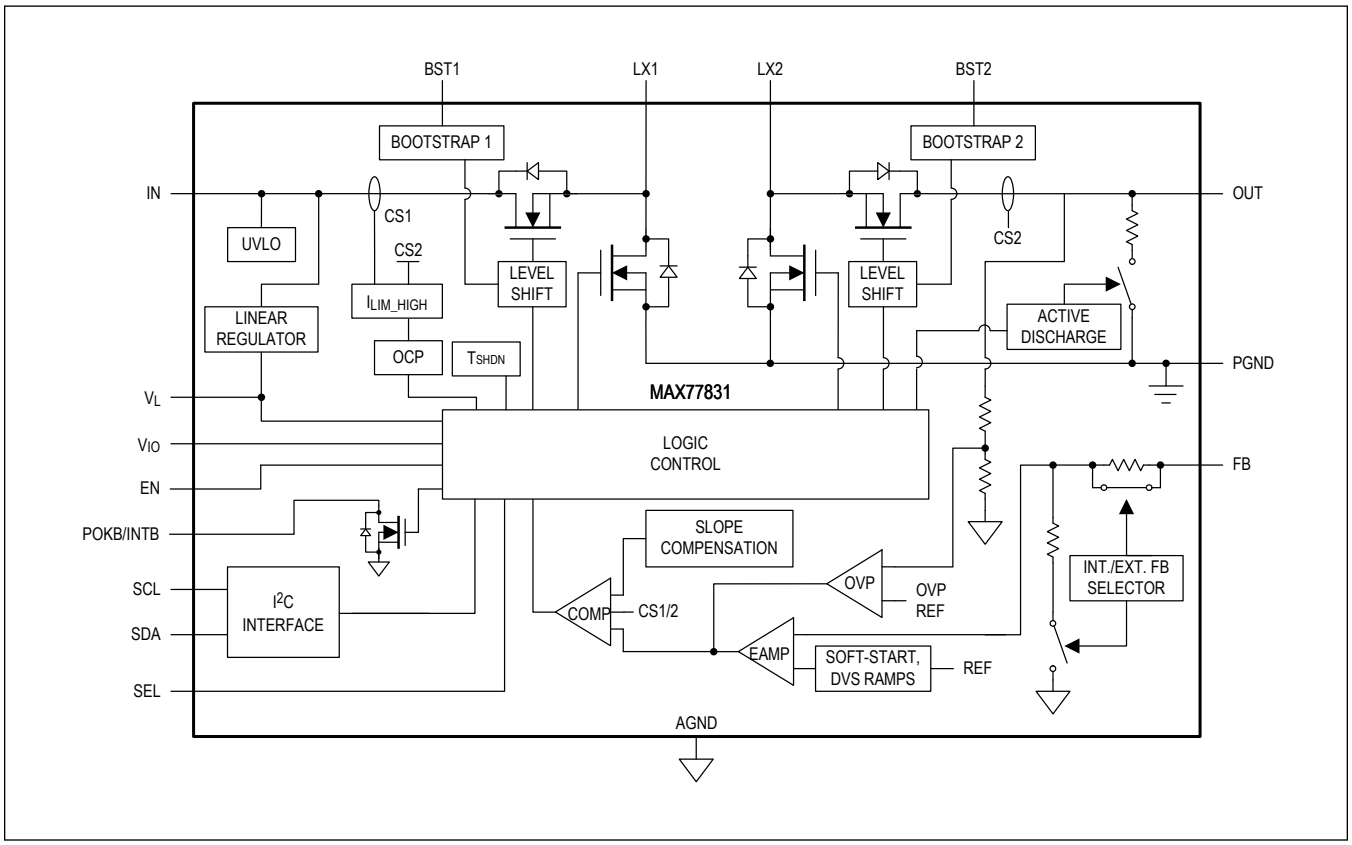
Pin Description

PIN	NAME	FUNCTION	TYPE
A1	SCL	I^2C Serial Interface Clock (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor when using the I^2C interface or connect to AGND when the I^2C interface is not in use.	Digital Input
B1	SDA	I^2C Serial Interface Data (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor when using the I^2C interface or connect to AGND when the I^2C interface is not in use.	Digital I/O
C2	POKB/INTB	Buck-Boost Output Power-OK Monitor or Fault Interrupt Active-Low Open Drain Output. Connect to V_{IO} with a 15kΩ pullup resistor. See the *Power-OK Monitor and Fault Interrupts* section for more details. Do not connect to this pin if not in use.	Digital Output
C1	V_L	Low-Voltage Internal Supply. Powered from IN. Bypass to AGND with a 10V 2.2µF ceramic capacitor. Do not load this pin externally.	Analog
D1	SEL	Configuration Selection. Connect a resistor between SEL and AGND. See Table 2 for resistor value and configurations.	Analog

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
E1	FB	**Using Internal Feedback Resistors**: Output Voltage Sense Input. Connect to the output at the point-of-load (close to output capacitor). **Using External Feedback Resistors**: Output Voltage Feedback Input. Connect to the center tap of an external resistor divider from the output to AGND to set the output voltage. See the *Output Voltage Configuration* section for more details.	Analog
E2	AGND	Analog Ground. Connect to PGND on the PCB. See the *PCB Layout Guideline* section for more details.	Ground
E3	BST2	LX2 High-Side FET Driver Supply. Connect a 50V 0.22µF ceramic capacitor between BST2 and LX2.	Power Input
D4, E4, E5, E6	OUT	Buck-Boost Output. Bypass to PGND with two 25V 22µF ceramic capacitor as close as possible.	Power Output
D5, D6, D7, E7	LX2	Buck-Boost Switching Node 2	Power
C3, C4, C5, C6, C7, D2, D3	PGND	Power Ground. Connect to AGND on the PCB. See the *PCB Layout Guideline* section for more details.	Ground
A7, B5, B6, B7	LX1	Buck-Boost Switching Node 1	Power
A4, A5, A6, B4	IN	Buck-Boost Input. Bypass to PGND with two 25V 10µF ceramic capacitors as close as possible.	Power Input
A3	BST1	LX1 High-Side FET Driver Supply. Connect a 50V 0.22µF ceramic capacitor between BST1 and LX1.	Power Input
B2, B3	EN	Active-High Buck-Boost Enable Input. Compatible with the V_{IO} voltage domain. Pulled down to AGND internally with 800kΩ resistance.	Digital Input
A2	V_{IO}	IO Voltage Supply. Connect to V_{VIO} and bypass to AGND with a 6.3V 0.47µF ceramic capacitor. Registers are held in reset and regulator remains disabled when this pin's voltage is invalid.	Power Input

Functional Diagram



Detailed Description

The MAX77831 is a high-efficiency, high-performance buck-boost converter targeted for systems requiring a wide input voltage range (2.5V to 16V). The IC can supply 18W of continuous output power (for example, up to 2A at 9V (V_{IN} ≥ 4V)). The IC allows systems to change the output voltage and load current capacity dynamically through the I^2C interface. The IC supports the standard 5V/3A USB V_{BUS} requirement as well as 9V/2A, 12V/1.5A, and 15V/1.2A. Systems equipped with the MAX77831 can provide fast-charging peripheral devices with higher output voltage. This minimizes power loss across the cable/connector and reduces charging time.

The IC operates only in forced-PWM mode. The default output voltage is 5V when using internal feedback resistors. The IC can also be configured to any default output voltages between 3V and 15V when using external feedback resistors. The output voltage is adjustable dynamically (DVS) between 4.5V and 15V in 73.5mV steps when using internal feedback resistors, or between 3V to 15V when using external feedback resistors (with step-size dependent on the external feedback resistor ratio), by programming the internal reference voltage through the I^2C interface. See the *Output Voltage Configuration* section for more information.

The SEL pin allows a single external resistor, R_{SEL}, to connect to AGND to program the following:

- I^2C Interface Slave Address (4 options)
- Switching Current Limit Threshold (4 options)
- Feedback Resistor Selection (Internal or external)

The different I^2C interface slave addresses accommodate multiple devices in a system with a limited I^2C bus. The different switching current limit thresholds allow the use of lower profile and smaller external components optimized for a particular application. The use of external feedback resistors allows for wider output voltage range and customizable output voltages at startup. See the *SEL Pin Configuration* section for more information.

An optional I^2C serial interface allows dynamic control of the following:

- Output Voltage (using Internal Reference Voltage)
- Slew Rate of Output Voltage Change (4 options)
- Switching Current Limit Threshold (8 options)
- Switching Frequency (3 options)
- Power-OK (POK) Status and Fault Interrupts
- Internal Compensation

The different switching frequencies provide options to improve the EMI performance by avoiding EMI sensitive frequency bands. The I^2C-programmed settings have priority over the R_{SEL} decoded settings.

Startup

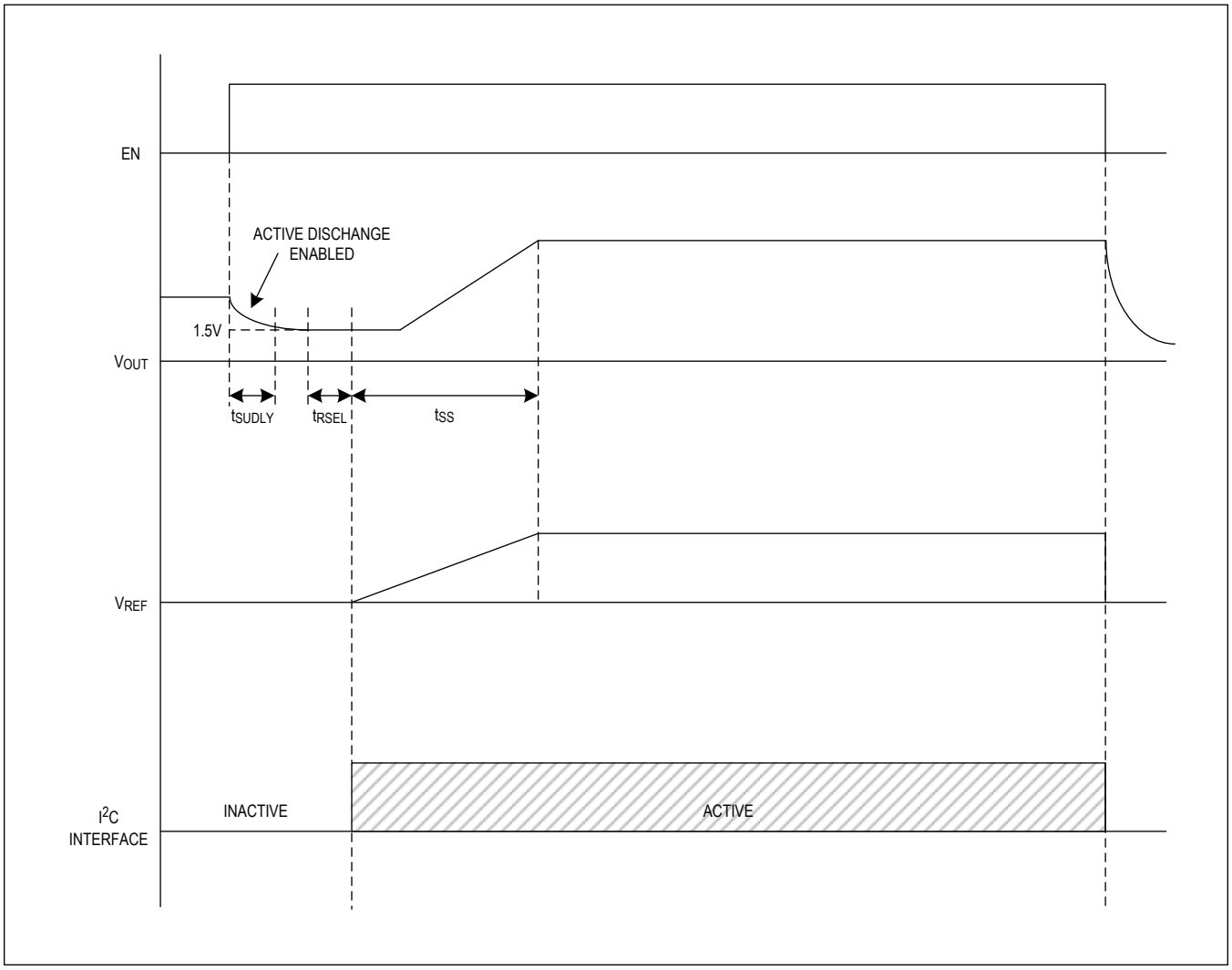


Figure 1. Pre-Biased Startup Waveform

Pull the EN pin to logic HIGH to start up the IC. Ensure that V_{VIO} and V_{IN} are valid. (Note that there is an ESD diode that connects the EN pin to the V_{IO} pin. If the V_{IO} pin is floating, the voltage on the EN pin less a diode-drop voltage appears on the V_{IO} pin.) The IC turns on the internal bias circuitry, which takes typically 100µs (t_{SUDLY}) to settle. During this time, output active discharge is enabled in case of pre-biased startup. After the t_{SUDLY} timer finishes and output is below 1.5V, active discharge is disabled and the IC senses the SEL pin resistance to set the I²C interface slave address, switching current limit threshold, and the use of internal or external feedback resistors. The R_{SEL} reading takes typically 100µs (t_{RSEL}) to complete. See the *SEL Pin Configuration* section for more information. After that, the IC activates the I²C interface and begins the soft-start process. When EN toggles to logic HIGH, if output active discharge is still active from a previous shutdown event, the IC waits for active discharge to finish and then initiates the startup sequence.

Soft-Start

The IC features soft-start to avoid a large amount of input current drawn from the system supply during startup. The default soft-start time (t_{SS}) is 2ms typical. During soft-start time, the internal reference voltage (V_{REF}) slowly ramps up to the target value. When V_{OUT} is below 2V, the switching frequency is lowered to 300kHz, and the current limit threshold is lowered to the skip mode current limit threshold I_{LIM_SKIP} (1.4A typical), which affects the amount of output current supported during startup. After V_{OUT} reaches above 2V, the normal switching frequency and normal current limit threshold apply.

Output hardshort detection is disabled during soft-start and is enabled after the soft-start timer (t_{SS}) expires. See the *Overcurrent Protection (OCP)* section for more information regarding the output hardshort.

Shutdown

Pull the EN pin to logic LOW to shut down the IC. In a shutdown event, the IC stops switching, resets all registers, and activates the output active discharge.

Immediate Shutdown and Latch-Off Conditions

The IC has a latch-off feature to protect itself under certain fault conditions by shutting down the buck-boost regulator.

Immediate Shutdown Conditions:

- IN UVLO: V_{IN} < Input UVLO Falling Threshold (V_{UVLO_F})
- V_{IO} UVLO: V_{VIO} < V_{IO} Valid Falling Threshold ($V_{VIO\_VALID\_F}$)

Latch-Off Conditions:

- Thermal Shutdown: T_J > Thermal Shutdown Rising Threshold (T_{SHDN_R}) (See the *Thermal Shutdown* section)
- HARDSHORT: I_{LIM} Timer > 427µs (See the *Overcurrent Protection* section)

The events in this category are associated with potentially hazardous system states. Under immediate shutdown conditions, the IC shuts down the buck-boost regulator output and the I^2C serial communication bus and resets all registers until the system recovers from these fault conditions. Under latch-off conditions, the IC shuts down the buck-boost regulator output only. It keeps the I^2C serial communication bus active and preserves the state of the registers. To recover from latch-off, the fault condition needs to be removed from the system and power-cycling the EN pin or IN pin is required. Active discharge is engaged when the buck-boost regulator is shut down from all fault conditions except for thermal shutdown. See the *Output Active Discharge* section for more information.

Output Active Discharge

The IC includes an internal switch that provides a path to discharge the energy stored in the output capacitor to PGND. Output active discharge is activated whenever the buck-boost regulator is disabled (by a shutdown event or by any conditions described in the *Immediate Shutdown and Latch-Off Conditions* section, except for thermal shutdown). Output active discharge is also activated before soft-start in the pre-biased startup condition. Before startup, if there is a voltage greater than 1.5V on the OUT pin, output activate discharge is activated until this voltage drops below 1.5V, and then soft-start follows. The amount of discharge current is 5mA typical when V_{OUT} is at 15V, and it decreases as V_{OUT} decreases during the discharge. When the buck-boost regulator is operating, the internal discharging switch is disconnected from the output.

Power-OK Monitor and Fault Interrupts

The IC features power-OK (POK) monitor and fault interrupt functionalities. The status of the POK and the fault interrupts is stored in the INT_SRC register (address 0x10) and can be accessed through the I^2C interface. The IC also features an open-drain POKB/INTB pin digital output (active-low) to reflect the status of the POK or fault interrupts. Connect the POKB/INTB pin with a 15kΩ pullup resistor to the V_{IO} pin. The signal on the POKB/INTB is logical NOR of all POK and fault interrupt bitfields in the INT_SRC register. The connection of each individual POK and fault interrupt bitfield in the INT_SRC register to the POKB/INTB pin can be masked by writing 1 to the corresponding mask bitfield in the INT_MASK register (address 0x11). (For example, when the POK_M bitfield in the INT_MASK register is 1, although the POK bitfield

in the INT_SRC register still updates based on V_{OUT}, the signal on the POKB/INTB pin does not toggle due to POK.) When intending to use the POKB/INTB pin for POK, it is recommended to mask all fault interrupt bits (and unmask the POK bit) by writing 0x0F to the INT_MASK register (default). On the other hand, when intending to use this pin for fault interrupts, it is recommended to mask the POK bit (and unmask all fault interrupt bits) by writing 0x10 to the INT_MASK register. See the Register Map for details.

The POK bit in the INT_SRC register is active-high (so the POKB pin is active-low). The POK status bit is logic LOW when V_{OUT} falls below 85% (typ) of the target voltage. The POK status bit is logic HIGH when V_{OUT} rises above 95% (typical) of the target voltage. The POK status bit is constantly updated based on the V_{OUT} level while the buck-boost regulator is enabled. During a soft-start or V_{OUT} DVS event, V_{OUT} sensing for the POK is disabled, and the POK status bit holds its previous value prior to the soft-start or V_{OUT} DVS event.

The fault interrupt bits in the INT_SRC register are active-high (so the INTB pin is active-low). Any of the following conditions triggers the fault interrupt by setting the corresponding fault interrupt bit to 1 in the INT_SRC register. The interrupts can only be reset by power cycling the IN pin or EN pin.

- OVP: The IC activates overvoltage protection. (See the *Overvoltage Protection* section.)
- HARDSHORT: The IC is latched off by output hardshort. (See the *Overcurrent Protection* section.)
- THS: The IC is latched off by thermal shutdown. (See the *Thermal Shutdown* section.)
- OCP: The IC is latched off by overcurrent protection. (See the *Overcurrent Protection* section.)

Buck-Boost Regulator

The MAX77831 buck-boost regulator utilizes a four-switch H-bridge configuration and contains buck, boost, or 3-phase buck-boost operating modes. This topology maintains output voltage regulation over the input voltage range. The buck-boost regulator provides 3V to 15V of output voltage range. High switching frequency and a unique control algorithm allow for the smallest solution size, low output noise, and the highest efficiency across a wide input voltage and output current range.

Buck-Boost Control Scheme

The buck-boost regulator operates using a fixed-frequency pulse-width modulated (PWM) control scheme with current-mode compensation. The buck-boost utilizes an H-bridge topology using a single inductor.

The default switching frequency is 1.8MHz. The bitfield FREQ[1:0] sets the switching frequency. The different switching frequencies provide options to avoid EMI sensitive frequency bands and improve EMI performance.

The H-bridge topology has three switching phases, as shown in Figure 2:

- Φ1 switch phase (HS1 = ON, LS2 = ON) stores energy in the inductor and ramps up the inductor current at a rate proportional to the input voltage divided by inductance: V_{IN}/L.
- Φ2 switch phase (HS1 = ON, HS2 = ON) ramps the inductor current up (in buck mode) or down (in boost mode) at a rate proportional to the differential voltage across the inductor: $(V_{IN} - V_{OUT})/L$
- Φ3 switch phase (LS1 = ON, HS2 = ON) ramps down the inductor current at a rate proportional to the output voltage divided by the inductance: $-V_{OUT}/L$.

Boost operation ($V_{IN} < V_{OUT}$) utilizes Φ1 and Φ2 within a single clock period. See the representation of the inductor current waveform for boost mode operation in Figure 2.

Buck operation ($V_{IN} > V_{OUT}$) utilizes Φ2 and Φ3 within a single clock period. See the representation of the inductor current waveform for buck mode operation in Figure 2.

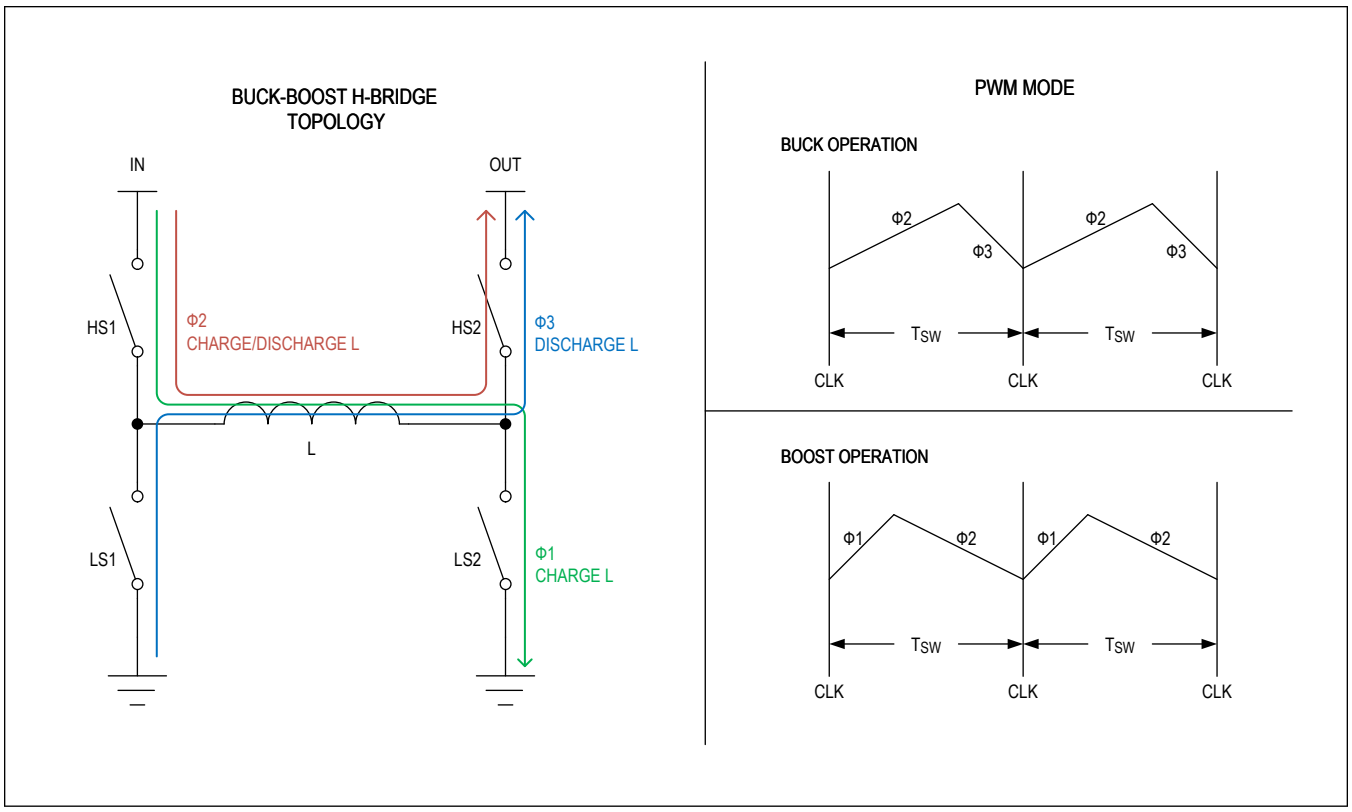


Figure 2. Buck-Boost H-Bridge Topology

Output Voltage Configuration

The IC supports a wide output voltage range between 4.5V and 15V when using internal feedback resistors, and between 3.0V and 15V when using external feedback resistors. The use of internal feedback resistors provides the benefits of less external components and less overall solution size, while the use of external feedback resistors allows for wider output voltage range and customizable output voltage V_{OUT} at startup without using the I^2C interface. The selection between using internal or external feedback resistors is configurable by R_{SEL}. See the *SEL Pin Configuration* section for more information.

When using internal feedback resistors, the output voltage range is between 4.5V and 15V in 73.5mV steps. The default V_{OUT} is 5V (V_{REF} = 0.333V). Use the appropriate R_{SEL} value to configure the IC for using internal feedback resistors, and connect the FB pin directly to the OUT pin at the local output capacitor.

When using external feedback resistors, the output voltage range is between 3.0V and 15V. Actual output voltage range and step size depend on the external feedback resistor ratio. Use the appropriate R_{SEL} value to configure the IC for using external feedback resistors, and connect a resistor divider between V_{OUT}, FB, and AGND as shown in Figure 3. It is also recommended to add a 10pF feedforward capacitor (C_{FF}) in parallel with the top feedback resistor (R_{TOP}). Choose R_{TOP} (from OUT to FB) to be between 150kΩ and 330kΩ. Resistors with 1% tolerance (or better) are highly recommended to keep the accuracy of V_{OUT}. Calculate the value of R_{BOT} (from FB to AGND) for a desired V_{OUT} at startup with the following equation:

$$R_{BOT} = \frac{R_{TOP} \times V_{REF}}{(V_{OUT} - V_{REF})},\ V_{OUT} \le V_{OVP}$$

where V_{REF} is the default internal reference voltage.

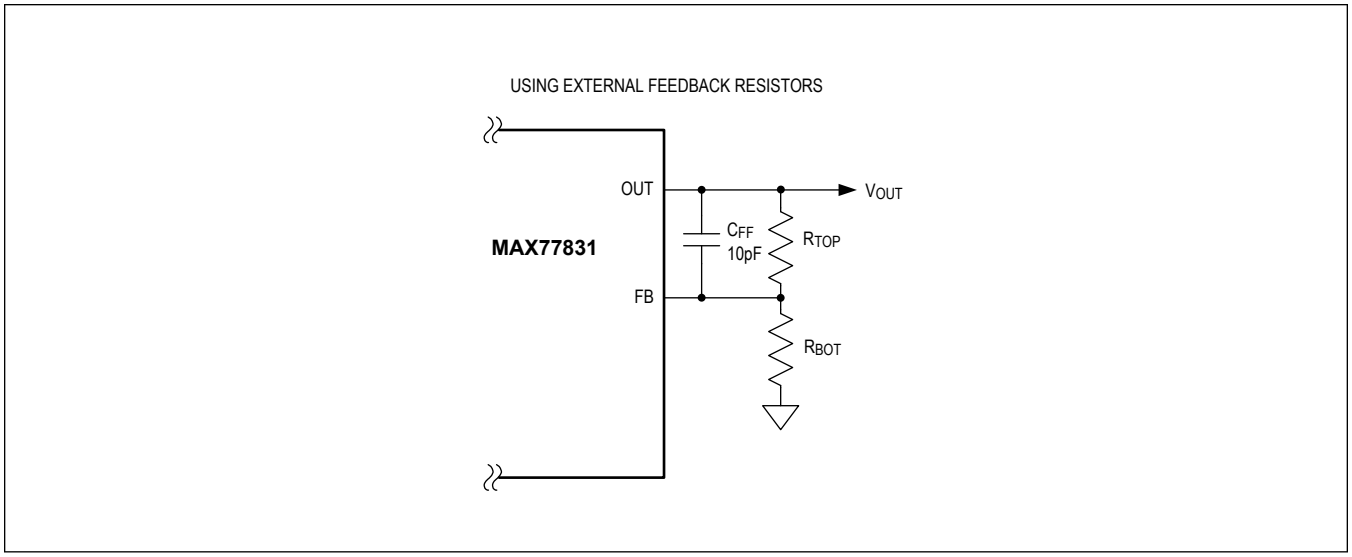


Figure 3. Connecting External Feedback Resistors to the MAX77831

With default V_{REF} of 0.333V, Table 1 lists the recommended external feedback resistors values (in E192 series) for common startup output voltages.

Table 1. External Feedback Resistor Value Recommendations

DEFAULT V_{REF} (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	STARTUP V_{OUT} (V)	PROGRAMMABLE V_{OUT} RANGE (V)	V_{OUT} STEP SIZE (mV)
0.333	160	20	3	3.0 to 9.0	44.1
	178	20	3.3	3.0 to 9.9	48.5
	312	12	9	8.1 to 15	132.3
	232	6.65	12	10.7 to 15	175.8
	234	5.3	15	13.5 to 15	221.2

V_{OUT} is dynamically adjustable by programming V_{REF} through the I^2C interface. The bitfield VREF[7:0] sets the V_{REF}. V_{REF} ranges between 0.299V and 1V in 4.9mV steps.

When using internal feedback resistors, V_{OUT} ranges between 4.5V and 15V in 73.5mV steps, and it can be calculated with the following equation:

$$V_{OUT} = V_{REF} \times 15$$

When using external feedback resistors, the V_{OUT} range and step size vary based on the external feedback resistor values. The V_{OUT} step size can be calculated with the following equation:

$$V_{OUT\_STEP} = (\frac{4.9mV}{R_{BOT}}) \times (R_{BOT} + R_{TOP})$$

To calculate the V_{OUT} range, use the following equation and plug in the minimum V_{REF} of 0.299V and maximum V_{REF} of 1V :

$$V_{OUT} = (\frac{V_{REF}}{R_{BOT}}) \times (R_{BOT} + R_{TOP}),\ V_{OUT} \le V_{OVP}$$

Note that V_{OUT} cannot exceed the output voltage range, or it triggers overvoltage protection (OVP). See the *Overvoltage Protection* section for more information.

The bitfield SLEW_RATE[1:0] sets the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$), with default value of 4/3mV/µs. The actual V_{OUT} DVS ramp rate ($\Delta V_{OUT}/\Delta t$) can be calculated from the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$) using the above equations

for external feedback resistors. For example, if using internal feedback resistors, the default $\Delta V_{REF}/\Delta t$ of 4/3mV/µs corresponds to the $\Delta V_{OUT}/\Delta t$ of 20mV/µs.

SEL Pin Configuration

The SEL pin allows a single resistor (R_{SEL}) to connect the SEL pin to AGND to configure the high-side switching current limit threshold (I_{LIM}), the I^2C interface slave address, and the use of internal or external feedback resistors. Resistors with 1% tolerance (or better) should be used for R_{SEL}. Table 2 lists nominal R_{SEL} values with the corresponding settings.

Table 2. MAX77831 R_{SEL} Selection Table

R_{SEL}(Ω)	FEEDBACK RESISTOR SELECTION	TYPICAL I_{LIM} (A)	I^2C SLAVE ADDRESS (7-BIT)	R_{SEL}(Ω)	FEEDBACK RESISTOR SELECTION	TYPICAL I_{LIM} (A)	I^2C SLAVE ADDRESS (7-BIT)
SHORT TO GND	Internal	7.0	110 0110 (0x66)	3740	External	7.0	110 0110 (0x66)
200			110 0111 (0x67)	8060			110 0111 (0x67)
309			110 1110 (0x6E)	12400			110 1110 (0x6E)
422			110 1111 (0x6F)	16900			110 1111 (0x6F)
536		5.6	110 0110 (0x66)	21500		5.6	110 0110 (0x66)
649			110 0111 (0x67)	26100			110 0111 (0x67)
768			110 1110 (0x6E)	30900			110 1110 (0x6E)
909			110 1111 (0x6F)	36500			110 1111 (0x6F)
1050		3.8	110 0110 (0x66)	42200		3.8	110 0110 (0x66)
1210			110 0111 (0x67)	48700			110 0111 (0x67)
1400			110 1110 (0x6E)	56200			110 1110 (0x6E)
1620			1101111 (0x6F)	64900			110 1111 (0x6F)
1870		1.72	110 0110 (0x66)	75000		1.72	110 0110 (0x66)
2150			110 0111 (0x67)	86600			110 0111 (0x67)
2490			110 1110 (0x6E)	100000			110 1110 (0x6E)
2870			110 1111 (0x6F)	OPEN			110 1111 (0x6F)

Internal Compensation Options

The IC is designed to work without the I^2C serial interface. For designs looking to optimize its performance, the COMP[2:0] bitfield for internal compensation adjustment is available only through the I^2C serial interface. For those systems that do not utilize the I^2C serial interface, the IC can still optimize the stability by adjusting the output capacitance. In general, performance can be further optimized by lowering the COMP[2:0] bitfield value through the I^2C interface or by adding additional output capacitance.

Protection Features

Undervoltage Lockout (UVLO)

The IC's undervoltage lockout feature prevents operation in abnormal input conditions when input voltage V_{IN} falls below the IN UVLO falling threshold (V_{UVLO_F}) or when the V_{IO} voltage (V_{VIO}) falls below the V_{IO} valid falling threshold ($V_{VIO\_VALID\_F}$). Regardless of the EN pin status, the IC becomes disabled and all registers reset until V_{IN} rises above the UVLO rising threshold (V_{UVLO_R}) and V_{IO} rises above the V_{IO} valid rising threshold ($V_{VIO\_VALID\_R}$). Note that there is an ESD diode that connects the EN pin to the V_{IO} pin. If the V_{IO} pin is floating and a voltage is applied to the EN pin, although no voltage is directly applied to V_{IO} because of the ESD diode is conducting, the voltage on the EN pin less a diode-drop voltage appears on the V_{IO} pin, potentially enabling the IC.

Overvoltage Protection (OVP)

The IC's overvoltage protection feature ensures that the output voltage V_{OUT} never exceeds the overvoltage limit threshold (V_{OVP} (15.9V typ)). In this fault condition, V_{OUT} rises up to V_{OVP}. The IC detects the overvoltage, sets the OVP[0] interrupt bit in the INT_SRC register (address 0x10), and activates the overvoltage protection by disabling the high-side MOSFETs and enabling the low-side MOSFETs until V_{OUT} drops below the overvoltage release threshold (V_{OVP_REL}). As a result, V_{OUT} regulates between V_{OVP} and V_{OVP_REL}.

Overcurrent Protection (OCP)

The IC features a robust switching current limit scheme that protects the IC and the inductor during overload and fast transient conditions. The current sensing circuit takes current information from the high-side MOSFETs to determine the peak switching current ($R_{DS(ON)}$ x I_L).

The IC provides eight different cycle-by-cycle current limit thresholds (I_{LIM}) for the high-side MOSFET to support different output current levels. The bitfield ILIM[2:0] or R_{SEL} resistor value sets the I_{LIM}. Note that while all eight options are programmable through the I^2C, only four options are selectable through R_{SEL}. When the I_{LIM} values from the I^2C interface and from R_{SEL} differ, the I^2C interface setting has priority over R_{SEL}.

When the inductor current (I_L) reaches the current limit level (I_{LIM}), the IC enters the OCP state. The inductor charging phase terminates, and the discharging phase begins during the rest of the switching cycle. If the V_{OUT} drops below 60% of target, then the IC enters the output HARD SHORT state by reducing the switching frequency to 300kHz. If V_{OUT} drops below 2V due to the HARD SHORT state, the switching current limit threshold is reduced to the skip mode switching current limit threshold, I_{LIM_SKIP} (1.4A typical). The IC also includes a 427µs I_{LIM} timer to latch off the buck-boost regulator. This timer is activated in the HARD SHORT state. When this timer expires after 427µs (i.e., when I_L has reached I_{LIM} continuously for 427µs), the IC latches off the buck-boost regulator and HARDSHORT[0] interrupt bit is set. Figure 4 depicts the behavior during the OCP and HARD SHORT states. See the *Immediate Shutdown and Latch-Off Conditions* section for information about latch-off. If prior to latch-off, the overcurrent event disappears and I_L no longer reaches the I_{LIM} threshold, the IC resets the timer.

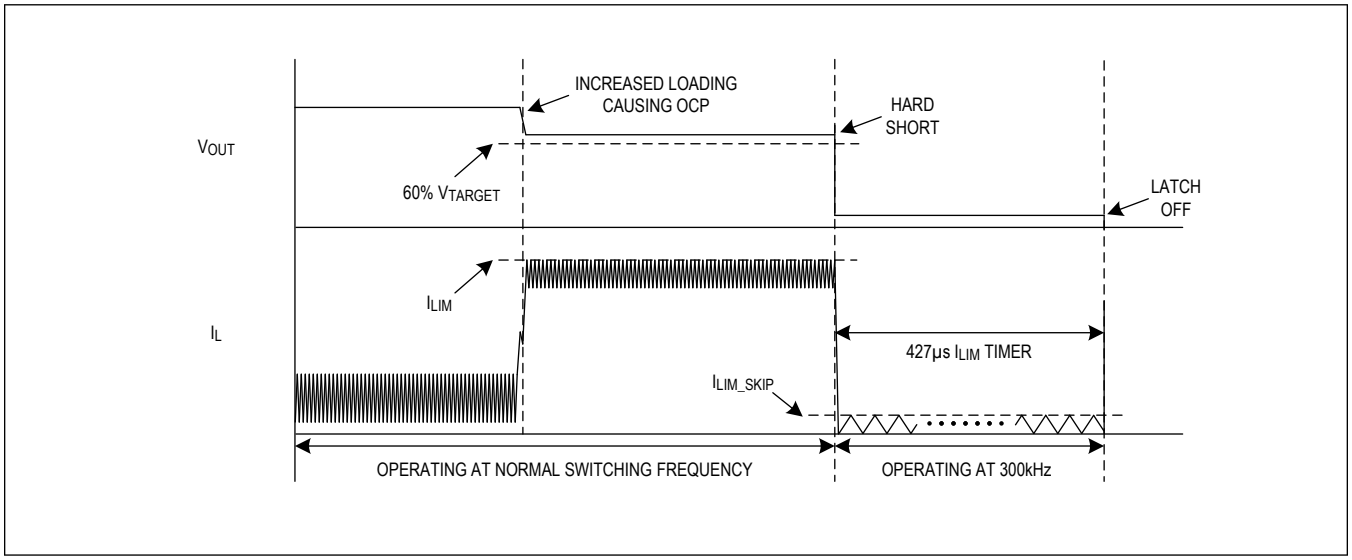


Figure 4. Overcurrent and Output Hard-Short Behavior

Thermal Shutdown (THS)

The IC contains an internal thermal protection circuit that monitors the die temperature. The IC enters thermal shutdown (THS) when the junction temperature (T_J) exceeds the thermal shutdown rising threshold (T_{SHDN_R} (150ºC typical)). In THS, the IC is latched off and sets the THS[0] interrupt bit in the INT_SRC register (address 0x10). Unlike other latch-off events, the output active discharge is not activated. Power cycling the EN pin or IN pin is required to recover from thermal

shutdown. See the *Immediate Shutdown and Latch-Off Conditions* section for more information. If power cycling while T_J is above T_{SHDN_R}, the IC waits until T_J drops below the thermal shutdown falling threshold (T_{SHDN_F} (135ºC typical)) before recovering and starting up again (Figure 5). If power cycling while junction temperature T_J is below T_{SHDN_R}, the IC recovers and starts up immediately.

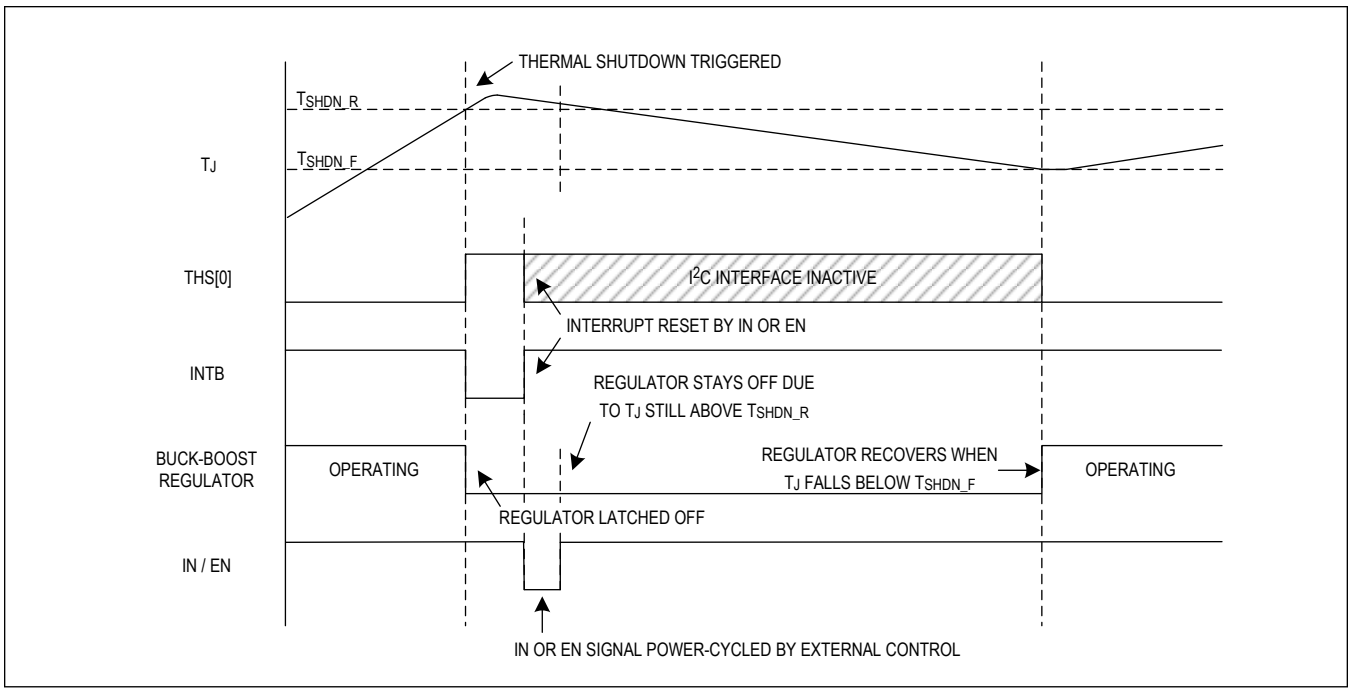


Figure 5. Thermal Shutdown Recovery, Power Cycling IN or EN While $T_J > T_{SHDN\_R}$

Detailed Description—I²C Serial Interface

General Description

The I²C-compatible 2-wire serial interface is used for setting output voltages and other functions. See the *Register Map* for available settings.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with the SDA and SCL help protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multi-master bus. The maximum number of devices that can be attached to the bus is only limited by bus capacitance.

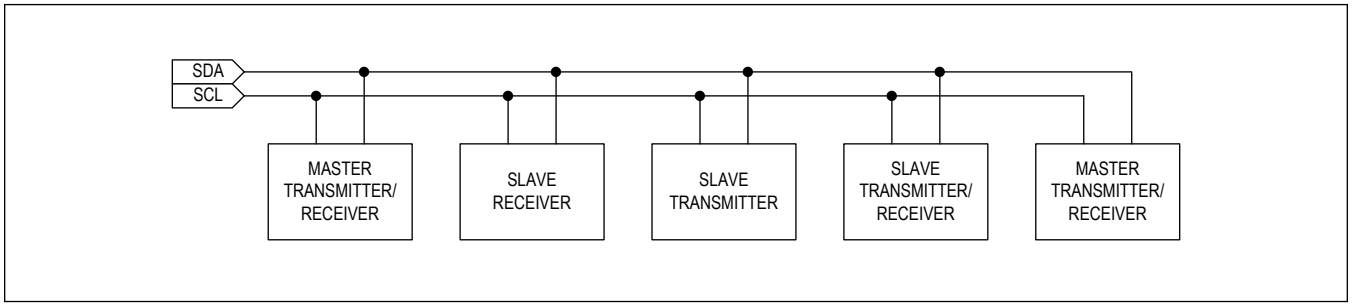


Figure 6. Functional Logic Diagram for the Communications Controller

Figure 6 shows an example of a typical the I²C bus system. A device on I²C bus that sends data to the bus is called a “transmitter.” A device that receives data from the bus is called a "receiver.” A device that initiates a data transfer and generates SCL clock signals to control the data transfer is called a “master.” Any device being addressed by the master is called a “Slave”. The MAX77831 is a slave on the I²C bus, and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on the SDA must remain stable during the HIGH portion of the SCL clock pulse. Changes in the SDA while the SCL is HIGH are control signals (START and STOP conditions).

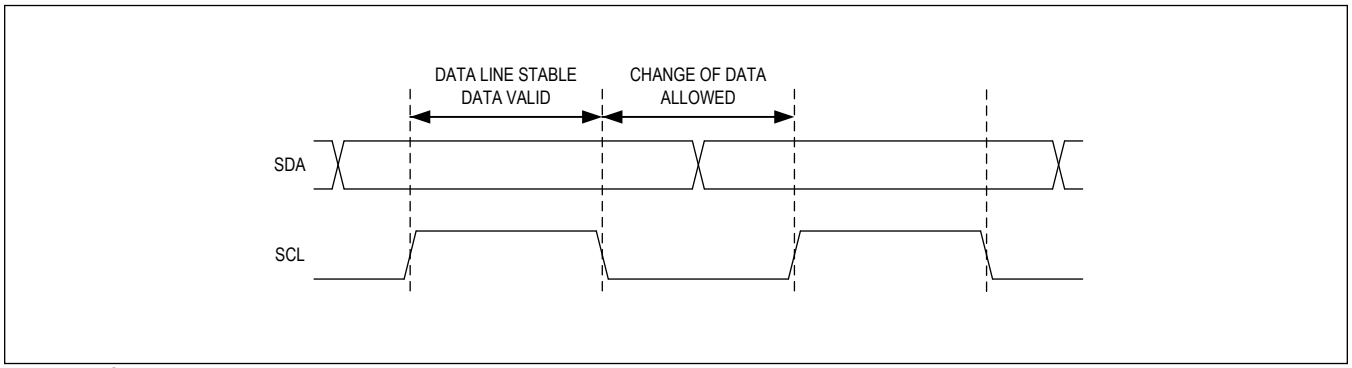


Figure 7. I²C Bit Transfer

START and STOP Conditions

When the I2C serial interface is inactive, the SDA and SCL idle HIGH. A master device initiates communication by issuing a START condition (S). A START condition (S) is a HIGH-to-LOW transition on the SDA while the SCL is HIGH. A STOP condition (P) is a LOW-to-HIGH transition on the SDA while the SCL is HIGH.

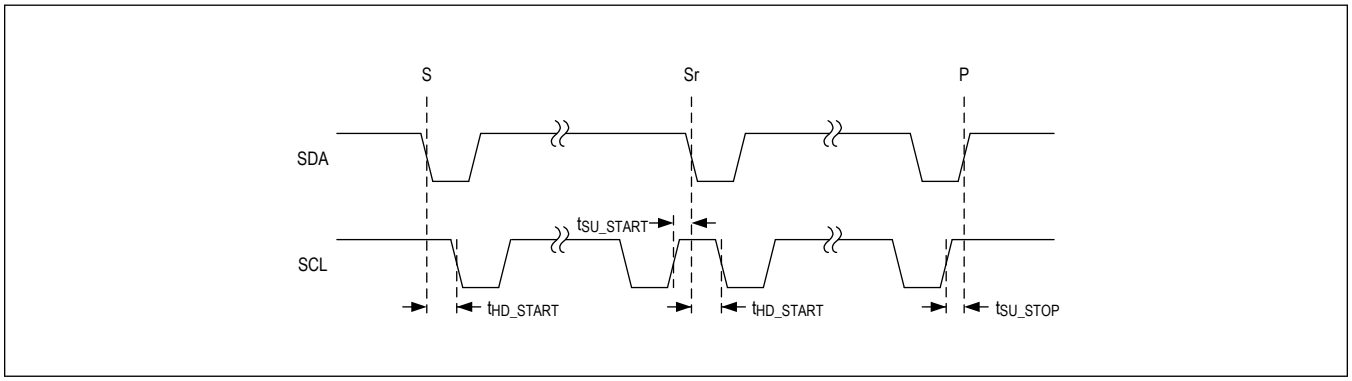


Figure 8. START and STOP Conditions

A START condition (S) from the master device signals the beginning of a transmission. The master terminates transmission by issuing a NOT-ACKNOWLEDGE (nA) followed by a STOP condition (P).

A STOP condition (P) frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP condition (P) in order to maintain control of the bus. In general, a REPEATED START (Sr) command is functionally equivalent to a regular START condition (S).

When a STOP condition (P) or incorrect address is detected, the MAX77831 internally disconnects the SCL from the I2C serial interface until the next START condition (S), minimizing digital noise and feed-through.

Acknowledge Bit

Both I2C bus master device and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it LOW during the HIGH portion of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows the SDA to be pulled HIGH before the rising edge of the acknowledge-related clock pulse and leaves it HIGH during the HIGH portion of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

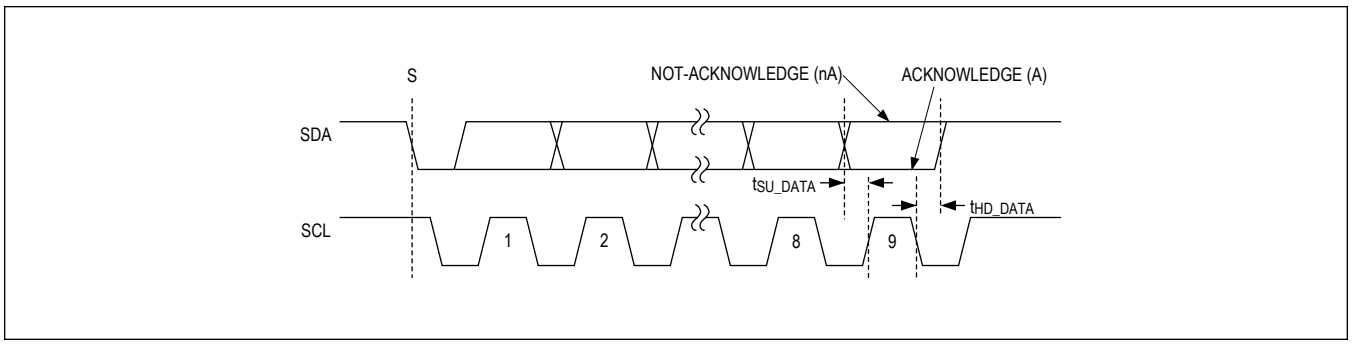


Figure 9. Acknowledge Bit

Slave Address

Table 3 shows the available I²C slave addresses of the MAX77831. The MAX77831 supports up to four different slave addresses through R_{SEL} programming for when multiple devices in the same I²C bus line need to be used or when there is a conflict between the slave addresses in the system. See Table 2 for available R_{SEL} values and the corresponding I²C slave addresses.

Table 3. I²C Slave Addresses

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
110 0110 (0x66)	1100 1100 (0xCC)	1100 1101 (0xCD)
110 0111 (0x67)	1100 1110 (0xCE)	1100 1111 (0xCF)
110 1110 (0x6E)	1101 1100 (0xDC)	1101 1101 (0xDD)
110 1111 (0x6F)	1101 1110 (0xDE)	1101 1111 (0xDF)

Figure 10 shows the 7-bit slave address at 0x66.

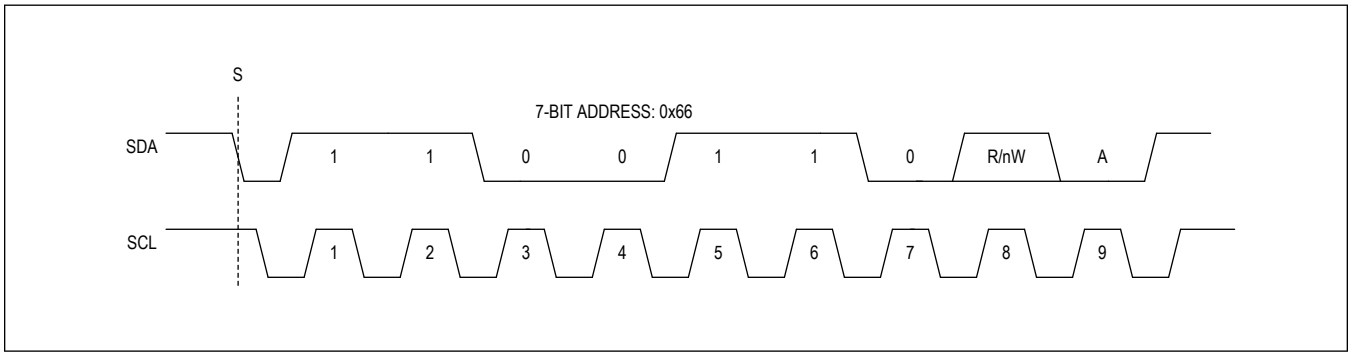


Figure 10. Slave Address Byte Example

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77831 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77831 does not implement the I²C specification "General Call Address." The MAX77831 does not issue an ACKNOWLEDGE (A) if it detects the "General Call Address" (0000 0000).

Communication Speed

The MAX77831 supports the following communication speeds outlined in the I2C revision 3.0 specification:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speed, the pullup resistance must be decreased to maintain a reasonable time constant. See the “Pull-up Resistor Sizing” section of the I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for a bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, see the I2C revision 3.0 specification. The major considerations with respect to the MAX77831 are as follows:

- Master device shall use current source pullups to shorten the signal rise times.
- Slave device must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition (P), the MAX77831 inputs filters that are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the protocol described in the *Engage in High-Speed Mode* section.

Communication Protocols

The MAX77831 supports both writing to and reading from its registers.

Writing to a Single Register

Figure 11 shows the protocol for writing to a single register. This protocol is the same as the “Write Byte” protocol in the SMBus specification.

The “Write Byte” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

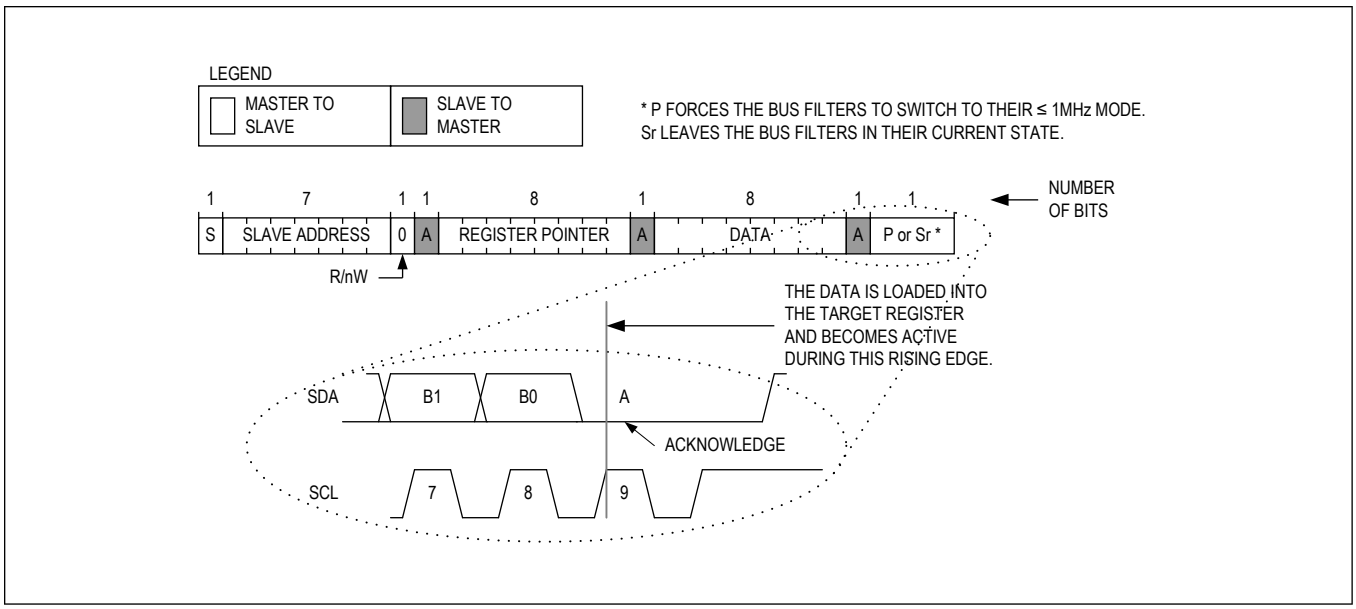


Figure 11. Writing to a Single Register

Writing to Sequential Registers

Figure 12 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the master device continues to write after the slave device receives the first byte of data. When the master is done writing data, it issues a STOP condition (P) or REPEATED START condition (Sr).

The “Writing to Sequential Registers” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register and the data becomes active.
8. Step 6 to step 7 are repeated as many times as the master requires.
9. During the last acknowledge-related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

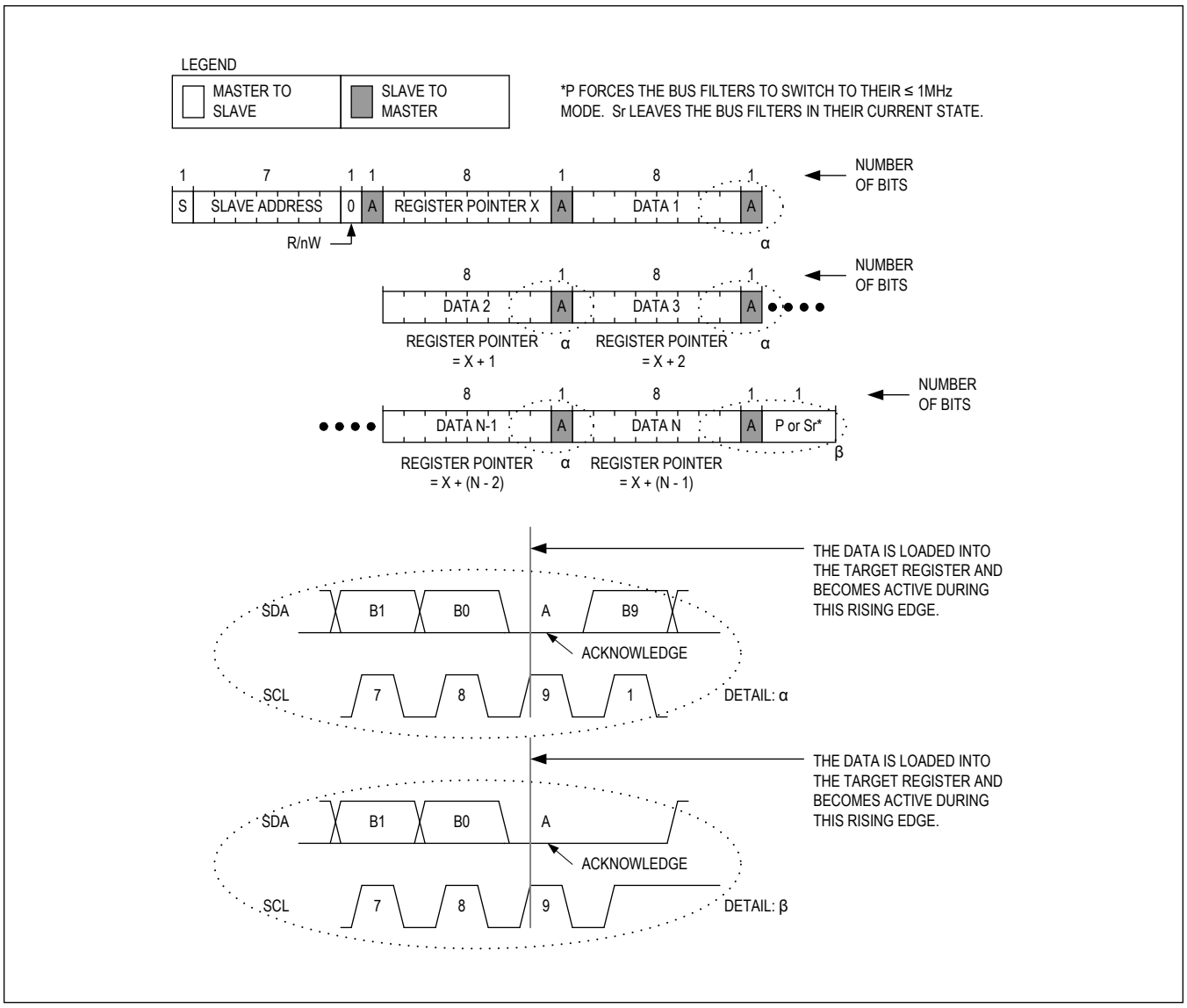


Figure 12. Writing to Sequential Registers

Reading from a Single Register

Figure 13 shows the protocol for reading from a single register. This protocol is the same as the “Read Byte” protocol in the SMBus specification.

The “Read Byte” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
9. The addressed slave places 8 bits of data from the location specified by the register pointer on the bus.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

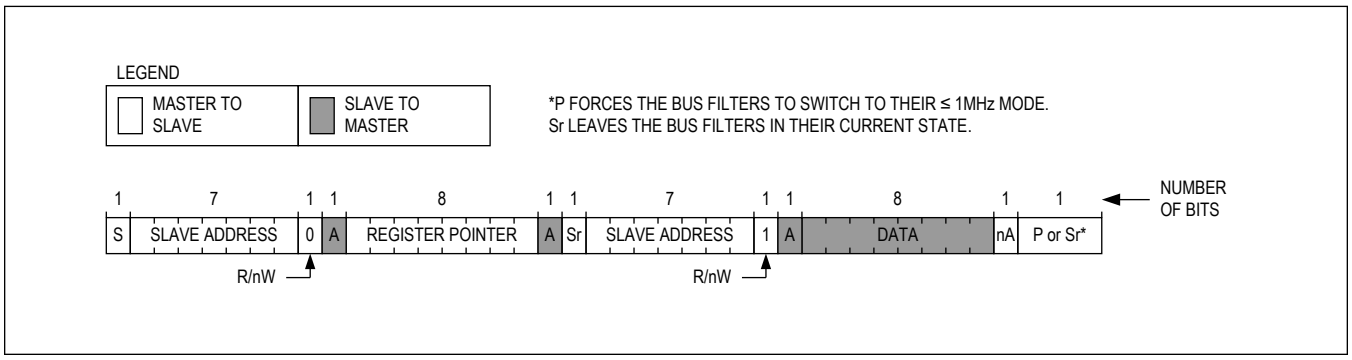


Figure 13. Reading from a Single Register

Reading from Sequential Registers

Figure 14 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol, except the master device issues an ACKNOWLEDGE (A) to signal the slave device that it wants more data. When the master device has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP condition (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
9. The addressed slave places 8 bits of data from the location specified by the register pointer on the bus.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Step 9 to step 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

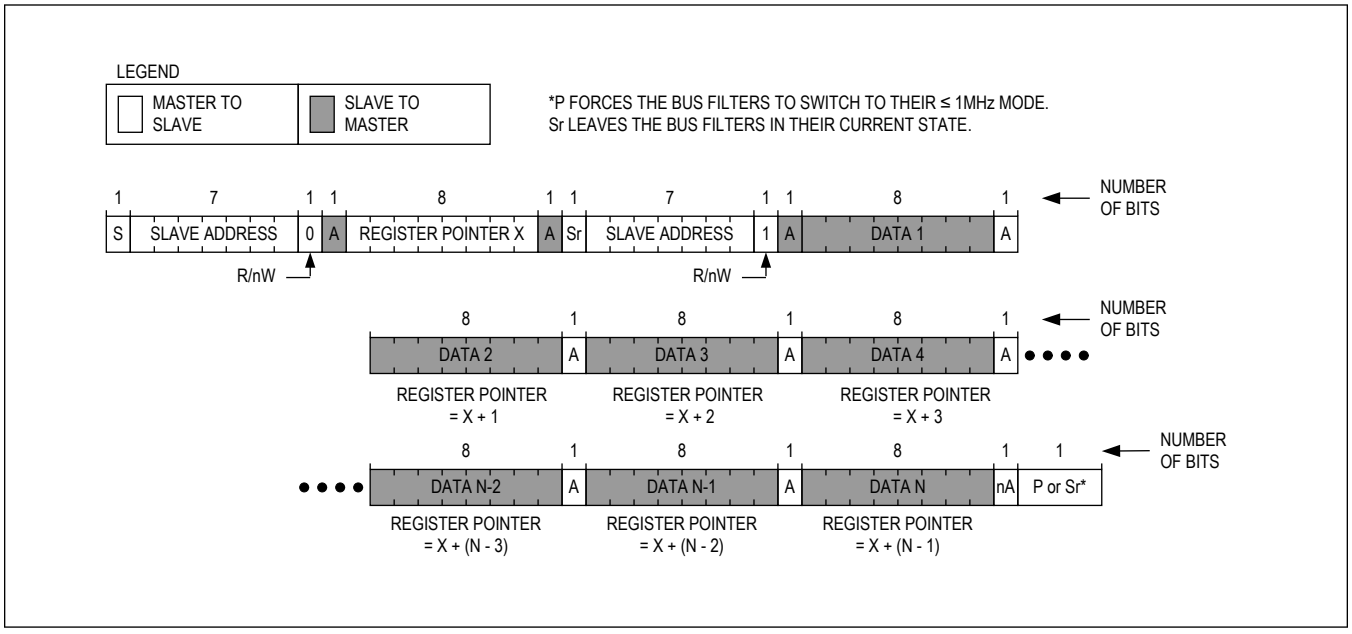


Figure 14. Reading from Sequential Registers

Engage in High-Speed Mode

Figure 15 shows the protocol for engaging in high-speed mode operation, which allows the bus to operate at speeds up to 3.4MHz.

The protocol to engage in high-speed mode is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START condition (S).
3. The master sends the 8-bit master code 0000 1xx0, where ‘xx’ are don’t care bits.
4. The addressed slave issues a NOT-ACKNOWLEDGE (nA).
5. The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a STOP condition (P) is issued. Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation.

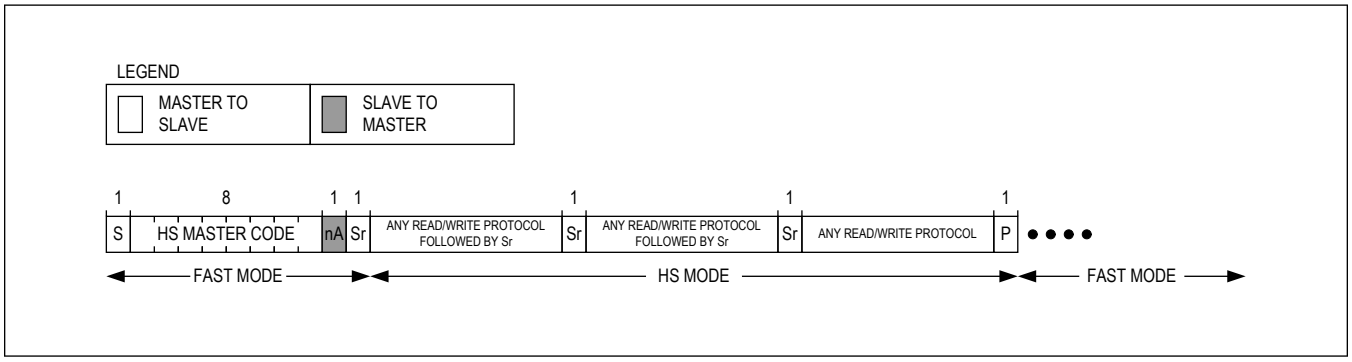


Figure 15. Engage in High-Speed Mode Protocol

The MAX77831 supports the high-speed mode extension feature. This feature keeps the IC in high-speed mode operation even after receiving a STOP condition (P). This eliminates the need for the master device to re-issue the command for engaging in high-speed mode when the master device wants to stay in high-speed mode for multiple read/write cycles.

Figure 16 shows the I^2C mode transition state diagram. Write 1 to the HS_EXT[0] bitfield to enable the high-speed mode extension when the MAX77831 is in low-speed mode. Enabling the high-speed mode extension when the MAX77831 is in high-speed mode is not supported.

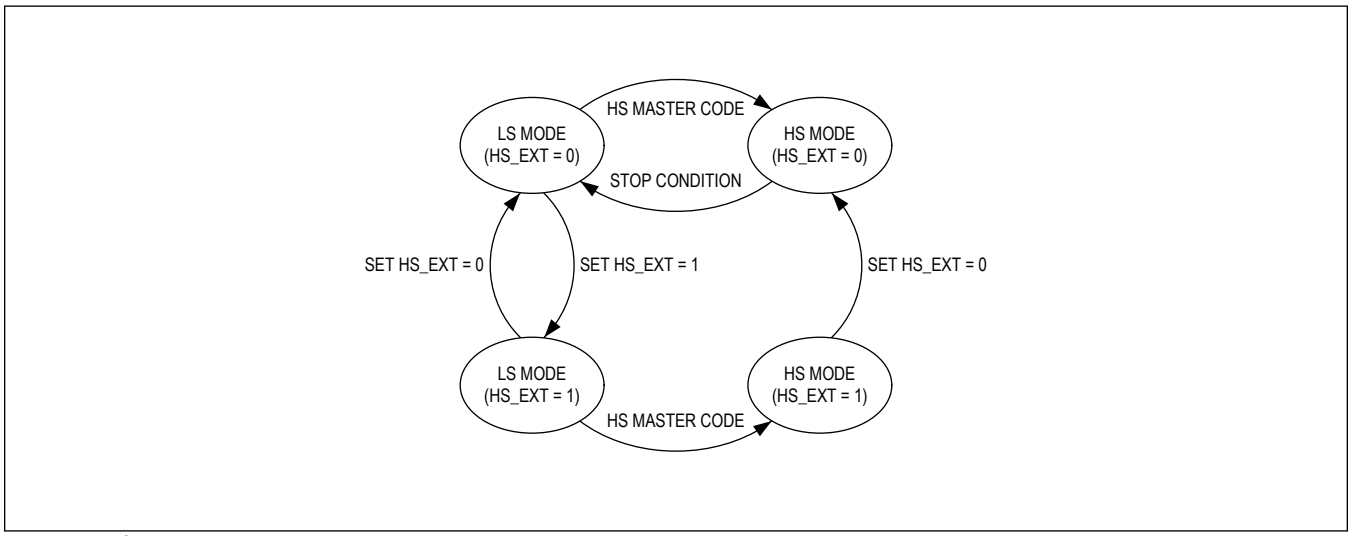


Figure 16. I^2C Operating Mode State Diagram

Register Map

User Registers

Registers reset when shut down.

ADDRESS	NAME	MSB							LSB
User Registers									
0x10	INT_SRC[7:0]	RSVD	RSVD	RSVD	POK	OVP	HARDSHORT	THS	OCP
0x11	INT_MASK[7:0]	RSVD	RSVD	RSVD	POK_M	OVP_M	HARDSHORT_M	THS_M	OCP_M
0x12	REG_CONT1[7:0]	COMP[2:0]			FREQ[1:0]		ILIM[2:0]		
0x13	REG_CONT2[7:0]	VREF[7:0]							
0x14	REG_CONT3[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]		SLEW_RATE[1:0]	
0x15	I2C_CNFG[7:0]	RSVD	RSVD[2:0]			RSVD	RSVD	RSVD	HS_EXT

Register Details

INT_SRC (0x10)

POK and Interrupt Source Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	POK	OVP	HARDSHORT	THS	OCP
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Reads back 0.	N/A
RSVD	6	Reserved. Reads back 0.	N/A
RSVD	5	Reserved. Reads back 0.	N/A
POK	4	Power-OK Status	0: Output voltage is below POK threshold 1: Output voltage is above POK threshold
OVP	3	Overvoltage Protection Interrupt	0: Output overvoltage has NOT been detected 1: Output overvoltage has been detected
HARDSHORT	2	Ouput Hard Short Interrupt	0: Buck-Boost regulator has NOT been latched off due to output hardshort 1: Buck-Boost regulator has been latched off due to output hardshort
THS	1	Thermal Shutdown Interrupt	0: Buck-Boost regulator has NOT been latched off due to thermal shutdown 1: Buck-Boost regulator has been latched off due to thermal shutdown
OCP	0	Overcurrent Protection Interrupt	0: Buck-Boost regulator has NOT been latched off due to overcurrent 1: Buck-Boost regulator has been latched off due to overcurrent

INT_MASK (0x11)

POK and Interrupt Mask Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	POK_M	OVP_M	HARDSHORT_M	THS_M	OCP_M
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved.	N/A
RSVD	6	Reserved.	N/A
RSVD	5	Reserved.	N/A
POK_M	4	Power-OK Status Mask	0: Power-OK status is NOT masked 1: Power-OK status is masked
OVP_M	3	Overvoltage Protection Interrupt Mask	0: Overvoltage protection interrupt is NOT masked 1: Overvoltage protection interrupt is masked
HARDSHORT_M	2	Ouput Hard Short Interrupt Mask	0: Ouput hard short interrupt is NOT masked 1: Ouput hard short interrupt is masked
THS_M	1	Thermal Shutdown Interrupt Mask	0: Thermal shutdown interrupt is NOT masked 1: Thermal shutdown interrupt is masked
OCP_M	0	Overcurrent Protection Interrupt Mask	0: Overcurrent protection interrupt is NOT masked 1: Overcurrent protection interrupt is masked

REG_CONT1 (0x12)

Control Register 1

BIT	7	6	5	4	3	2	1	0
Field	COMP[2:0]			FREQ[1:0]		ILIM[2:0]		
Reset	0b010			0b10		0b000		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
COMP	7:5	Internal Compensation R_C Option (Bandwidth)	000: R_C = 30kΩ, Buck mode R_C = 20kΩ, Boost mode 001: R_C = 45kΩ, Buck mode R_C = 30kΩ, Boost mode 010: R_C = 60kΩ, Buck mode R_C = 45kΩ, Boost mode (Default) 011: R_C = 70kΩ, Buck mode R_C = 50kΩ, Boost mode 100: R_C = 80kΩ, Buck mode R_C = 55kΩ, Boost mode 101: R_C = 90kΩ, Buck mode R_C = 60kΩ, Boost mode 110: R_C = 110kΩ, Buck mode R_C = 75kΩ, Boost mode 111: R_C = 150kΩ, Buck mode R_C = 100kΩ, Boost mode

BITFIELD	BITS	DESCRIPTION	DECODE
FREQ	4:3	Switching Frequency	00: 1.2MHz 01: 1.5MHz 10: 1.8MHz (Default) 11: Reserved. Do not write this value.
ILIM	2:0	High-Side Switching Current Limit	000: 7.0A 001: 6.2A 010: 5.6A 011: 4.6A 100: 3.8A 101: 2.73A 110: 1.72A 111: 0.98A

REG_CONT2 (0x13)

Control Register 2

BIT	7	6	5	4	3	2	1	0
Field	VREF[7:0]							
Reset	0b01000100							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VREF	7:0	Internal Reference Voltage	0x00–0x3C: 0.299V 0x3D–0xCC: 4.9mV/LSB in a linear transfer function between 0.299V (0x3D) and 1.000V (0xCC) 0xCD–0xFF: 1.000V Default: 0x44: 0.333V

REG_CONT3 (0x14)

Control Register 3

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]		SLEW_RATE[1:0]	
Reset	0b0	0b0	0b1	0b0	0b11		0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved.	N/A
RSVD	6	Reserved.	N/A
RSVD	5	Reserved.	N/A
RSVD	4	Reserved.	N/A
RSVD	3:2	Reserved.	N/A

BITFIELD	BITS	DESCRIPTION	DECODE
SLEW_RATE	1:0	Internal Reference DVS Ramp Rate. See the *Output Voltage Configuration* section for equations to convert the V_{REF} DVS ramp rate to the V_{OUT} ramp rate.	00: 7/6mV/µs (FREQ = 00 or 01), 4/3mV/µs (FREQ = 10) (Default) 01: 2/3mV/µs 10: 1/3mV/µs 11: 1/6mV/µs (FREQ = 00 or 01), 17/75mV/µs (FREQ = 10)

I2C_CNFG (0x15)

I²C Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD[2:0]			RSVD	RSVD	RSVD	HS_EXT
Reset	0b0	0x00			0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved.	N/A
RSVD	6:4	Reserved.	N/A
RSVD	3	Reserved.	N/A
RSVD	2	Reserved.	N/A
RSVD	1	Reserved.	N/A
HS_EXT	0	I²C High-Speed Mode Extension Control	0: I²C high-speed mode extension is disabled 1: I²C high-speed mode extension is enabled

Revision Register

Register does not reset.

ADDRESS	NAME	MSB							LSB
Revision Register									
0x80	REG_REV[7:0]	REVISION[2:0]			VERSION[4:0]				

Register Details

REG_REV (0x80)

IC Revision and Version

BIT	7	6	5	4	3	2	1	0
Field	REVISION[2:0]			VERSION[4:0]				
Reset	0b000			0b00000				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
REVISION	7:5	IC Revision	011: Pass 3 111: Pass 1 or 2
VERSION	4:0	IC Version	Contact factory

Applications Information

Software (I^2C) Control

Control the converter using software commands sent over the I^2C serial interface.

Assert V_{IO} valid and connect the SDA and SCL to a serial host to enable the serial bus and full software control of the IC. When using software, the serial host can do the following:

- Monitor the overvoltage protection interrupt using the OVP[0] bitfield.
- Monitor the overcurrent protection interrupt using the OCP[0] bitfield.
- Monitor the output hardshort interrupt using the HARDSHORT[0] bitfield.
- Monitor the thermal shutdown interrupt using the THS[0] bitfield.
- Change the individual POK and fault interrupt mask using the OVP_M[0], OCP_M[0], HARDSHORT_M[0], and THS_M[0] bitfields.
- Change the target output voltage (V_{OUT}) by setting the internal reference voltage (V_{REF}) using the VREF[7:0] bitfield.
- Change the slew rate of the output voltage change ($\Delta VOUT/\Delta t$) using the SLEW_RATE[1:0] bitfield.
- Change the switching current limit threshold (I_{LIM}) using the ILIM[2:0] bitfield.
- Change the switching frequency using the FREQ[1:0] bitfield.
- Change the internal compensation option using the COMP[2:0] bitfield.

The configuration registers reset when V_{IO} becomes invalid, when IN falls below the UVLO falling threshold (V_{UVLO_F}), or when EN is logic LOW. See the *Detailed Description—I^2C Serial Interface* section and the *Register Map* section for more information.

Non-I^2C Operation

The MAX77831 can operate without I^2C software control. The switching current limit can be configured by a resistor (R_{SEL}) connecting the SEL pin to AGND. The output voltage can be configured by external feedback resistors. See the *SEL Pin Configuration* section and the *Output Voltage Configuration* section for more information. If the I^2C serial interface is not in use, connect the SCL and SDA pins to AGND to avoid unwanted behavior.

Inductor Selection

Select an inductor with a saturation current rating (I_{SAT}) greater than or equal to the maximum high-side switching current limit threshold (I_{LIM}) setting. In general, inductors with lower saturation current and high DCR ratings are physically small. Higher values of DCR reduce converter efficiency. Choose the RMS current rating (I_{RMS}) of the inductor (the current at which the temperature rises appreciably) based on the expected load current.

The chosen inductor value should ensure that the peak-inductor ripple current (I_{PEAK}) is below the I_{LIM} setting so that the converter can maintain regulation. A 1.5µH inductor is recommended throughout the operation range of the converter. Table 4 lists recommended inductors.

Table 4. Inductor Recommendations

VENDOR	PART NUMBER	NOMINAL INDUCTANCE (µH)	TYPICAL DCR (mΩ)	I_{SAT} (A)	I_{RMS} (A)	DIMENSIONS L x W x H (mm)	I_{LIM} SETUP
Sumida	CDMT40D20HF-1R5NC	1.5	19.5	7.1	7.5	4.0 x 4.0 x 2.1	ILIM[2:0] = 000 (7.00A)
Coilcraft	XEL4020-152MEC	1.5	21.45	7.4	7.5	4.0 x 4.0 x 2.1	ILIM[2:0] = 000 (7.00A)
TDK	VLS3012HBX-1R0M	1.0	39	6.11	5.13	3.0 x 3.0 x 1.2	ILIM[2:0] = 100 (3.80A)
Samsung	CIGT252010EH1R0MNE	1.0	26	5	4.3	2.5 x 2.0 x 1.0	ILIM[2:0] = 100 (3.80A)

Table 4. Inductor Recommendations (continued)

VENDOR	PART NUMBER	NOMINAL INDUCTANCE (µH)	TYPICAL DCR (mΩ)	I_{SAT} (A)	I_{RMS} (A)	DIMENSIONS L x W x H (mm)	I_{LIM} SETUP
Cyntec	HTEH16080H-1R0MSR	1.0	95	2.1	1.8	1.6 x 0.8 x 0.8	ILIM[2:0] = 110 (1.72A)
Murata	DFE18SBN1R0ME0L	1.0	120 (max)	1.9	1.8	1.6 x 0.8 x 0.8	ILIM[2:0] = 111 (0.98A)

Input Capacitor Selection

For most applications, bypass the IN pin with two 25V 10µF nominal ceramic input capacitors (C_{IN}) that maintain 1µF or higher effective capacitance at its working voltage. Effective C_{IN} is the actual capacitance value seen from the converter input during operation. Larger values improve decoupling for the converter, but increase inrush current from the voltage supply when connected. C_{IN} reduces the current peaks drawn from the input power source and reduces switching noise in the system. The ESR/ESL of C_{IN} and its series PCB trace should be very low (i.e., < 15mΩ + < 2nH) for frequencies up to the converter's switching frequency.

Pay special attention to the capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{IN}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the converter. Choose the effective C_{OUT} to be 8.2µF minimum. Effective C_{OUT} is the actual capacitance value seen by the converter output during operation. Larger values (above the required effective minimum) improve load transient performance but increase the input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR for frequencies up to the converter's switching frequency to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. For most applications, two 25V 22µF capacitors are recommended for C_{OUT}.

Pay special attention to the capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{OUT}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Other Required Component Selection

Table 5 illustrates the requirements for other required components.

Table 5. Other Component Selection Requirements

SYMBOL	COMPONENT	PARAMETER	MIN	TYP	MAX	UNITS
C_{BST}	High-Side FET Driver Bootstrap Capacitor	Suggested Capacitance		0.22		µF
C_{VL}	V_L Regulator Bypass Capacitor	Effective Capacitance	0.5		3	µF
		Equivalent Series Resistance (ESR)			100	mΩ
C_{VIO}	V_{IO} Regulator Bypass Capacitor	Effective Capacitance	0.3		1.5	µF
		Equivalent Series Resistance (ESR)			100	mΩ
R_{SEL}	SEL Pin Resistor	Acceptable Tolerance	-1		+1	%
R_{PU}	POKB/INTB Pullup Resistor	Suggested Resistance		15		kΩ

PCB Layout Guideline

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. If the POK or fault interrupt functionality is desired, the high-density interconnect (HDI) PCB is required to route to the POKB/INTB pin. Otherwise, the HDI PCB is recommended but not required. Figure 17 and Figure 18 show example non-HDI and HDI PCB layouts for the MAX77831 WLP package.

When designing the PCB, follow these guidelines:

1. Place the input capacitors (C_{IN}) and output capacitors (C_{OUT}) immediately next to the IN pin and OUT pin of the IC, respectively. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
2. Place the inductor next to the LX bumps (as close as possible) and make the traces between the LX bumps and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3. Route LX nodes to its corresponding bootstrap capacitor (C_{BST}) as short as possible. Prioritize C_{BST} placement to reduce trace length to the IC.
4. Connect the inner PGND bumps to the low-impedance ground plane on the PCB with vias placed next to the bumps. Do not create PGND islands, as PGND islands risk interrupting the hot loops. Connect AGND and AGND island to the low-impedance ground plane on the PCB (the same net as PGND).
5. Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
6. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

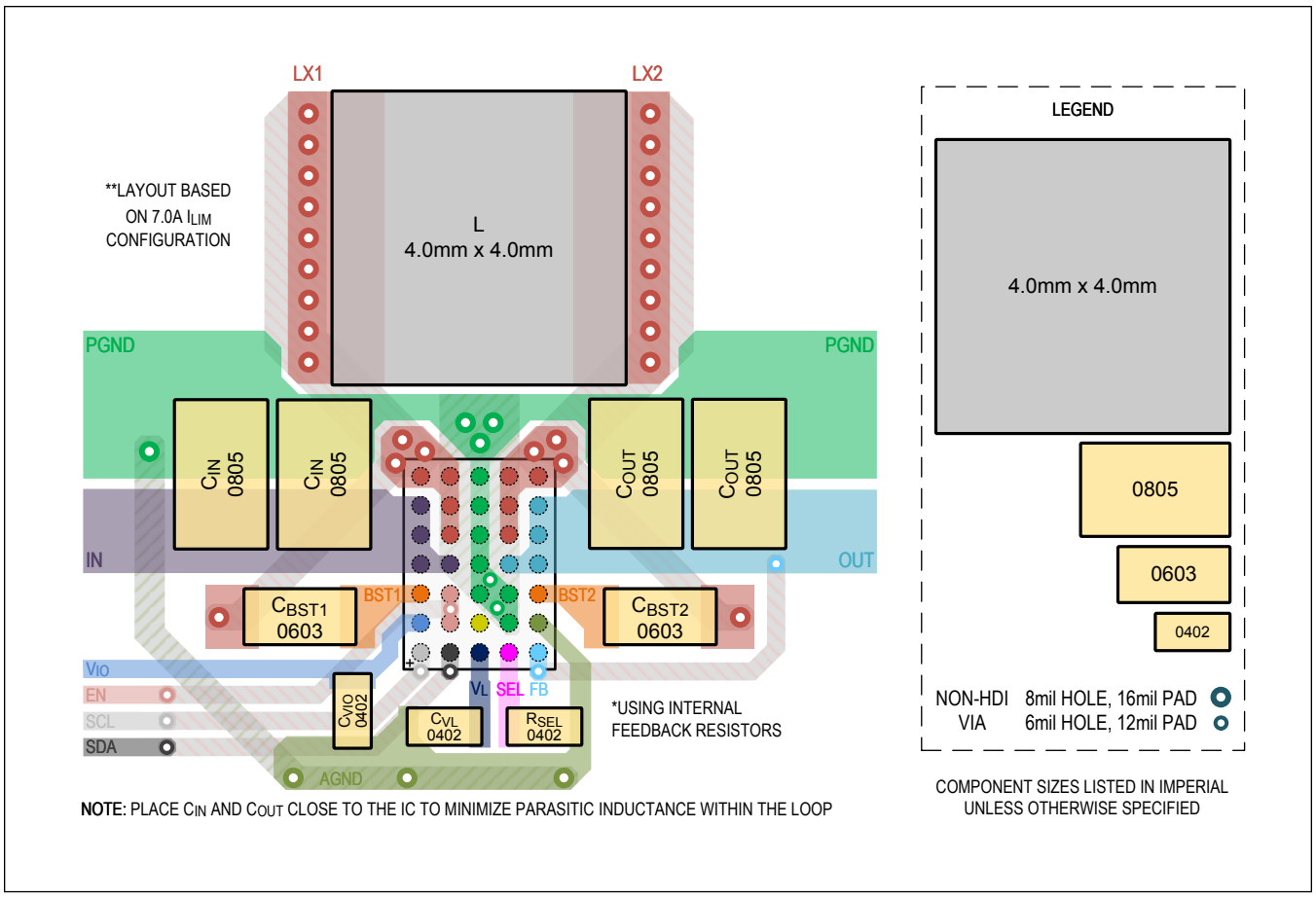


Figure 17. Non-HDI PCB Layout Recommendation for 35 WLP Package (with 4mm x 4mm Inductor and without POKB/INTB)

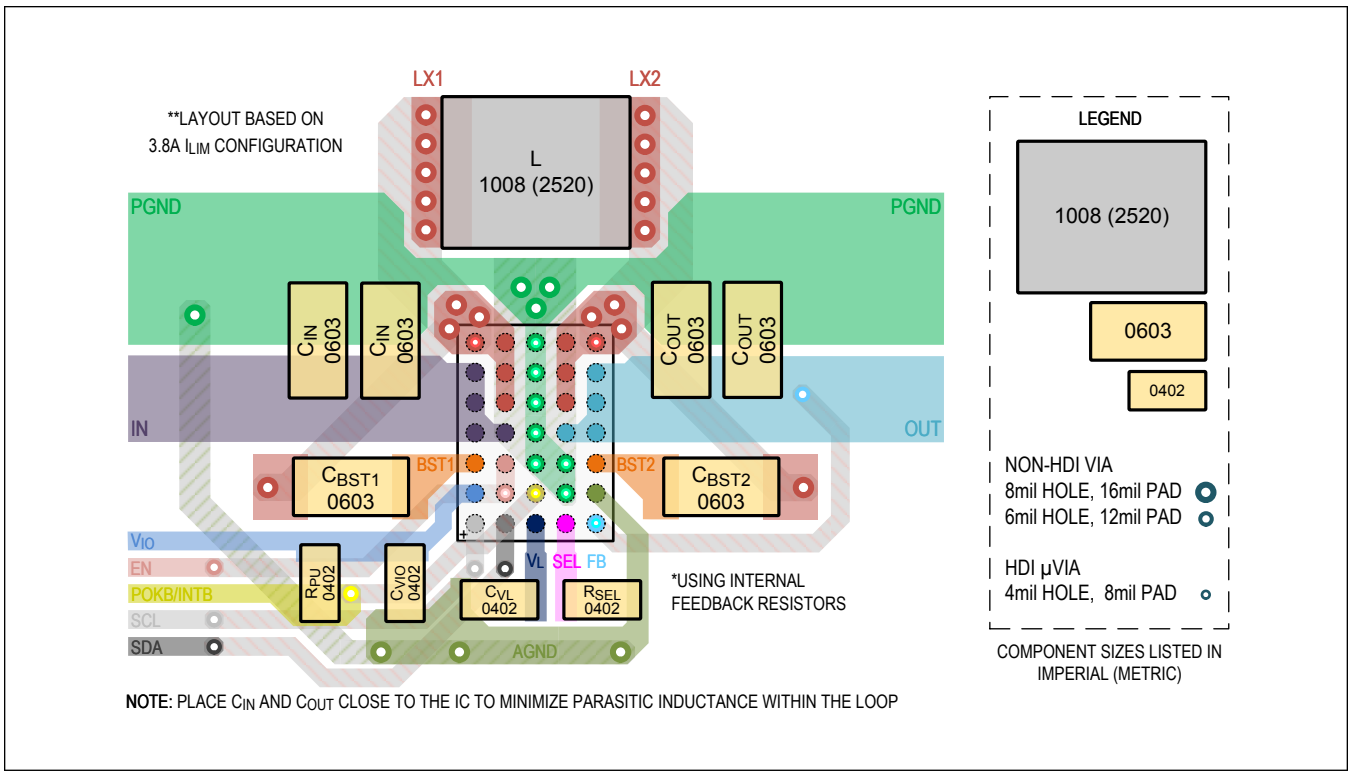
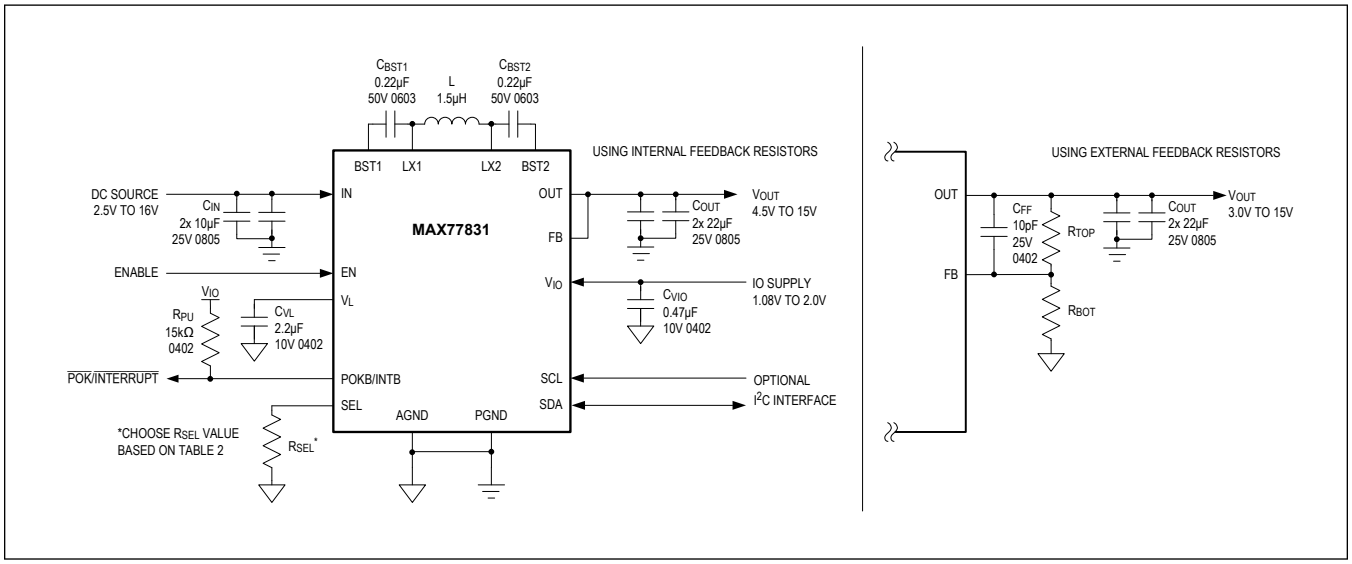


Figure 18. HDI PCB Layout Recommendation for 35 WLP Package (with 2520 Inductor and POKB/INTB)

Typical Application Circuits



Ordering Information

PART NUMBER	DEFAULT SWITCHING FREQUENCY	DEFAULT OUTPUT VOLTAGE	PIN-PACKAGE
MAX77831BEWB+T	1.8MHz	5V	35 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

For other switching frequency options, please contact sales representatives for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/20	Initial release	—
1	10/20	Updated *General Description*, *Benefits and Features*, *Simplified Block Diagram*, *Absolute Maximum Ratings*, *Package Information*, *Electrical Characteristics* table, *Pin Configuration*, *Pin Description*, *Functional Diagram*, *Detailed Description*, *Soft-Start*, *Shutdown*, *Immediate Shutdown and Latch-Off Conditions*, *Output Active Discharge*, *Power-OK Monitor and Fault Interrupts*, *Output Voltage Configuration*, *Overcurrent Protection (OCP)*, *Thermal Shutdown*, REG_CONT1 (0x12) description, *Software (I^2C) Control*, *Non-I^2C Operation*, Table 4, *PCB Layout Guideline*, *Typical Application Circuits* sections, and *Ordering Information* table; added *Typical Operating Characteristics*, *Internal Compensation Options*, and *Other Required Component Selection* sections	1, 2, 7, 8, 10, 14–23, 25, 27–31, 43–51