GaAs, pHEMT, MMIC, Low Noise Amplifier, 14 GHz to 24 GHz

FEATURES

- Low noise, high gain LNA for Ku and K band
- Frequency range: 14 GHz to 24 GHz
- Low noise figure: 1.4 dB typical at 15 GHz to 22 GHz
- High gain: 29 dB typical at 14 GHz to 15 GHz
- Integrated AC coupling capacitors
- Integrated bias inductor
- Single positive supply: 2 V with I_{DQ} = 25 mA
- RBIAS drain current adjustment pin
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Ku band and K band satellite communications

GENERAL DESCRIPTION

The ADL8141 is a low power consumption, low noise amplifier that operates from 14 GHz to 24 GHz. Typical gain, noise figure, and output third-order intercept (OIP3) are 29 dB, 1.4 dB, and 18 dBm, respectively. Typical supply current is 25 mA from a 2 V supply. OIP3 and output power for 1 dB compression (OP1dB) can be increased by adjusting a supply-referenced resistor connected to the RBIAS pin. The RF input and output of the ADL8141 are internally matched and AC-coupled.

The ADL8141 is fabricated on a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC) process. The ADL8141 is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP and is specified for operation from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

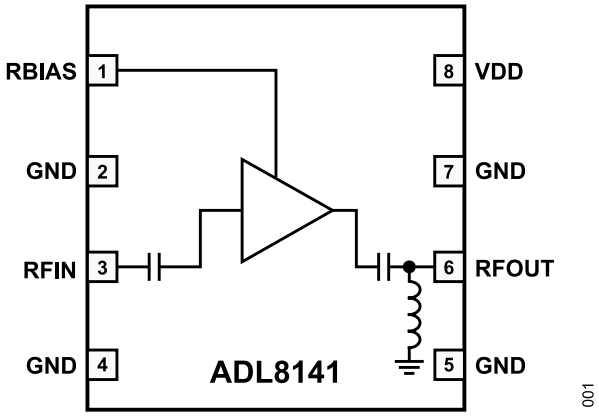

Figure 1. Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

7/2023—Revision 0: Initial Version

SPECIFICATIONS

14 GHz TO 15 GHz FREQUENCY RANGE

Supply voltage (V_{DD}) = 2 V, quiescent current (I_{DQ}) = 25 mA, bias reference (R_{BIAS}) = 768 Ω, and T_C = 25°C, unless otherwise noted.

Table 1. 14 GHz to 15 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	14		15	GHz	
GAIN	27	29		dB	
Gain Variation over Temperature		0.025		dB/°C	
NOISE FIGURE		1.7		dB	
RETURN LOSS					
Input (S11)		12.5		dB	
Output (S22)		7		dB	
OUTPUT					
OP1dB	3.5	6		dBm	
Saturated Output Power (P_{SAT})		9		dBm	
OIP3		11		dBm	Measurement taken at output power (P_{OUT}) per tone = −2 dBm
Second-Order Intercept (OIP2)		8.5		dBm	Measurement taken at P_{OUT} per tone = −2 dBm

15 GHz TO 22 GHz FREQUENCY RANGE

V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω, and T_C = 25°C, unless otherwise noted.

Table 2. 15 GHz to 22 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	15		22	GHz	
GAIN	26.5	28.5		dB	
Gain Variation over Temperature		0.024		dB/°C	
NOISE FIGURE		1.4		dB	
RETURN LOSS					
S11		15		dB	
S22		12		dB	
OUTPUT					
OP1dB	6	9		dBm	
P_{SAT}		11.5		dBm	
OIP3		18		dBm	Measurement taken at P_{OUT} per tone = −2 dBm
OIP2		23		dBm	Measurement taken at P_{OUT} per tone = −2 dBm

22 GHz TO 24 GHz FREQUENCY RANGE

V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω, and T_C = 25°C, unless otherwise noted.

Table 3. 22 GHz to 24 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	22		24	GHz	
GAIN		26		dB	
Gain Variation over Temperature		0.033		dB/°C	
NOISE FIGURE		1.5		dB	
RETURN LOSS					
S11		13.5		dB	
S22		5		dB	

SPECIFICATIONS

Table 3. 22 GHz to 24 GHz Frequency Range Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT					
OP1dB		11		dBm	
P_{SAT}		12		dBm	
OIP3		17		dBm	Measurement taken at P_{OUT} per tone = −2 dBm
OIP2		31		dBm	Measurement taken at P_{OUT} per tone = −2 dBm

DC SPECIFICATIONS

Table 4. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		25		mA
Amplifier Current (I_{DQ_AMP})		23		mA
RBIAS Current (I_{RBIAS})		2		mA
SUPPLY VOLTAGE				
V_{DD}	1.5	2	3.5	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	4 V
RF Input Power (RFIN)	20 dBm
Pulsed RFIN (Duty Cycle = 10%, Pulse Width = 100 µs)	22 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 5.71 mW/°C Above 85°C)	0.51 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 2 V, I_{DQ} = 25 mA, Input Power (P_{IN}) = Off)	93.75°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	141	°C/W
Worst Case[1], T_{CASE} = 85°C	175	°C/W

[1] Worst case across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8141

Table 7. ADL8141, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

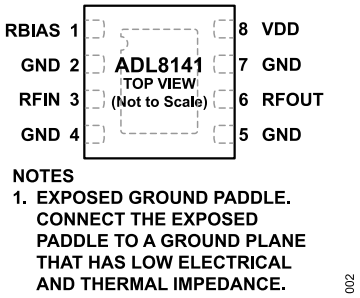

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the I_{DQ}. See Figure 72 and Table 9 for more details. See Figure 3 for the interface schematic.
2, 4, 5, 7	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
3	RFIN	RF Input. The RFIN pin is AC-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
6	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 5 for the interface schematic.
	EXPOSED PADDLE	Exposed Ground Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

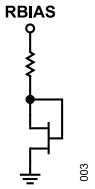

Figure 3. RBIAS Interface Schematic

Figure 4. RFIN Interface Schematic

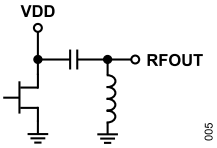

Figure 5. RFOUT/VDD Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

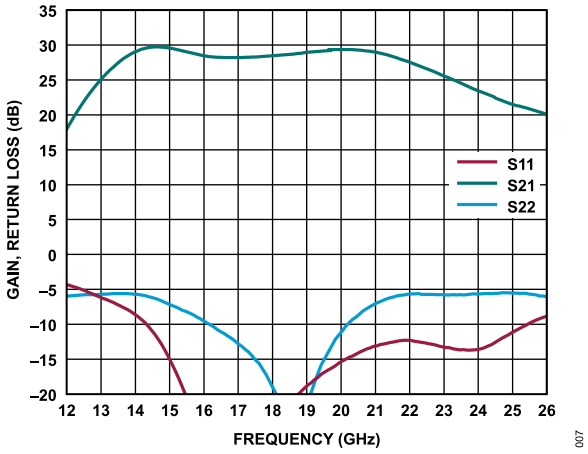

Figure 7. Broadband Gain and Return Loss vs. Frequency, V_{DD} = 2 V, I_{DQ} = 25 mA

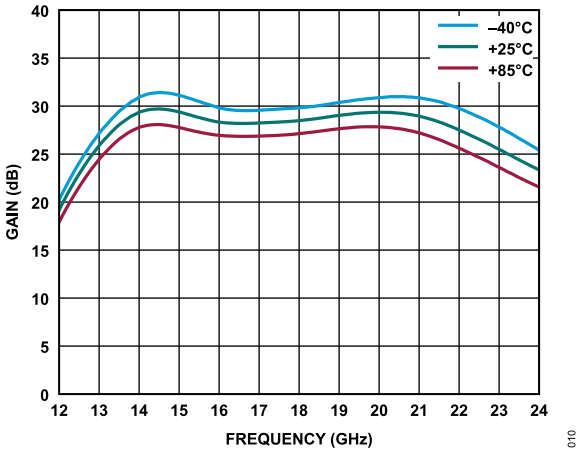

Figure 10. Gain vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

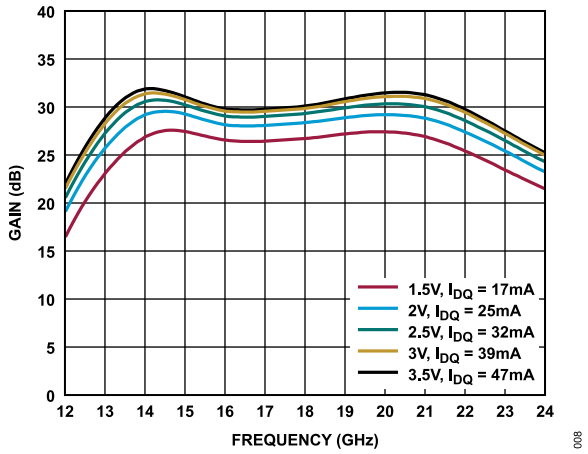

Figure 8. Gain vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 768 Ω

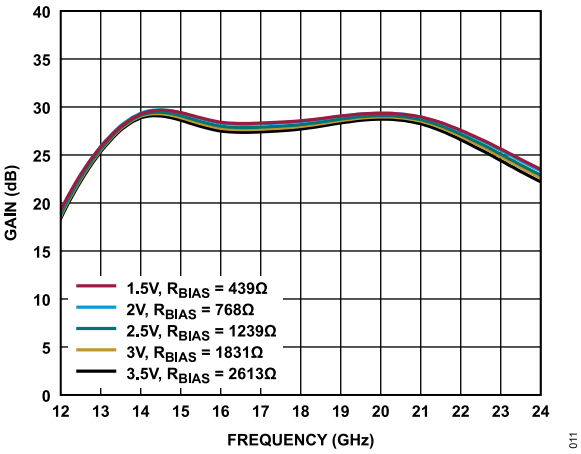

Figure 11. Gain vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

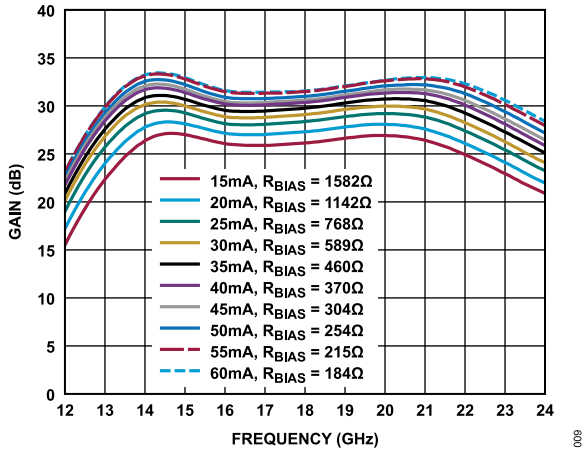

Figure 9. Gain vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

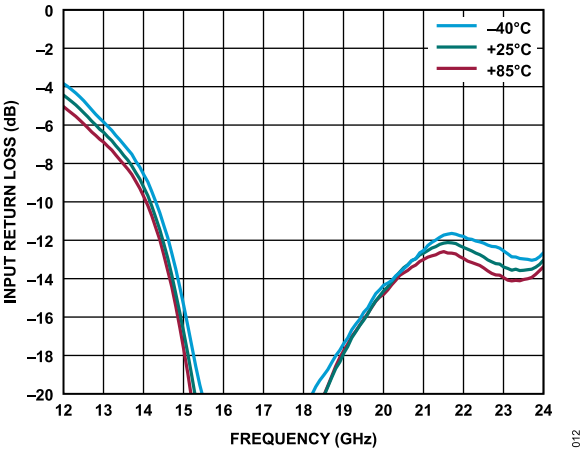

Figure 12. Input Return Loss vs. Frequency for Various Temperature, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

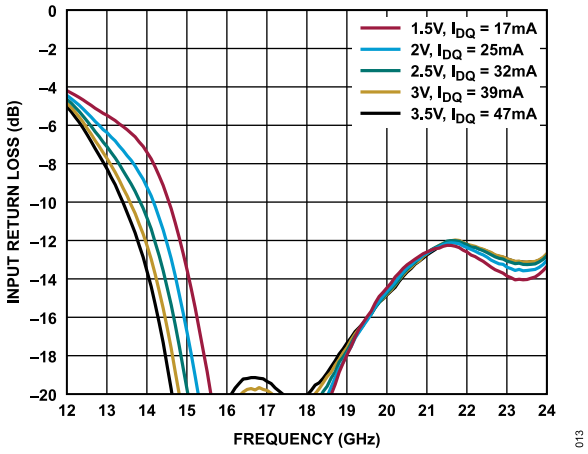

Figure 13. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

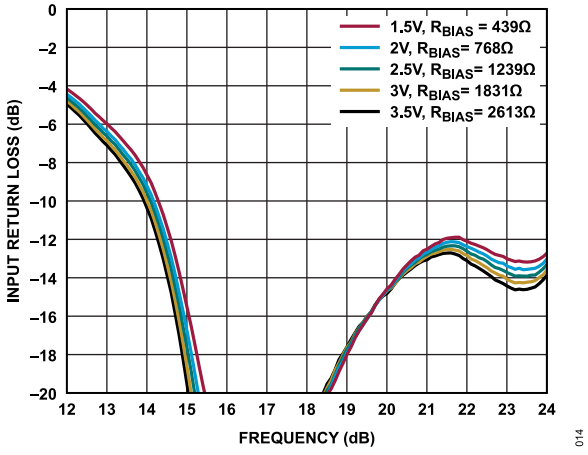

Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

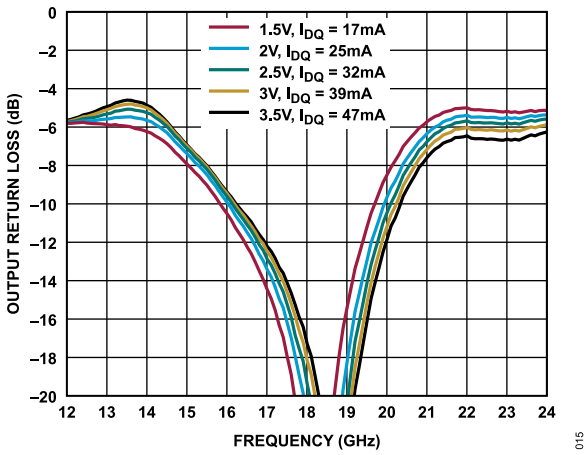

Figure 15. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

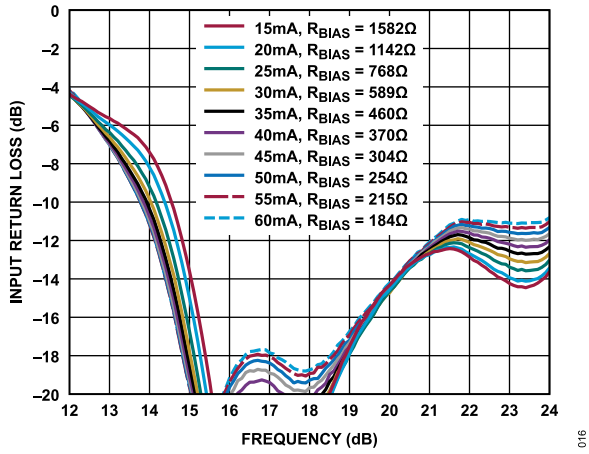

Figure 16. Input Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

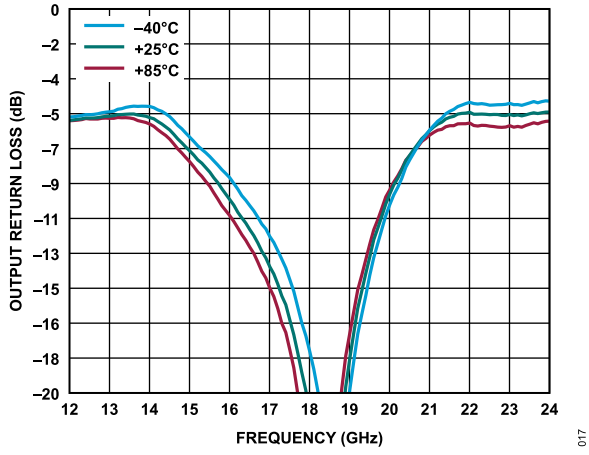

Figure 17. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

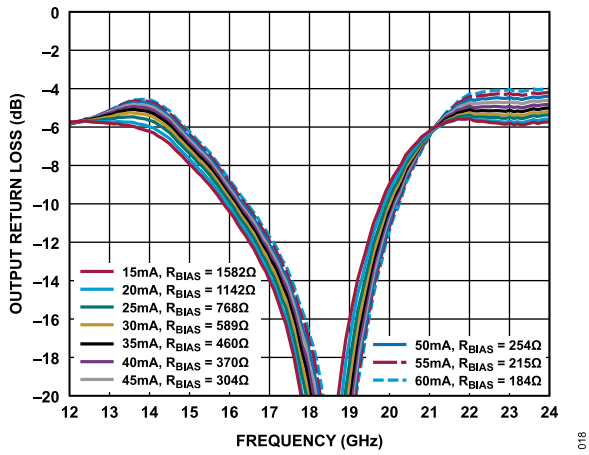

Figure 18. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

TYPICAL PERFORMANCE CHARACTERISTICS

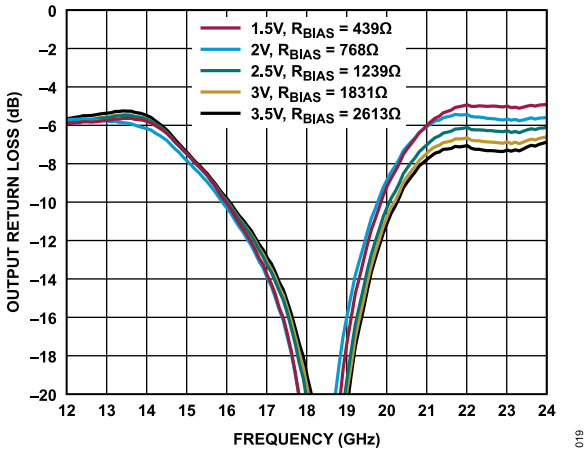

Figure 19. Output Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

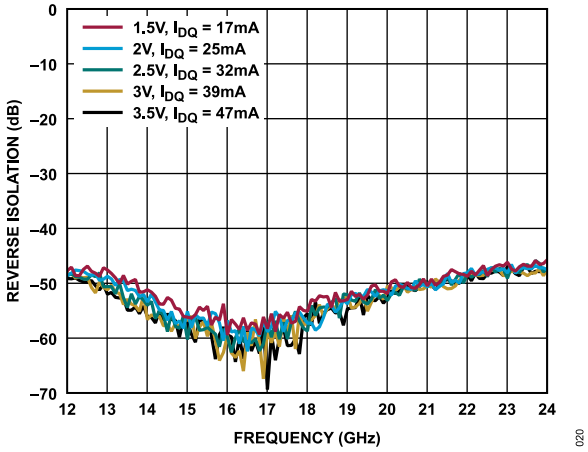

Figure 20. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

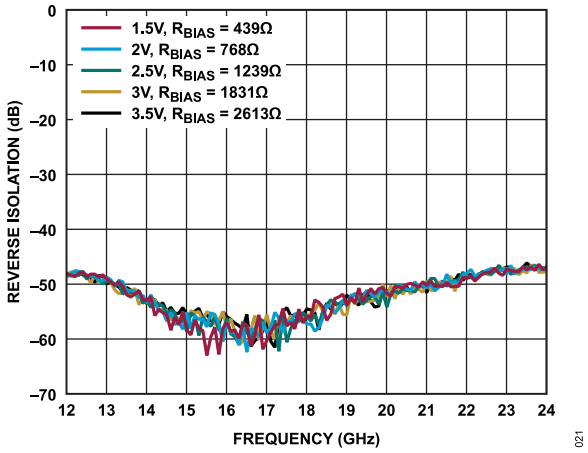

Figure 21. Reverse Isolation vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

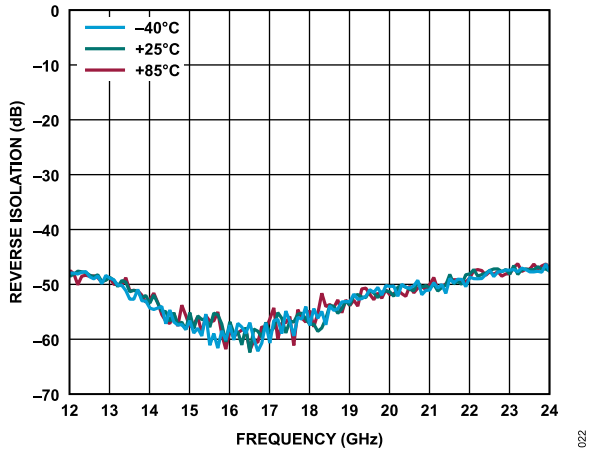

Figure 22. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

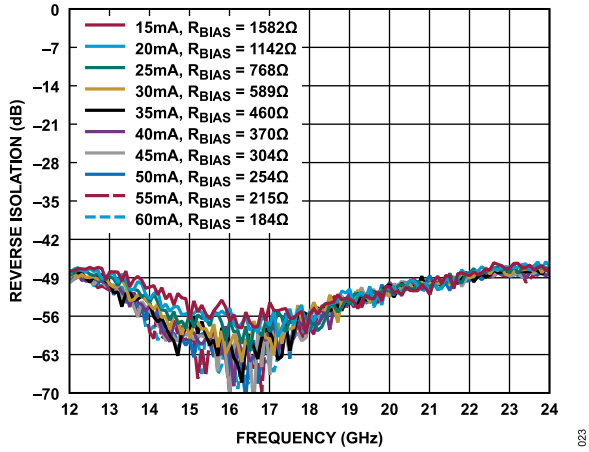

Figure 23. Reverse Isolation vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

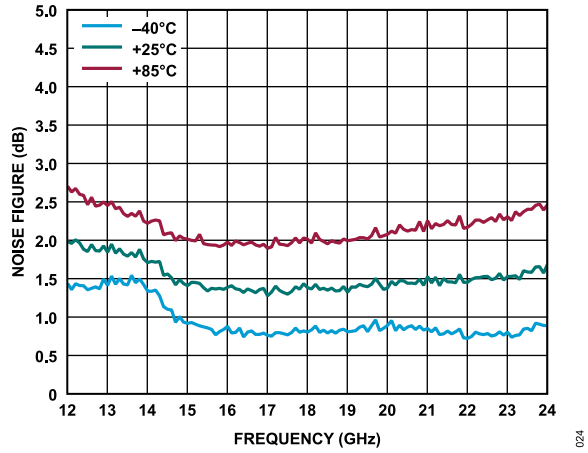

Figure 24. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

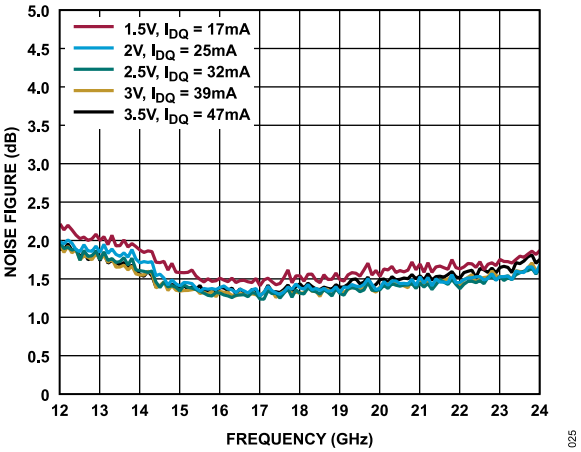

Figure 25. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

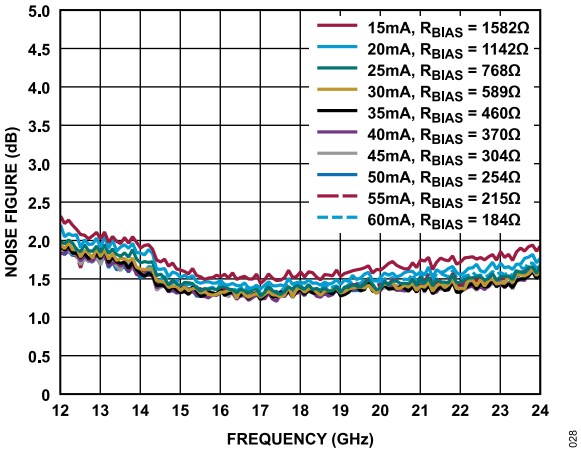

Figure 28. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

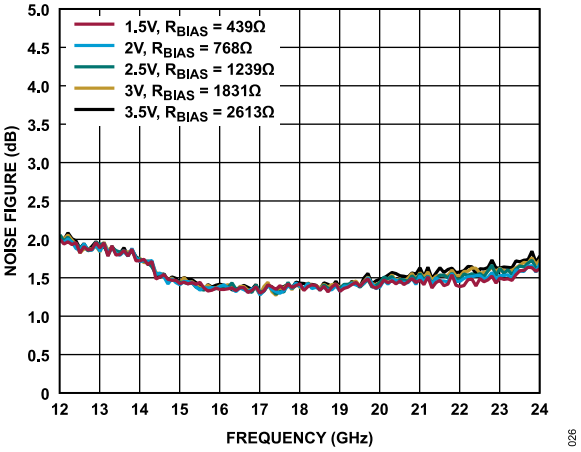

Figure 26. Noise Figure vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

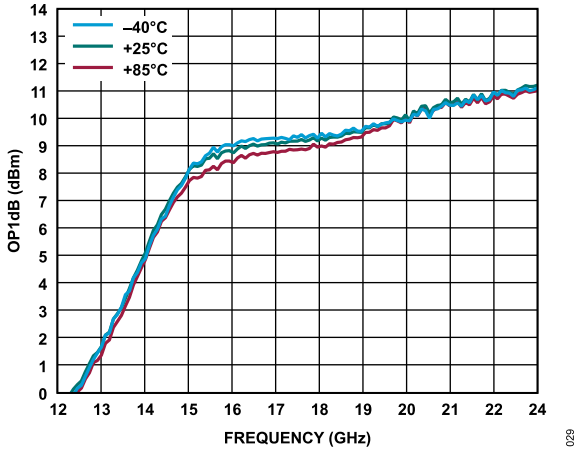

Figure 29. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

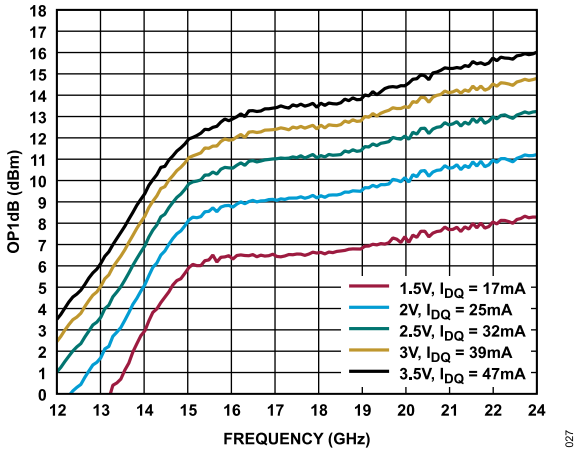

Figure 27. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

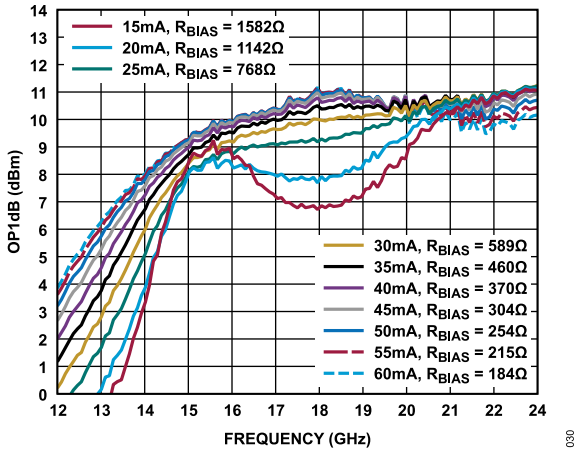

Figure 30. OP1dB vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

TYPICAL PERFORMANCE CHARACTERISTICS

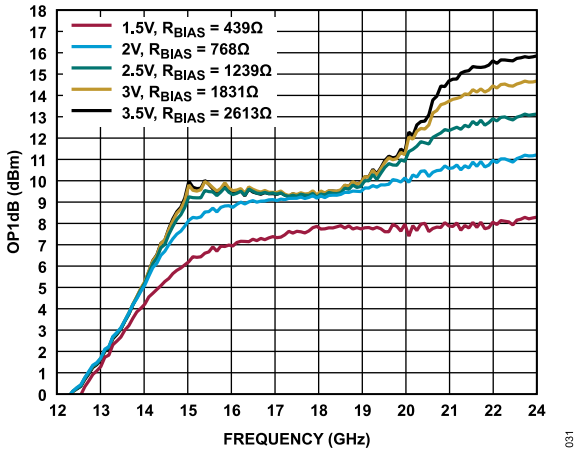

Figure 31. OP1dB vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

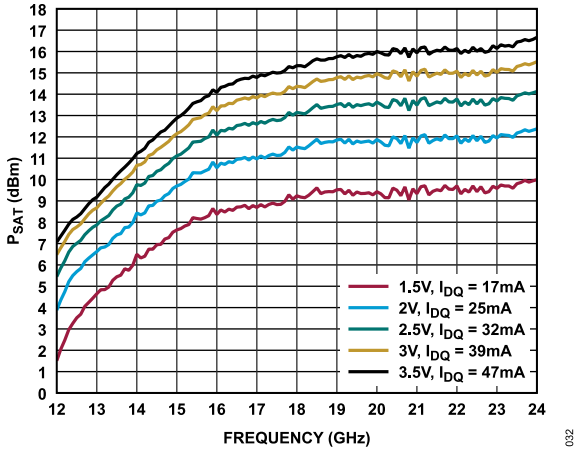

Figure 32. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

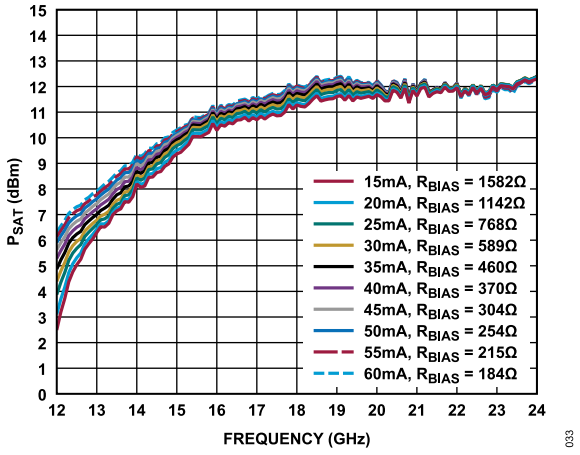

Figure 33. P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

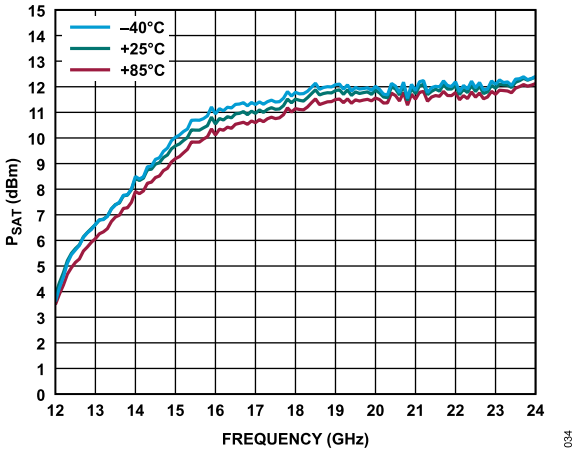

Figure 34. P_{SAT} vs. Frequency for Various Temperature, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

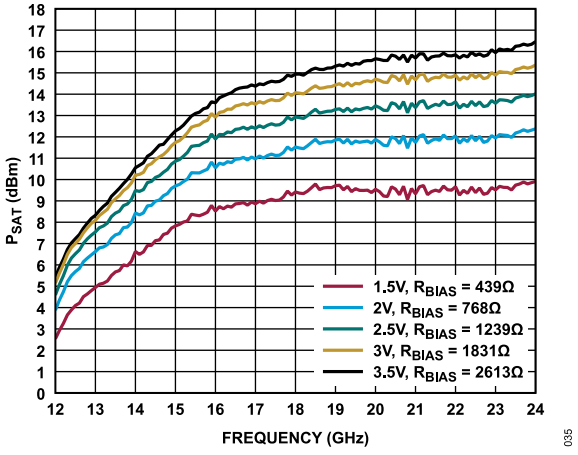

Figure 35. P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

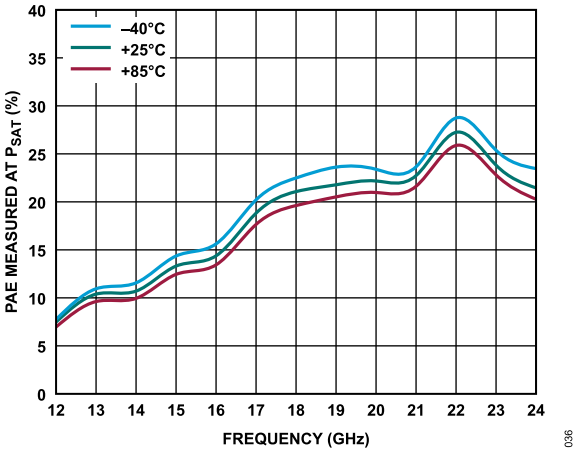

Figure 36. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 2 V and I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

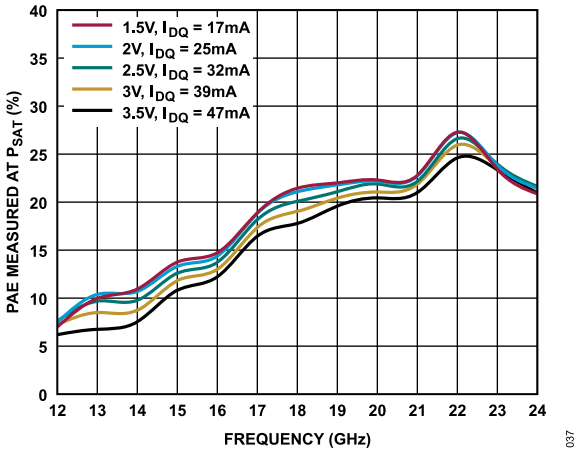

Figure 37. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

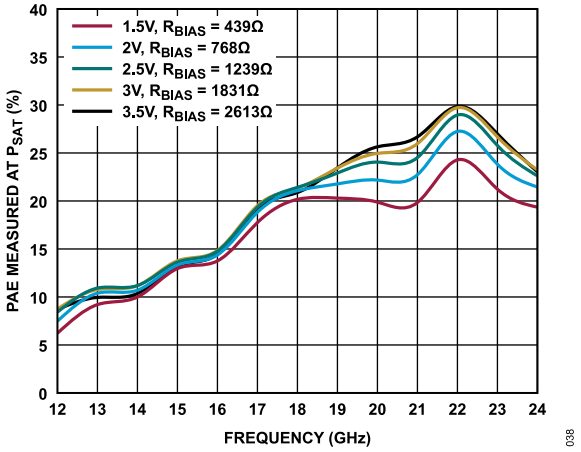

Figure 38. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

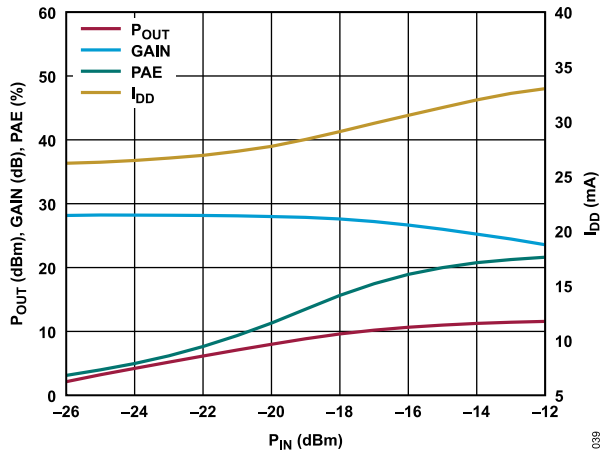

Figure 39. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 19 GHz, V_{DD} = 2 V, R_{BIAS} = 768 Ω

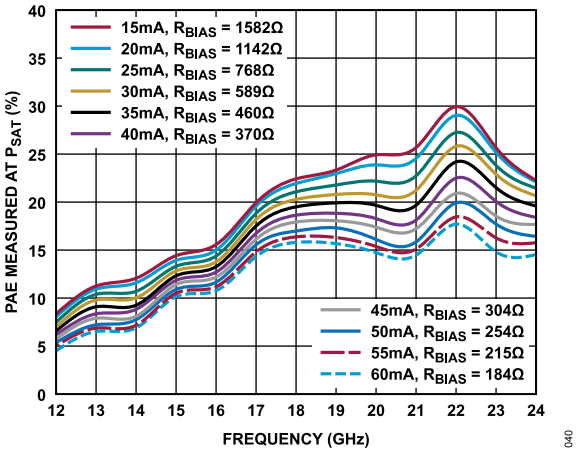

Figure 40. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

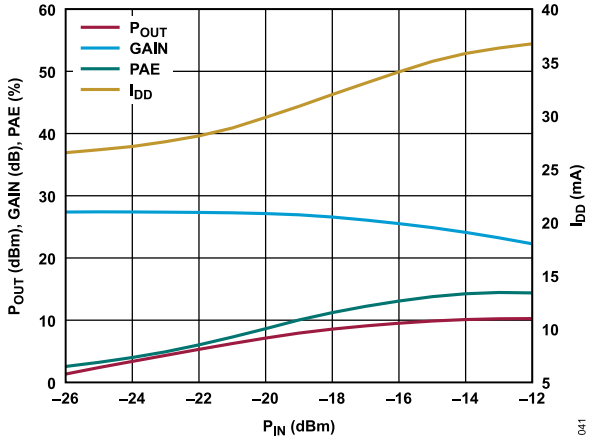

Figure 41. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 16 GHz, V_{DD} = 2 V, R_{BIAS} = 768 Ω

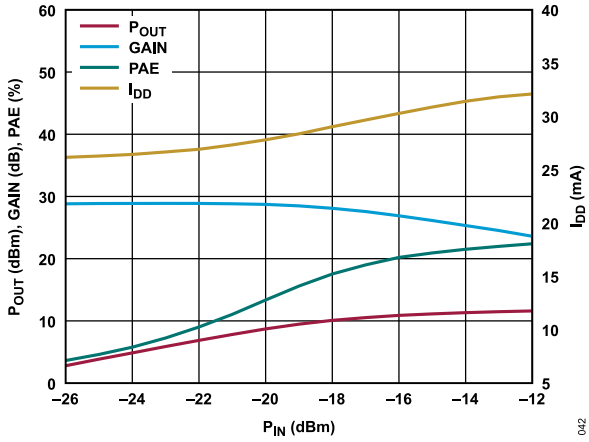

Figure 42. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 21 GHz, V_{DD} = 2 V, R_{BIAS} = 768 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

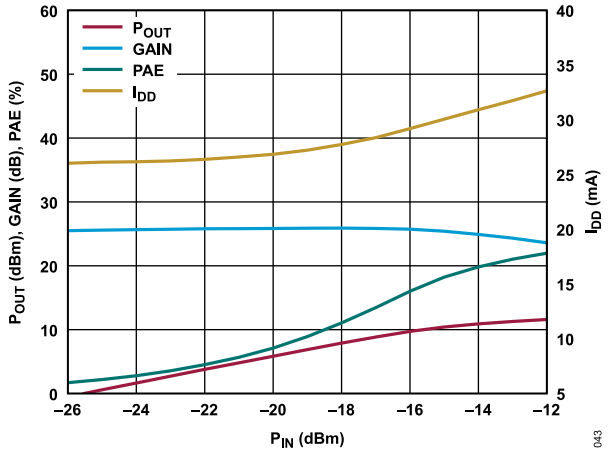

Figure 43. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 23 GHz, V_{DD} = 2 V, R_{BIAS} = 768 Ω

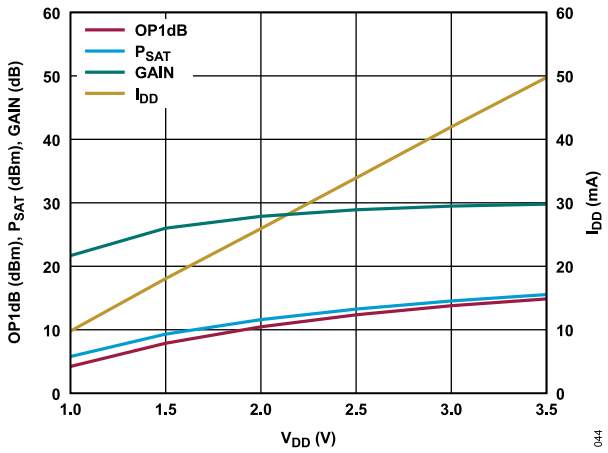

Figure 44. OP1dB, P_{SAT}, Gain, and I_{DD} vs. V_{DD} at 19 GHz, R_{BIAS} = 768 Ω

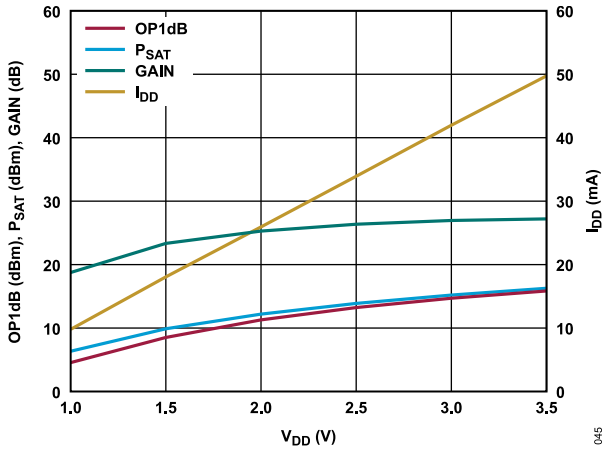

Figure 45. OP1dB, P_{SAT}, Gain, and I_{DD} vs. V_{DD} at 23 GHz, R_{BIAS} = 768 Ω

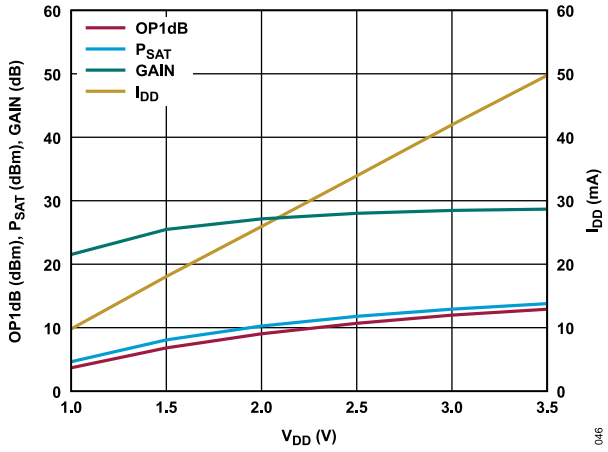

Figure 46. OP1dB, P_{SAT}, Gain, and I_{DD} vs. V_{DD} at 16 GHz, R_{BIAS} = 768 Ω

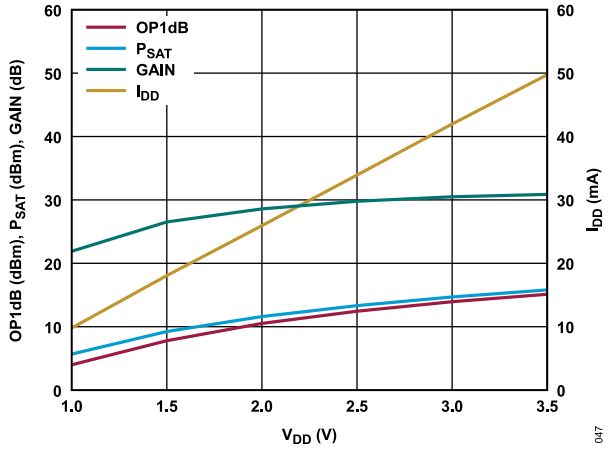

Figure 47. OP1dB, P_{SAT}, Gain, and I_{DD} vs. V_{DD} at 21 GHz, R_{BIAS} = 768 Ω

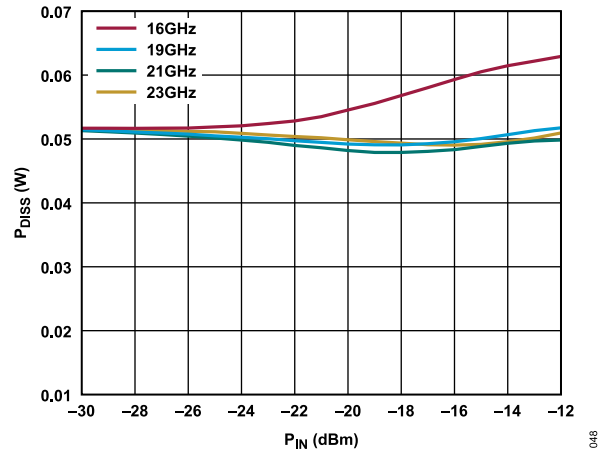

Figure 48. P_{DISS} vs. P_{IN} at Various Frequencies at 85°C, V_{DD} = 2 V, I_{DQ} = 25 mA

TYPICAL PERFORMANCE CHARACTERISTICS

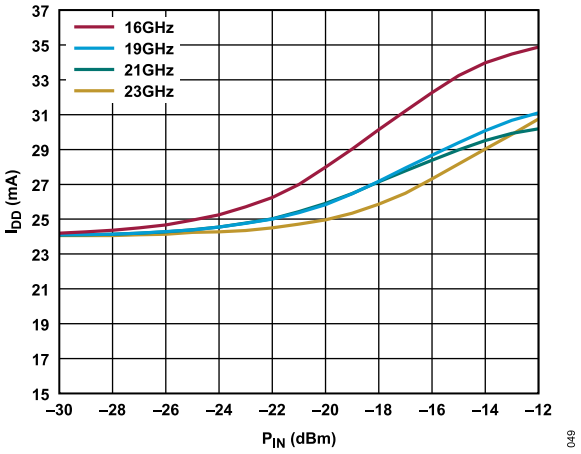

Figure 49. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 2 V

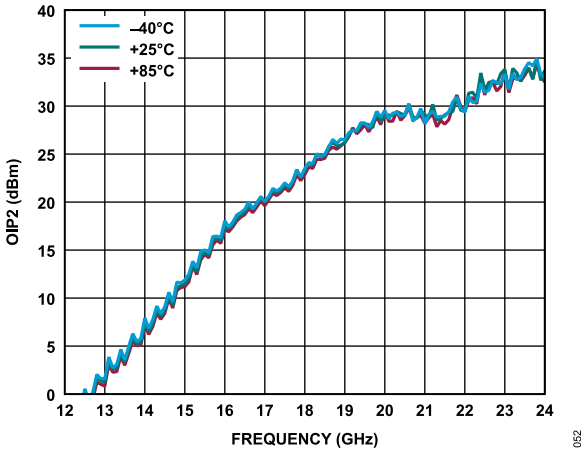

Figure 52. OIP2 vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

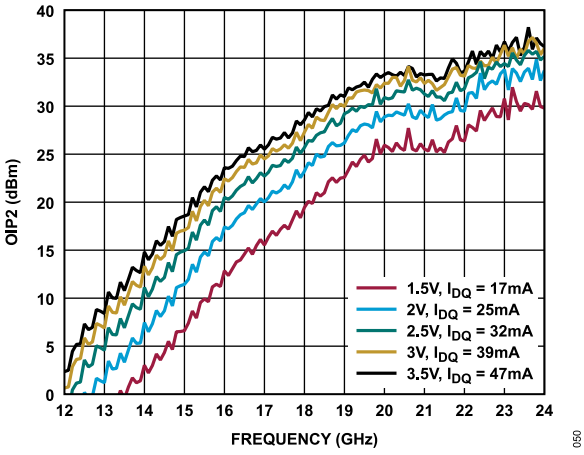

Figure 50. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 768 Ω

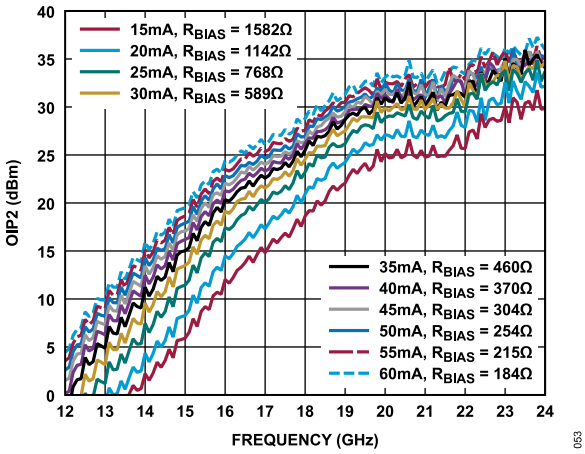

Figure 53. OIP2 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

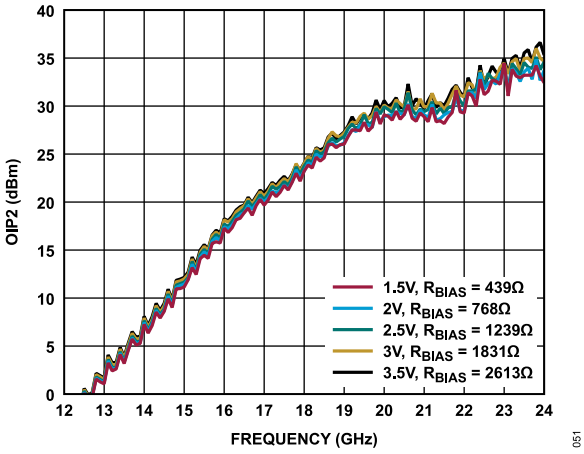

Figure 51. OIP2 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

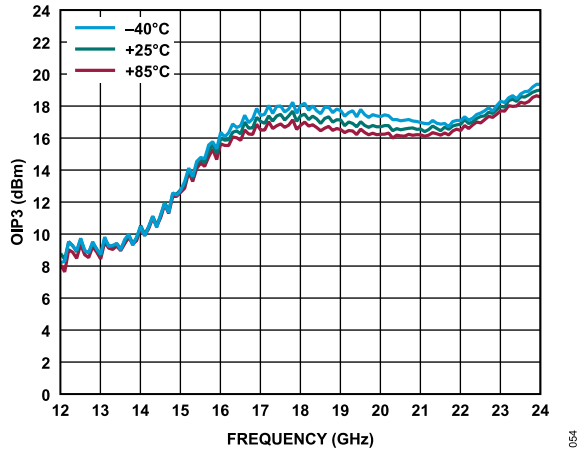

Figure 54. OIP3 vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

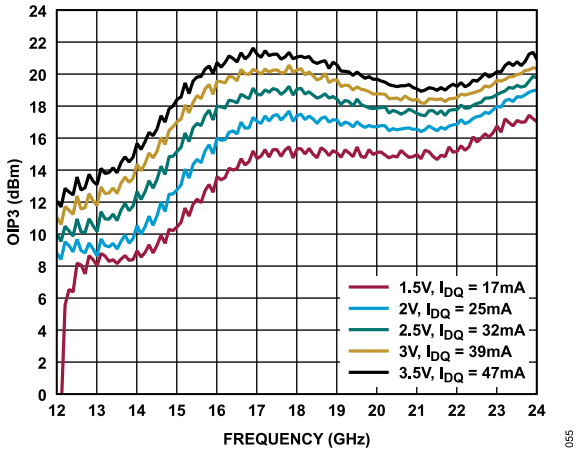

Figure 55. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

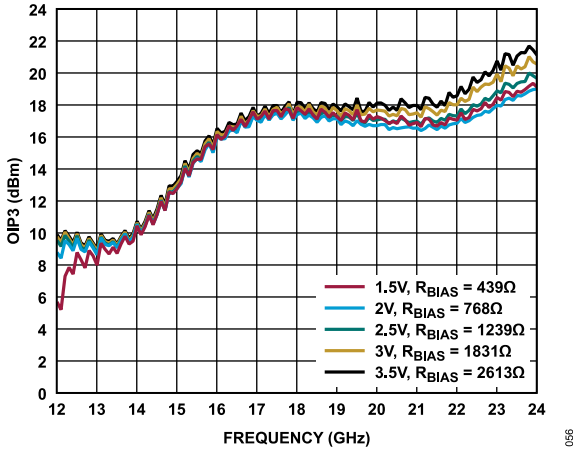

Figure 56. OIP3 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

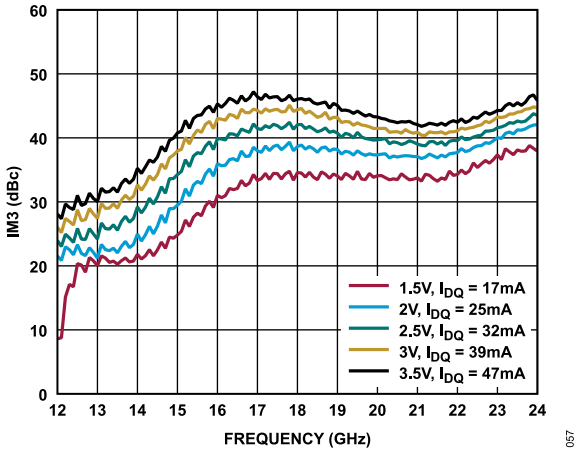

Figure 57. Third-Order Intermodulation (IM3) vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 768 Ω

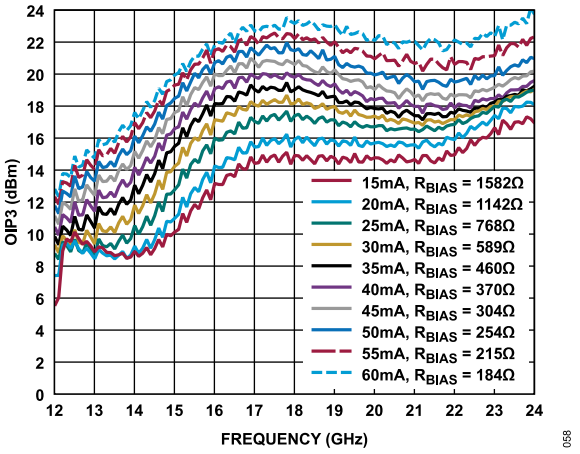

Figure 58. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

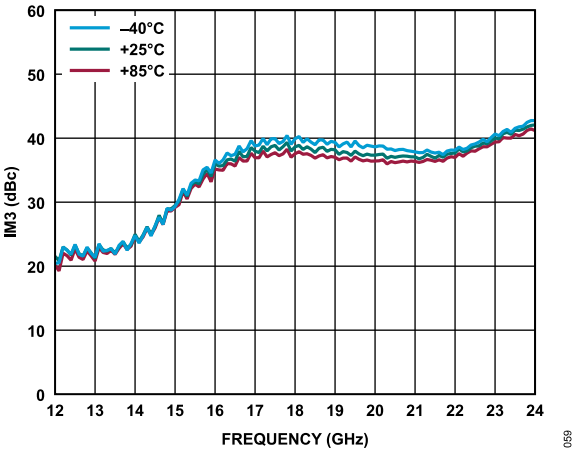

Figure 59. IM3 vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 768 Ω

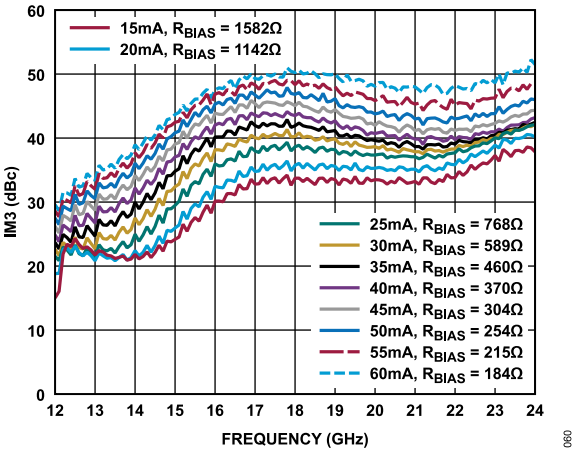

Figure 60. IM3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

TYPICAL PERFORMANCE CHARACTERISTICS

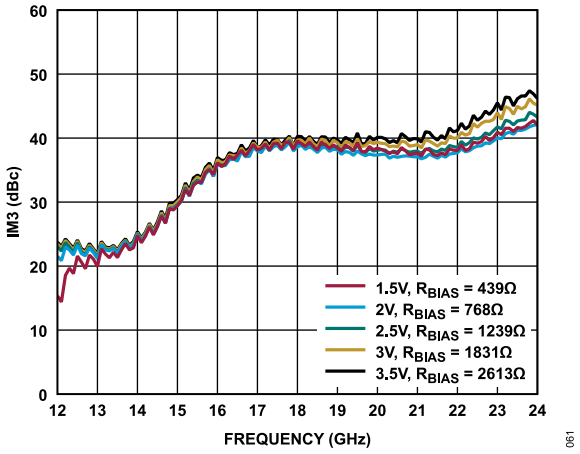

Figure 61. IM3 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

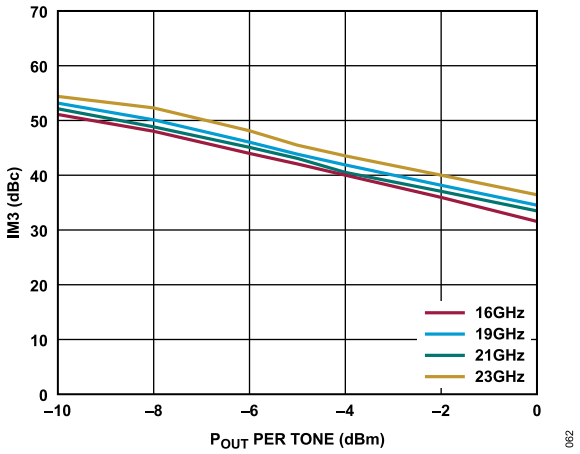

Figure 62. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2 V, R_{BIAS} = 768 Ω

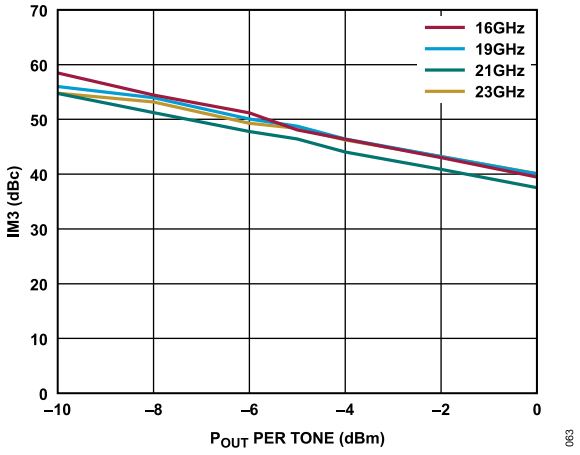

Figure 63. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, R_{BIAS} = 768 Ω

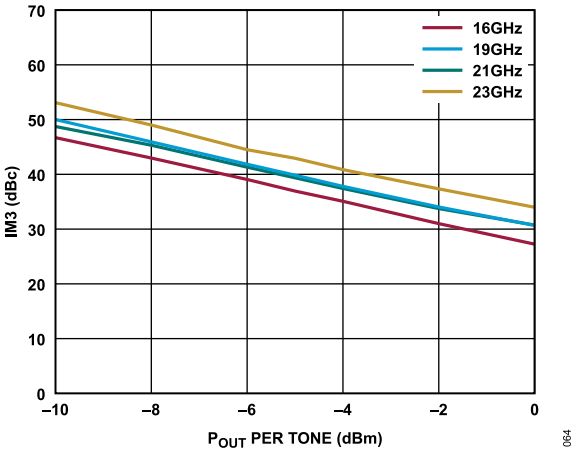

Figure 64. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 1.5 V, R_{BIAS} = 768 Ω

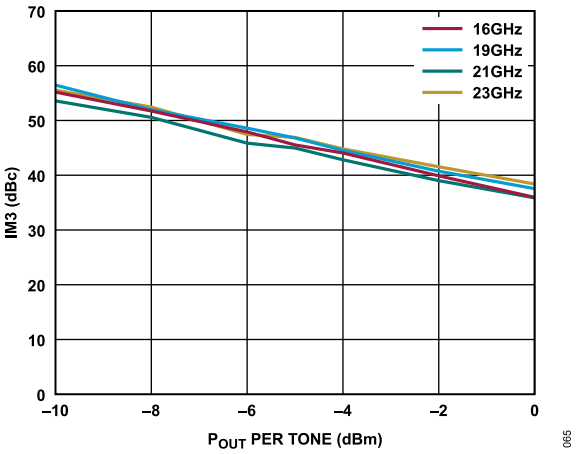

Figure 65. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2.5 V, R_{BIAS} = 768 Ω

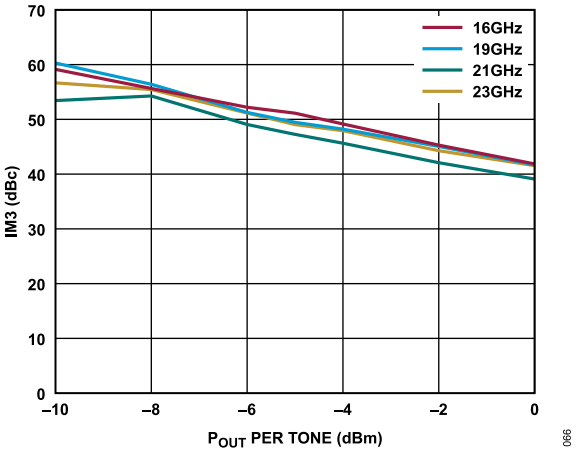

Figure 66. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.5 V, R_{BIAS} = 768 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

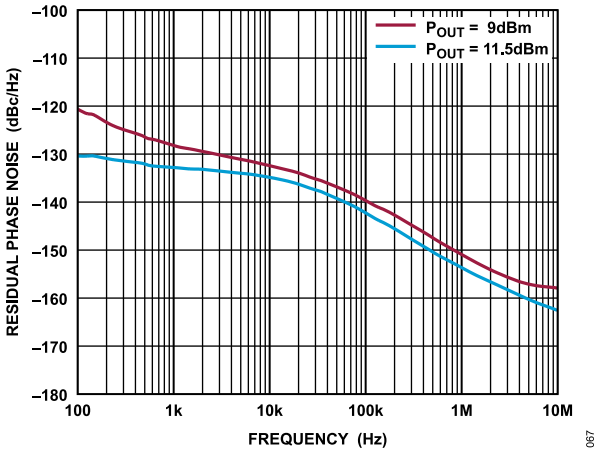

Figure 67. Residual Phase Noise vs. Frequency at 19 GHz for Various P_{OUT} Values

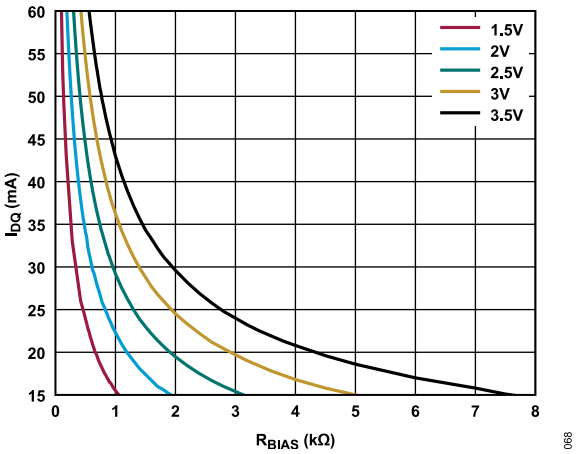

Figure 68. I_{DQ} vs. R_{BIAS} for Various Supply Voltages, R_{BIAS} Range = 0 Ω to 8.0 kΩ

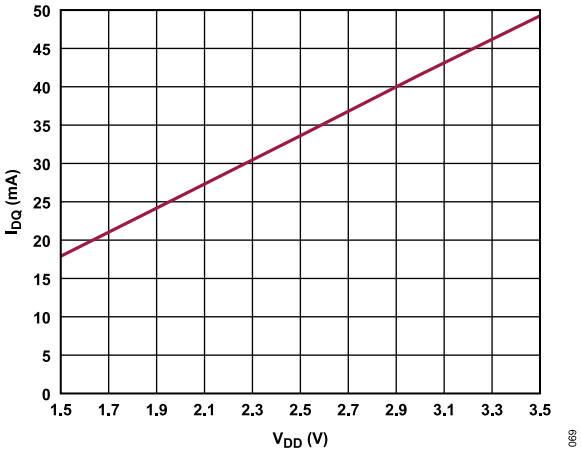

Figure 69. I_{DQ} vs. V_{DD}, R_{BIAS} = 768 Ω

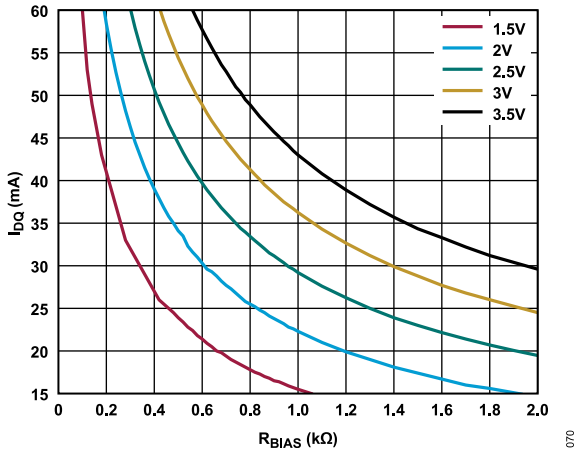

Figure 70. I_{DQ} vs. R_{BIAS} for Various Supply Voltages, R_{BIAS} Range = 0 Ω to 2.0 kΩ

THEORY OF OPERATION

The ADL8141 is a GaAs, MMIC, pHEMT, low noise wideband amplifier with an integrated bias inductor and AC-coupling capacitors. A simplified schematic is shown in Figure 71.

To set the drain bias current, connect an external resistor between the RBIAS and VDD pins.

The ADL8141 has AC-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 14 GHz to 24 GHz frequency range. No external matching components are required. While the RF output path is AC-coupled, there is a DC path to ground on the RFOUT side of the AC-coupling capacitor.

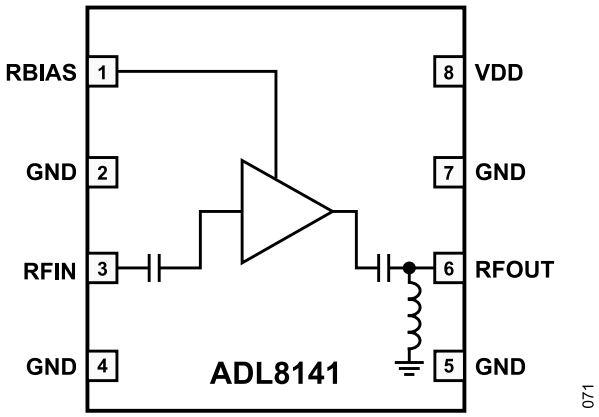

Figure 71. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8141 over the specified frequency range are shown in Figure 72. No external biasing inductor is required, allowing the 2 V supply to be connected to the VDD pin. Power supply decoupling capacitors of 0.1 µF and 100 pF are recommended. The power supply decoupling capacitors shown in Figure 72 represent the configuration used to characterize and qualify the ADL8141.

To set the I_{DQ}, connect a resistor, R2, between the RBIAS and VDD pins. A default value of 768 Ω is recommended, which results in a nominal I_{DQ} of 25 mA. The RBIAS pin also draws a current that varies with the value of R_{BIAS}, and this current is typically a few mA. Do not leave the RBIAS pin open.

The RFIN and RFOUT pins are internally AC-coupled. If the RFOUT pin is connected to a DC bias level other than 0 V, AC-couple the RFOUT pin because of the internal DC path to ground on RFOUT.

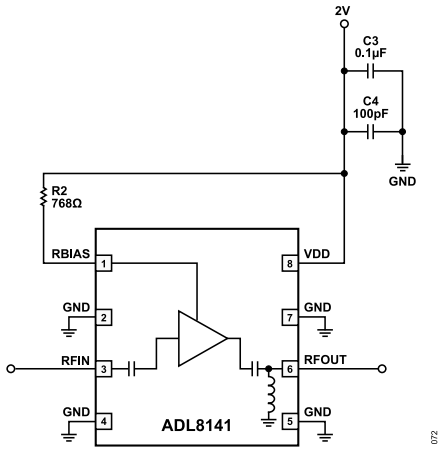

Figure 72. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

See the ADL8141-EVALZ user guide for the recommended bias sequencing information.

Table 9. Recommended Bias Resistor Values for V_{DD} = 2 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
1582	15	14	1
1142	20	18.7	1.3
768	25	23	2
589	30	27.7	2.3
460	35	32.1	2.9
370	40	36.5	3.49
304	45	40.9	4.07
254	50	45.39	4.67
215	55	49.79	5.27
184	60	54.17	5.86

USING RBIAS AS A FAST ENABLE AND DISABLE FUNCTION

The RBIAS pin can be used as a fast enable and disable control input. In the schematic in Figure 73, an SPDT switch is used to switch the voltage on the RBIAS resistor between 0 V and 2.5 V. When the voltage on the RBIAS pin is equal to 0 V, I_{DQ} reduces to less than 1 mA with P_{IN} set to −20 dBm. The response time of this circuit is shown in Figure 74.

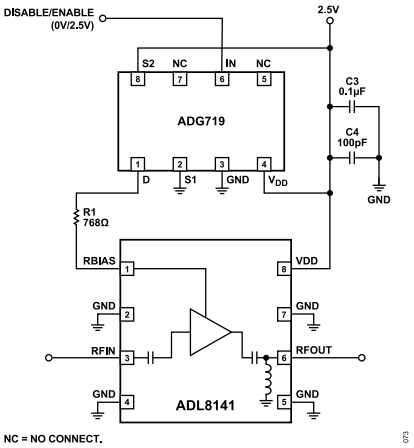

Figure 73. Fast Enable and Disable Using a 0 V to 2.5 V Pulse on the RBIAS Resistor

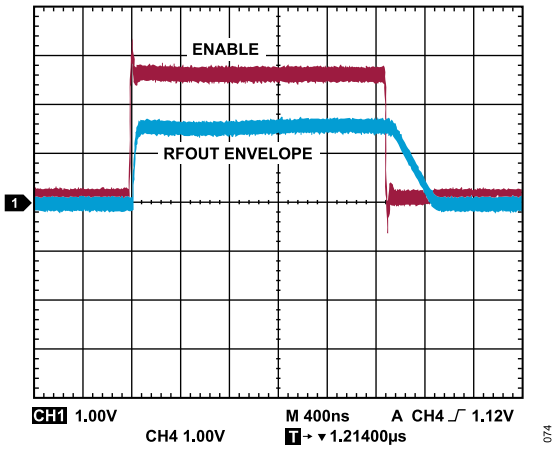

Figure 74. On and/or Off Response of the RFOUT Envelope When the IN Pin of the ADG719 Is Pulsed, P_{OUT} = 6 dBm at 19 GHz

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 75 shows a recommended power management circuit that uses the LT3083 low dropout (LDO) regulator. With the IN and $V_{CONTROL}$ pins tied together, the minimum input voltage (V_{IN}) is 3.6 V when an output voltage (V_{OUT}) of 2 V is required along with a current draw of up to 3 A. Assuming that the ADL8141 is used in a large array, a single LT3083 can easily provide power to the low noise amplifier in a 64-element array.

Table 10 provides recommended resistor values to set the other V_{DD} voltages. In each case, the minimum external supply is the minimum dropout voltage from the $V_{CONTROL}$ input to V_{OUT}.

Table 10. Recommended Resistor Values for the Various LDO Output Voltages

LDO V_{OUT} (V)	R2 (kΩ)	Minimum V_{DD} (V)
1.5	30.1	3.1
2	40.2	3.6
2.5	49.9	4.1
3.3	66.5	4.9
4	80.6	5.6

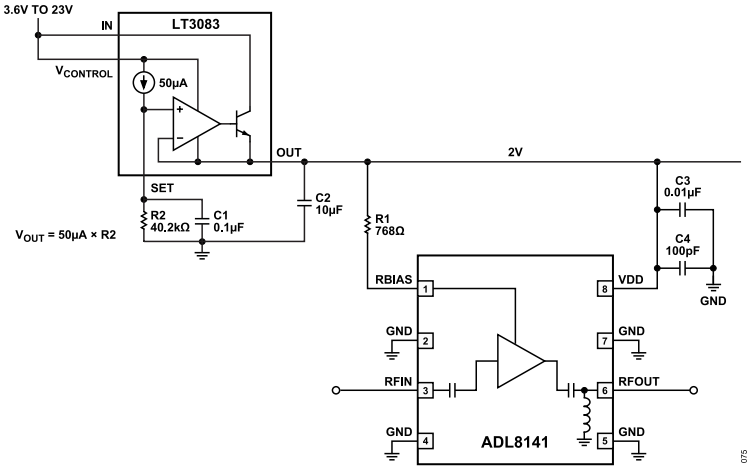

Figure 75. Recommended Power Management Circuit

OUTLINE DIMENSIONS

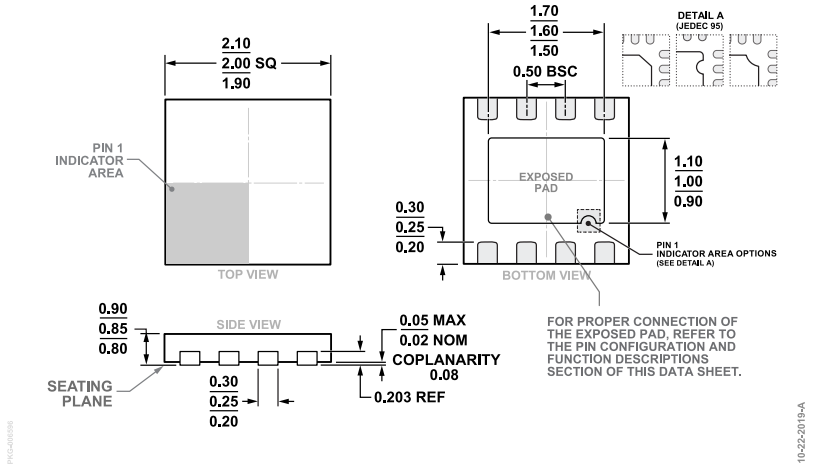

Figure 76. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

Updated: June 21, 2023

ORDERING GUIDE

Model[1,2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8141ACPZN	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 500	CP-8-30
ADL8141ACPZN-R7	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 500	CP-8-30

[1] Z = RoHS Compliant Part.

[2] The lead finish of ADL8141ACPZN and ADL8141ACPZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model[1]	Description
ADL8141-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.