

DI CMOS Protected Analog Switches

AD7510DI/AD7511DI/AD7512DI

FEATURES

Latch-Proof

Overvoltage-Proof: ±25V

Low R_{ON}: 75Ω

Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Manalithia Dialectrically, lea

Monolithic Dielectrically-Isolated CMOS

Standard 14-/16-Pin DIPs and

20-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25 \text{V}$ above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75 Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

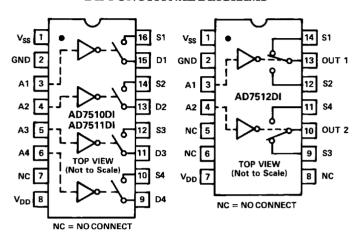
CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH" AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to

Out 2

DIP FUNCTIONAL DIAGRAMS



ORDERING GUIDE

Model ¹	Temperature Range	Package Option ²
AD7510DIKN	0 to +70°C	N-16
AD7510DIKP	0 to +70°C	P-20A
AD7510DIKQ	-25°C to +85°C	Q-16
AD7510DISQ	-55°C to +125°C	Q-16
AD7510DISE	-55°C to +125°C	E-20A
AD7511DIKN	0 to +70°C	N-16
AD7511DIKP	0 to +70°C	P-20A
AD7511DIKQ	-25°C to +85°C	Q-16
AD7511DISQ	-55°C to +125°C	Q-16
AD7511DITE	-55°C to +125°C	E-20A
AD7512DIKN	0 to +70°C	N-14
AD7512DIKP	0 to +70°C	P-20A
AD7512DIKQ	-25°C to +85°C	Q-14
AD7512DITQ	-55°C to +125°C	Q-14
AD7512DITE	-55°C to +125°C	E-20A

NOTES

 $P = Plastic \ Leaded \ Chip \ Carrier \ (PLCC); Q = Cerdip.$

REV. A

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Telex: 924491 Cable: ANALOG NORWOODMASS

¹To order MIL-STD-883, Class B, processed parts, add/883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.

²E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP;

AD7510DI/AD7511DI/AD7512DI — SPECIFICATIONS

 $(V_{DD} = +15V, V_{SS} = -15V, unless otherwise noted.)$

INDUSTRIAL VERSION (K)					
PARAMETER	MODEL	VERSION	+25°C (N, P, Q)	0 to +70°C (N, P) -25°C to +85°C (Q)	TEST CONDITIONS
ANALOG SWITCH					
R _{ON} ¹	All	K	75Ω typ, 100Ω max	175 Ω max	$-10V \le V_D \le +10V$
R_{ON} vs V_D (V_S)	All	K	20% typ		l _{DS} = 1.0mA
R _{ON} Drift	All	K	+0.5%/°C typ		
R _{ON} Match	All	K	1% typ		$V_{D} = 0, I_{DS} = 1.0 \text{mA}$
R _{ON} Drift Match	All	K	0.01%/°C typ		D V DS
ID (IS)OFF1	All	К	0.5nA typ, 5nA max	500nA max	$V_D = -10V, V_S = +10V \text{ and } V_D = +10V, V_S = -10V$
I _D (I _S) _{ON} ¹	All	K	10nA max		$V_S = V_D = +10V$ $V_S = V_D = -10V$
LOUT 1	AD7512DI	K	15nA max	1500nA max	$V_{S1} = V_{OUT} = \pm 10V, V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V, V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}^{1}	All	K		0.8V max	
V_{INH}^{-1}	All			2.4V min	
C _{IN}	All	K	7pF typ		
I _{INH} 1	All	К	10nA max		$V_{IN} = V_{DD}$
I _{INL} 1	All	K	10nA max		$V_{IN} = 0$
DYNAMIC	,				
CHARACTERISTICS	A D 25 1 0 D I	v	100ms tun		
t _{ON}	AD7510DI AD7511DI	K K	180ns typ 350ns typ		
t	AD7511DI	K	350ns typ		$V_{IN} = 0 \text{ to } +3.0V$
toff	AD7511DI	K	180ns typ		
^t TRANSITION	AD7512DI	K	300ns typ		
C _S (C _D)OFF	All	K	8pF typ		
$C_S(C_D)ON$	All	K	17pF typ		
$C_{DS}(C_{S-OUT})$	All	K	1pF typ		$V_D(V_S) = 0V$
$C_{DD}(C_{SS})$	All	K	0.5pF typ		
COUT	AD7512DI	K	17pF typ		
Q _{INJ}	All	K	30pC typ		Measured at S or D terminal. $C_L = 1000 \text{pF}, V_{IN} = 0 \text{ to } 3V,$ $V_D (V_S) = +10V \text{ to } -10V$
POWER SUPPLY					
$l_{\mathbf{DD}}^{-1}$	All	K	800μA max	800μA max	All digital inputs = V _{INH}
L _{SS} 1	All	K	800μA max	800μA max	
I _{DD} 1	All	K	500μA max	500μA max	All digital inputs = V _{INL}
rss r	All	K	500μA max	500μA max	

PIN CONFIGURATIONS **PLCC PLCC** LCCC LCCC NC SI OUT 1 GND VSS NC S1 2 1 20 19 3 2 1 20 19 3 2 1 20 19 3 2 1 20 19 ٥ 18 S2 17 NC 16 S4 15 NC 14 OUT 2 18 S2 17 D2 16 NC 15 S3 14 D3 A1 4 A1 4 18 S2 A1 18 S2 A1 4 AD7510DI AD7511DI TOP VIEW (NOT TO SCALE) NC 5 A2 5 AD7512DI 17 NC AD7510DI AD7511DI TOP VIEW NC 5 A2 5 17 D2 A2 6 NC 7 NC 6 A3 7 AD7512DI TOP VIEW (Not to Scale) A2 6 16 S4 16 NC NC 6 TOP VIEW A3 7 15 83 NC 7 15 NC NC 8 A4 8 14 OUT 2 A4 8 14 D3 9 10 11 12 13 9 10 11 12 13 10 11 12 10 11 12 13 13 S D A S N 00 N 40 8 S N N S NC = NO CONNECT NC = NO CONNECT NC = NO CONNECT NC = NO CONNECT

NOTES
1100% tested.

Specifications subject to change without notice.

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH	All	S, T	100Ω max	175Ω max	$-10V \le V_{D} \le +10V$ $I_{DS} = 1 \text{mA}$
I _D (I _S) _{OFF} ¹	All	S, T	3nA max	200nA max	$V_D = -10V, V_S = +10V \text{ and}$ $V_D = +10V, V_S = -10V$
I _D (I _S)ON ¹	All	S, T	10		$V_S = V_D = +10V$ and $V_S = V_D = -10V$
I _{OUT} ¹	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V \text{ and}$ $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL V _{INL} ¹	All	S, T		0.8V max	
V _{INH} 1,2	AD7510DI AD7511DI AD7512DI AD7511DI AD7512DI	T T	* ***	2.4V min 2.4V min 2.4V min 3.0V min 3.0V min	
I _{INH} I _{INL}	All All	S, T S, T	10nA max 10nA max	7.5 V IIIII	$V_{IN} = V_{DD}$ $V_{IN} = 0$
OYNAMIC CHARACTERISTICS					
t _{ON} ³	AD7510DI AD7511DI AD7510DI	S, S, T S, T	1.0µs max 1.0µs max 1.0µs max		$V_{IN} = 0 \text{ to } +3V$
^t TRANSITION ³	AD7511DI AD7512DI	S, T S, T	1.0µs max 1.0µs max	• • • • • • • • • • • • • • • • • • •	
POWER SUPPLY IDD ISS	All All	S, T S, T		800μA max 800μA max	All digital inputs = V _{INH}
I _{DD} 1 I _{SS}	All All	S, T S, T		500μA max 500μA max	All digital inputs = V _{INL}

NOTES

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND				
V_{SS} to GND				
Overvoltage at $V_D(V_S)$				
(1 second surge) V_{DD} +25V				
or $V_{SS} - 25V$				
(Continuous) $V_{DD} + 20V$				
or $V_{SS} - 20V$				
or 20mA, Whichever Occurs First				
Switch Current (I _{DS} , Continuous) 50mA				
Switch Current (I _{DS} , Surge)				
1ms Duration, 10% Duty Cycle 150mA				
Digital Input Voltage Range 0V to V _{DD} +0.3V				
Power Dissipation (Any Package)				
Up to +75°C				
Derates above +75°C by 6mW/°C				

Lead Temperature (Soldering, 10sec) +3	300°C
Storage Temperature $\dots \dots -65^{\circ}C$ to $+1$	150°C
Operating Temperature	
Commercial (KN, KP Versions) 0 to +	70°C
Industrial (KQ Versions)25°C to +	85°C
Extended (SQ, TQ, SE, TE Versions)55°C to +1	125℃

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



^{1100%} tested.

²A pullup resistor, typically 1-2k Ω is required to make AD7511DISQ and AD7512DISQ TTL compatible.

Guaranteed, not production tested.

Specifications subject to change without notice.

AD7510DI/AD7511DI/AD7512DI — Circuit Description

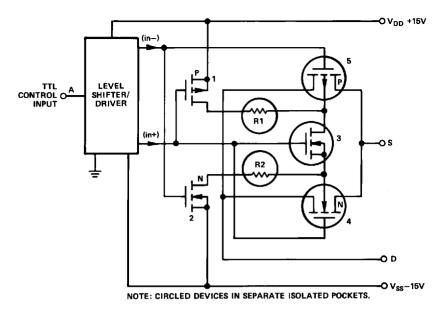


Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CIRCUIT DESCRIPTION

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as $R_{\rm ON}$ or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is $V_{\rm DD}$ and (in-) is $V_{\rm SS}$ from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 in "ON". Hence, the backgates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. The circled devices are located in separate dielectrically isolated pockets. Floating the output switch backgates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter $R_{\rm ON}$ versus $V_{\rm S}$ response.

For an "OFF" switch, device number 3 is "OFF," and the backgates of devices 4 and 5 are tied through $1k\Omega$ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D (OUT) terminal which exceeds $V_{\rm DD}$ or $V_{\rm SS}$, the S- or D-to-backgate diode is forward biased; however, R1 and R2 provide current limiting action to the supplies.

An equivalent circuit of the output switch element in Figure 3 shows that, indeed, the $1k\Omega$ limiting resistors are in series with the backgates of the P- and N-channel output devices – not in series with the signal path between the S and D terminals.

It is possible to turn on an "OFF" switch by applying a voltage in excess of $V_{\rm DD}$ or $V_{\rm SS}$ to the S or D terminal. If a positive stress voltage is applied to the S or D terminal which exceeds $V_{\rm DD}$ by a threshold, then the P-channel (device 5) will turn on creating a low impedance path between the S and D terminals. A similar situation exists for negative stress voltages which exceed $V_{\rm SS}$. In this case the N-channel provides the low impedance path between the S and D terminals. The limiting factor on the overvoltage protection is the power dissipation of the package and is $\pm\,20V$ continuous (or 20mA whichever occurs first) above the supply voltages.

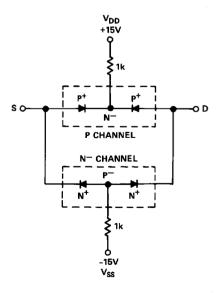
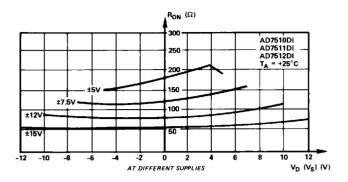
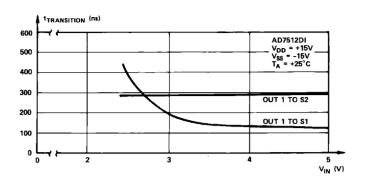


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

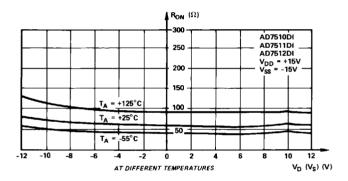
Typical Performance Characteristics—AD7510DI/AD7511DI/AD7512DI



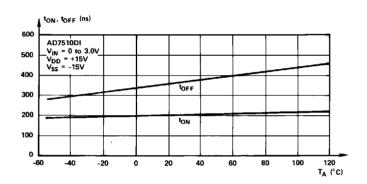
 R_{ON} as a Function of V_D (V_S)



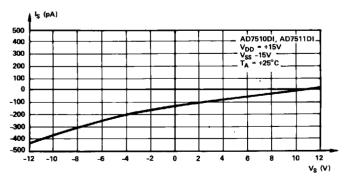
tTRANSITION as a Function of Digital Input Voltage



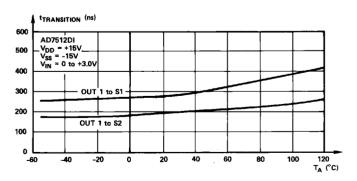
RON as a Function of VD (VS)



 t_{ON} , t_{OFF} as a Function of Temperature



Is, (ID)OFF VS VS

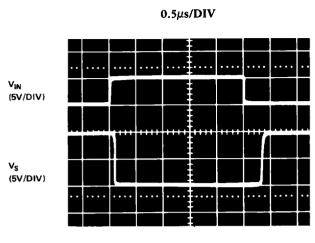


tTRANSITION as a Function of Temperature

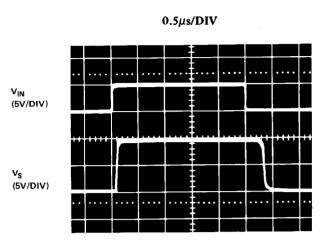
AD7510DI/AD7511DI/AD7512DI

TYPICAL SWITCHING CHARACTERISTICS

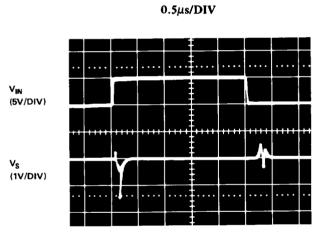
AD7510DI, AD7511DI



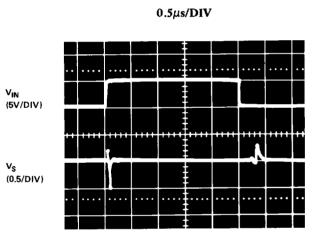
Switching Waveforms for $V_D = -10V$



Switching Waveforms for $V_D = +10V$

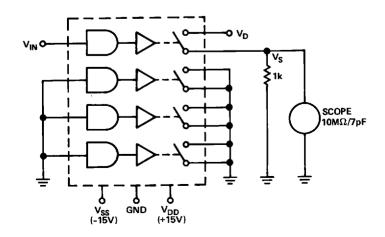


Switching Waveforms for V_D = Open



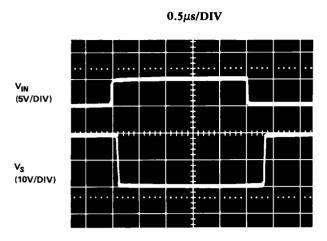
Switching Waveforms for $V_D = 0V$

AD7510DI, AD7511DI TEST CIRCUIT



AD7510DI/AD7511DI/AD7512DI

AD7512DI

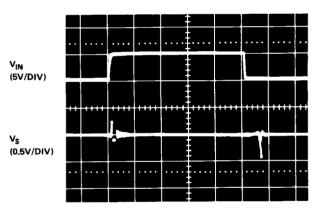


Switching Waveforms for $V_{S1} = -10V$, $V_{S2} = +10V$, $R_L = 1k$

0.5μs/DIV

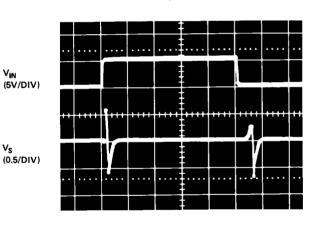
Switching Waveforms for $V_{S1} = +10V$, $V_{S2} = -10V$, $R_L = \infty$





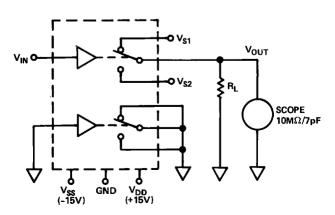
Switching Waveforms for V_{S1} and $V_{S2} = 0V$, $R_L = \infty$

$0.5\mu s/DIV$



Switching Waveforms for V_{S1} and V_{S2} = Open, R_L = 1k

AD7512DI TEST CIRCUIT



AD7510DI/AD7511DI/AD7512DI

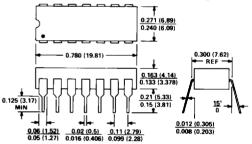
TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S.	$C_{\mathbf{DD}}(C_{SS})$	Capacitance between terminals D(S) of any	
R _{ON} Drift Match	Difference between the R_{ON} drift of any two switches.		two switches. (This will determine the cross coupling between switches vs. frequency.)	
R _{ON} Match	Difference between the R _{ON} of any two switches.	t _{ON}	Delay time between the 50% points of the digital input and switch "ON" condition.	
$I_D(I_S)_{OFF}$	Current at terminals D or S. This is a leakage current when the switch is "OFF".	t _{OFF}	Delay time between the 50% points of the digital input and switch "OFF" condition.	
$I_D(I_S)_{ON}$	Leakage current that flows from the closed switch into the body. (This leakage will	t _{TRANSITION}	Delay time when switching from one address state to another.	
	show up as the difference between the	V_{INL}	Maximum input voltage for a logic low.	
	current I_D going into the switch and the outgoing current I_S .)	V_{INH}	Minimum input voltage for a logic high.	
		$I_{\rm INL}(I_{\rm INH})$	Input current of the digital input.	
$V_D(V_S)$	Analog voltage on terminal $D(S)$.	C_{IN}	Input capacitance to ground of the digital	
$C_S(C_D)$	Capacitance between terminal S(D) and ground. (This capacitance is specified for the switch open and closed.)		input.	
		V_{DD}	Most positive voltage supply.	
C_{DS}	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)	V_{SS}	Most negative voltage supply.	
		I_{DD}	Positive supply current.	
		I_{SS}	Negative supply current.	

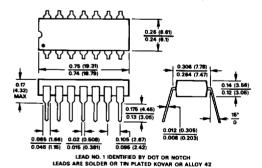
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

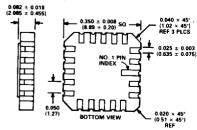
14-Pin Cerdip Package (Suffix Q)



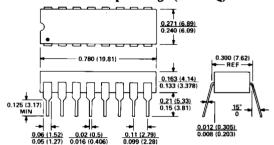
14-Pin Plastic DIP (Suffix N)



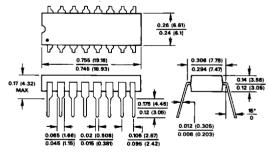
20-Terminal Leadless Ceramic Chip Carrier (Suffix E)



16-Pin Cerdip Package (Suffix Q)



16-Pin Plastic DIP (Suffix N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

20-Terminal Plastic Leaded Chip Carrier (Suffix P)

