

# Low $V_{IN}$ , Quad 8A Silent Switcher $\mu$ Module Regulator

## FEATURES

- Quad Output Step-Down  $\mu$ Module<sup>®</sup> Regulator with Configurable 8A Output Array
- Ultralow Noise Silent Switcher<sup>®</sup>2 Architecture
- CISPR32 Class B Compliant
- Input Voltage Range: 2.5V to 5.5V
- Output Voltage Range: 0.5V to 3.6V
- 8A DC Output Current, Each Channel
- Parallelable for Higher Output Current
- $\pm 1.5\%$  Maximum Total DC Output Voltage Accuracy
- Selectable Switching Frequency: 1MHz to 5MHz
- Power Good Indicator
- Die Temperature Monitoring
- 6mm  $\times$  12mm  $\times$  3.54mm Land Grid Array (LGA) with Presolder Package

## APPLICATIONS

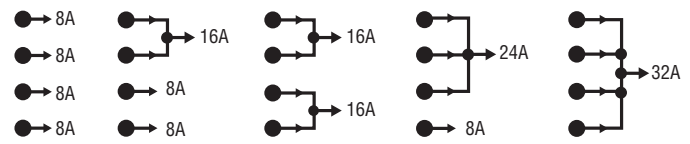
- Optical Communications
- Multi-Rail Point-of-Load Regulation
- Field Programmable Gate Arrays (FPGAs), Digital signal processing (DSPs) and Application Specific Integrated Circuits (ASICs) Applications
- Telecom, Datacom, Networking System

## DESCRIPTION

The LTM<sup>®</sup>4710-1 is a quad DC/DC step-down  $\mu$ Module (micromodule) regulator with 8A per output. The package includes the switching controllers, the power MOSFETs, inductors and all supported components. Operating over an input voltage range of 2.5V to 5.5V. Channel 1's output voltage can be set by only one external resistor, where the outputs for channel 2, channel 3, and channel 4 can be set by two external resistors. All output voltages are programmable up to 3.6V.

The LTM4710-1 employs Silent Switcher 2 architecture with internal hot loop bypass capacitors to achieve both low Electromagnetic Interference (EMI) and high efficiency. The LTM4710-1 is packaged in a compact (6mm  $\times$  12mm  $\times$  3.54mm) LGA with presolder package and is RoHS compliant.

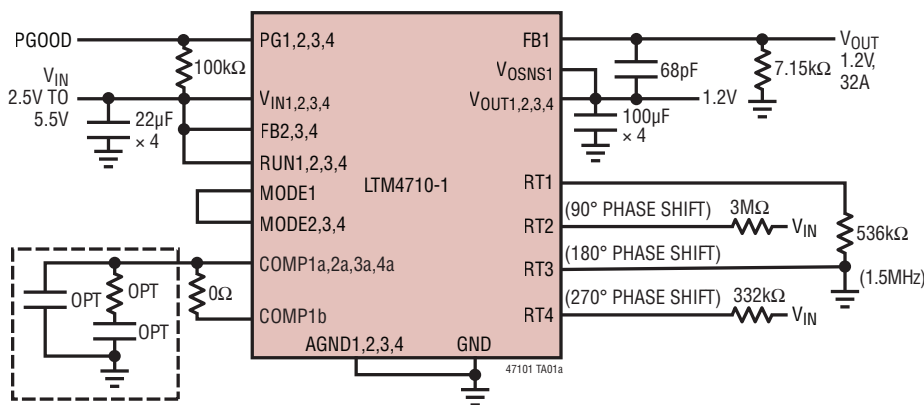
### Configurable Output Array



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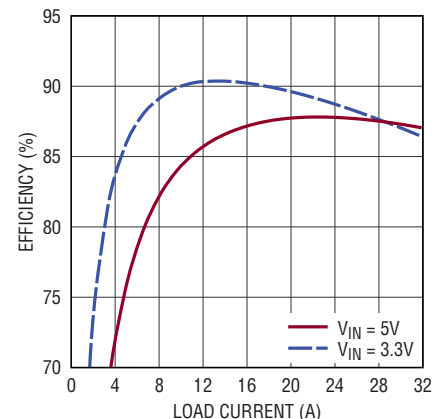
## TYPICAL APPLICATION

Paralleled Single Output, 32A DC/DC  $\mu$ Module Regulator



PINS NOT SHOWN IN THIS CIRCUIT: SSTT, SW

Efficiency at 1.2V<sub>OUT</sub>



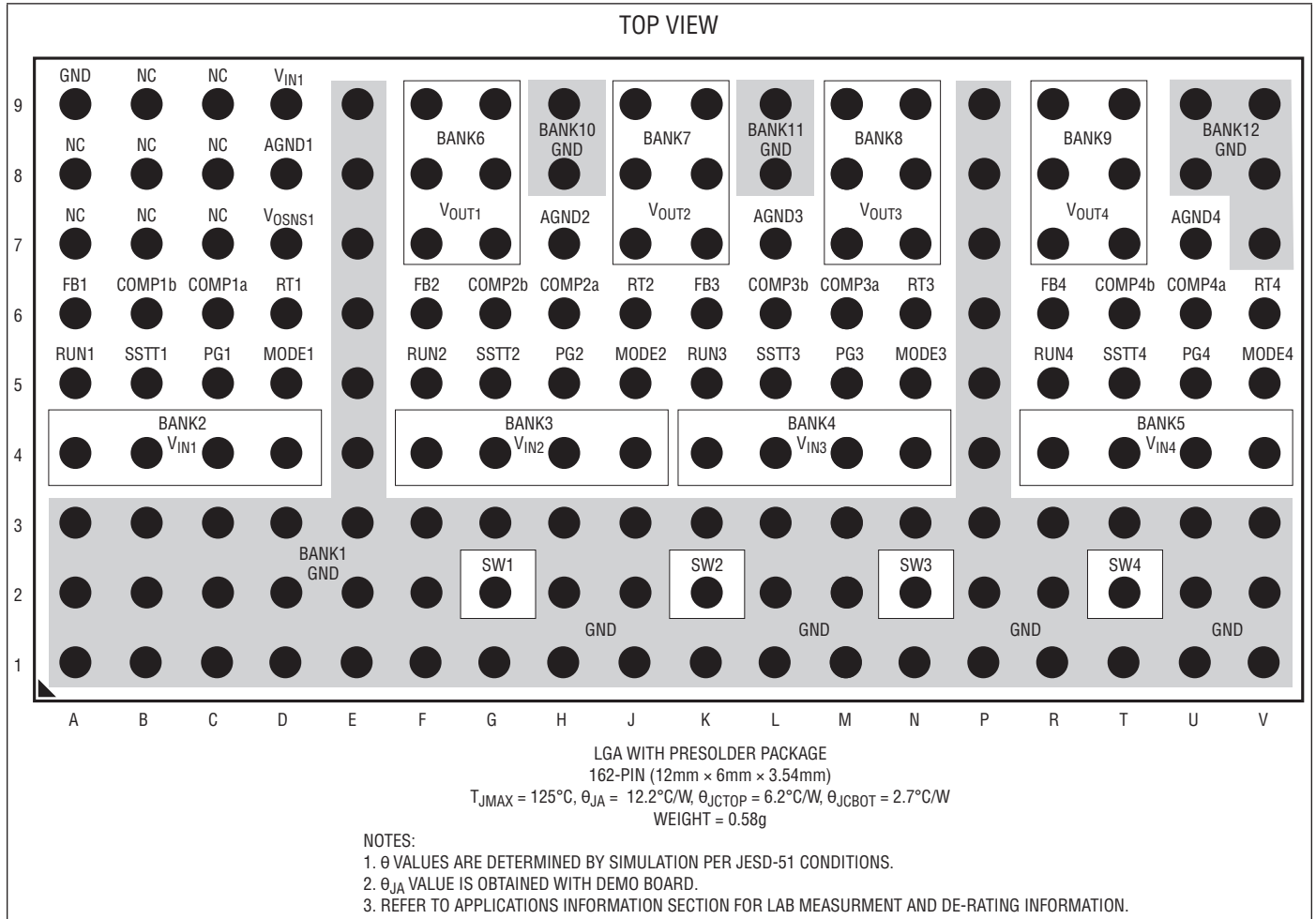
47101 TA01b

# LTM4710-1

## ABSOLUTE MAXIMUM RATINGS (Note 1)

All Pins Except GND and AGND<sub>n</sub> ..... -0.3V to 6V      Storage Temperature Range ..... -55°C to 125°C  
 Operating Junction Temperature (Note 2) ..... -40°C to 125°C      Peak Solder Reflow Body Temperature ..... 250°C

## PIN CONFIGURATION (See Pin Functions, Package Pinout Description table)



## ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4710EV-1#PBF	SAC305 (RoHS)	4710-1	e1	LGA with Presolder	4	-40°C to 125°C
LTM4710IV-1#PBF	SAC305 (RoHS)	4710-1	e1	LGA with Presolder	4	-40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over specified internal operating junction temperature range (Note 2), otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 3.3\text{V}$ , per the typical application.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input DC Voltage		● 2.5		5.5	V
$V_{OUT(RANGE)}$	Output Voltage Range		● 0.5		3.6	V
$V_{IN\_UVLO}$	$V_{IN}$ Undervoltage Lockout	$V_{IN}$ Rising	2.0	2.1	2.2	V
$V_{IN\_UVLO\_HYS}$	$V_{IN}$ Undervoltage Lockout Hysteresis			150		mV
$V_{RUN}$	RUN Pin On-Threshold	$V_{RUN}$ Rising	0.375	0.4	0.425	V
$V_{RUN\_HYS}$	RUN Pin Hysteresis			75		mV
$I_{RUN}$	RUN Pin Leakage Current	$RUN = 0.4\text{V}$			$\pm 20$	nA
$I_{Q(VIN)}$	Input Supply Current	$V_{OUT} = 0.5\text{V}$ , $MODE = \text{FLOAT}$ , $FCM$ Shutdown, $RUN = 0\text{V}$ (Note 5)		50 2		mA $\mu\text{A}$
$I_{OUT(DC)}$	Output Continuous Current Range	$V_{OUT} = 0.5\text{V}$ (Note 3)			8	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	$V_{OUT} = 0.5\text{V}$ , $V_{IN} = 2.5\text{V}$ to $5.5\text{V}$ , $I_{OUT} = 0\text{A}$			0.2	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	$V_{OUT} = 0.5\text{V}$ , $I_{OUT} = 0\text{A}$ to $8\text{A}$	●	0.5	1.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	$I_{OUT} = 0\text{A}$ , $V_{OUT} = 0.5\text{V}$		12		mV
$I_{SST}$	Track Pin Soft-Start Pull-Up Current	$V_{SST} = 0.5\text{V}$	7	10	13	$\mu\text{A}$
$V_{FB}$	Voltage at $V_{FB}$ Pin		● 0.495	0.50	0.505	V
$I_{FB}$	Current at $V_{FB}$ Pin	(Note 4)			$\pm 20$	nA
$t_{ON(MIN)}$	Minimum On-Time			40		ns
$V_{PG}$	Power Good Rising Threshold Power Good Overvoltage Threshold	$V_{FB}$ as a Percentage of Regulated $V_{OUT}$ $V_{FB}$ as a Percentage of Regulated $V_{OUT}$		98 110		% %
$I_{PG}$	Power Good Leakage	$V_{PG} = 5.5\text{V}$			50	nA
$f_{OSC}$	Oscillator Frequency Range		1		5	MHz
SYNC_RANGE	Synchronization Frequency Range	$R_T = V_{IN}$	1.2		2.6	MHz
SYNC_LEVEL Input	Clock Level High Clock Level Low	$R_T = V_{IN}$	1.2		0.4	V V

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4710-1 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTM4710E-1 is guaranteed to meet performance specifications over the  $0^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Specifications over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4710I-1 is guaranteed to meet

specifications over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

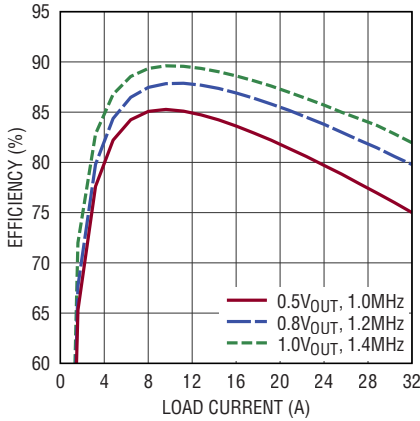
**Note 3:** See output current thermal derating curves for different  $V_{IN}$ ,  $V_{OUT}$  and  $T_A$ .

**Note 4:** Wafer sort tested.

**Note 5:** Guaranteed by design.

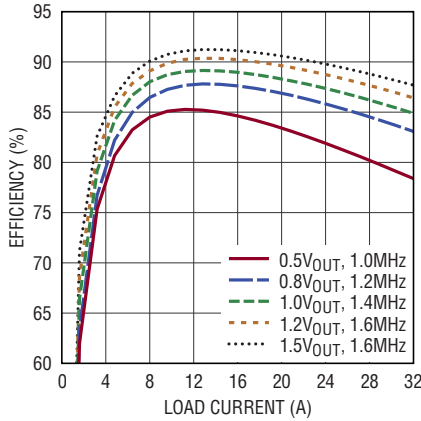
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Efficiency, 4-Channel Paralleled**  
 $V_{IN} = 2.5\text{V}$



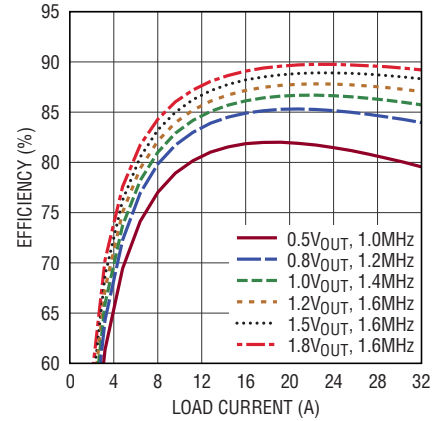
47101 G01

**Efficiency, 4-Channel Paralleled**  
 $V_{IN} = 3.3\text{V}$



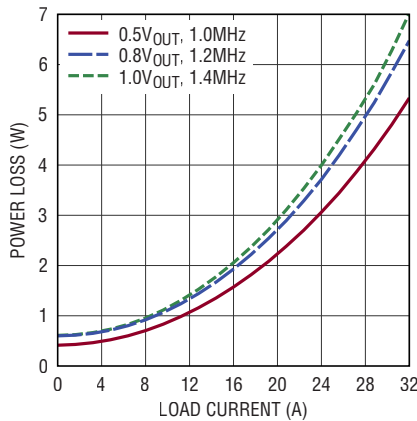
47101 G02

**Efficiency, 4-Channel Paralleled**  
 $V_{IN} = 5.5\text{V}$



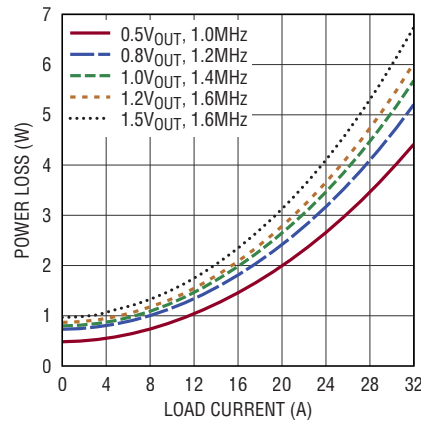
47101 G03

**Power Loss, 4-Channel Paralleled**  
 $V_{IN} = 2.5\text{V}$



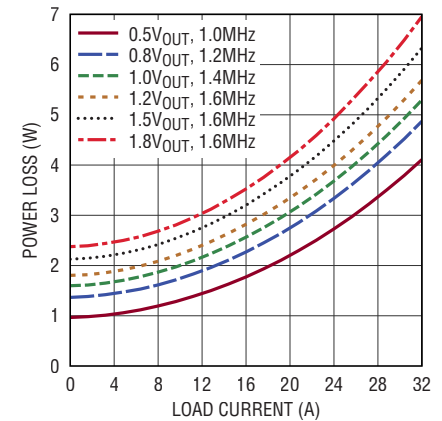
47101 G04

**Power Loss, 4-Channel Paralleled**  
 $V_{IN} = 3.3\text{V}$



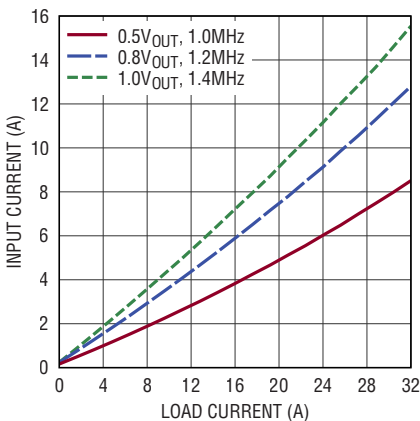
47101 G05

**Power Loss, 4-Channel Paralleled**  
 $V_{IN} = 5.5\text{V}$



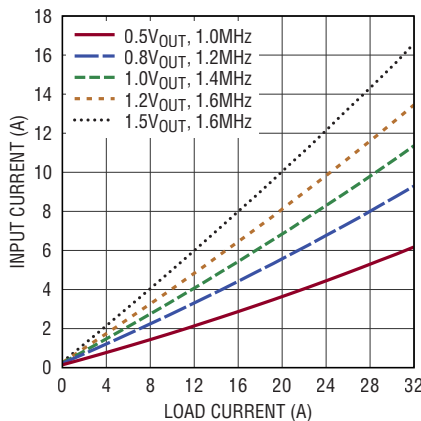
47101 G06

**Input vs Load Current**  
 $V_{IN} = 2.5\text{V}$ , 4-Channel Paralleled



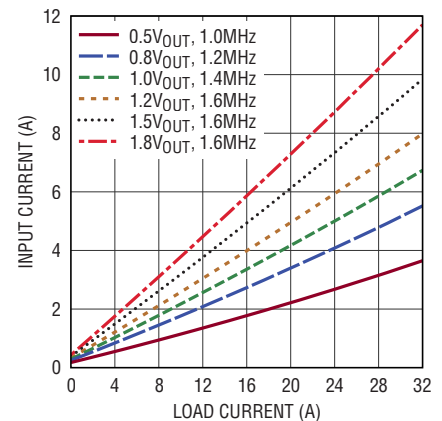
47101 G07

**Input vs Load Current**  
 $V_{IN} = 3.3\text{V}$ , 4-Channel Paralleled



47101 G08

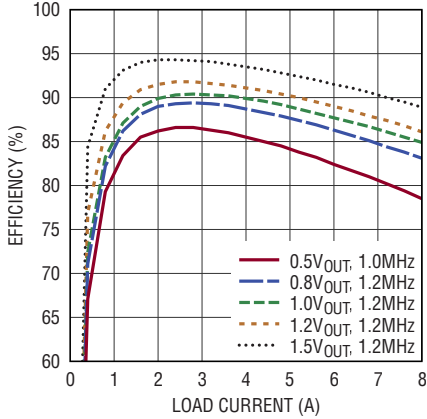
**Input vs Load Current**  
 $V_{IN} = 5.5\text{V}$ , 4-Channel Paralleled



47101 G09

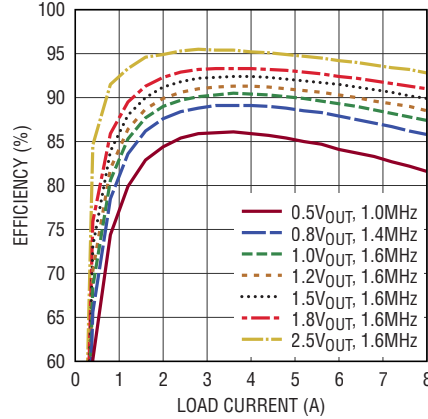
**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Efficiency, Single Channel**  
 $V_{IN} = 2.5\text{V}$



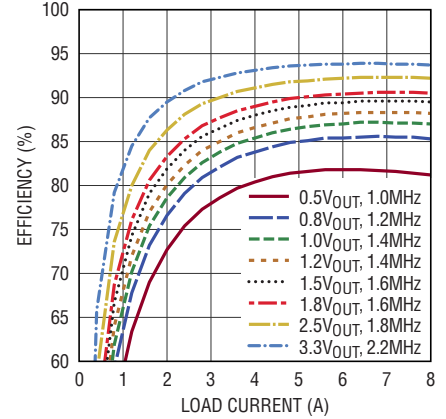
47101 G10

**Efficiency, Single Channel**  
 $V_{IN} = 3.3\text{V}$



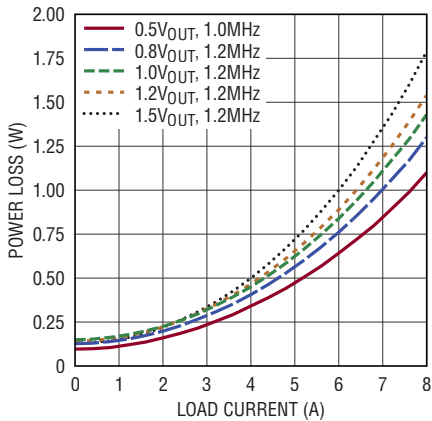
47101 G11

**Efficiency, Single Channel**  
 $V_{IN} = 5.5\text{V}$



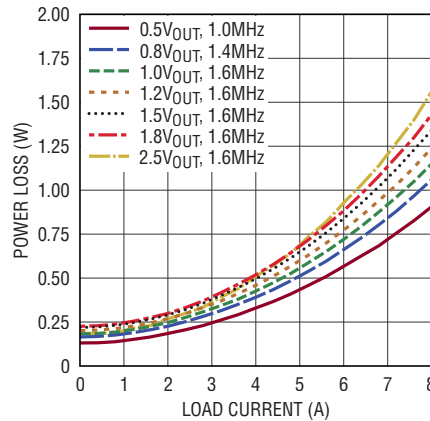
47101 G12

**Power Loss, Single Channel**  
 $V_{IN} = 2.5\text{V}$



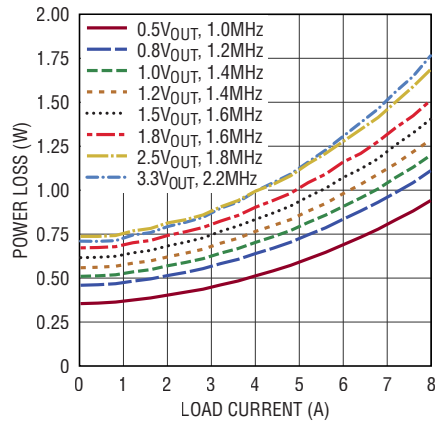
47101 G13

**Power Loss, Single Channel**  
 $V_{IN} = 3.3\text{V}$



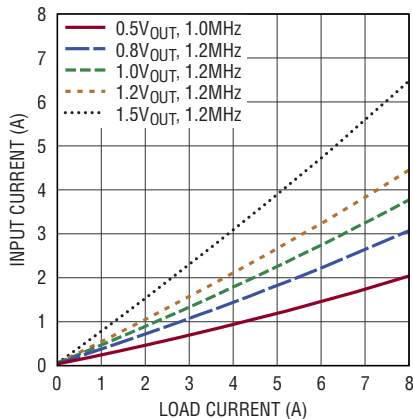
47101 G14

**Power Loss, Single Channel**  
 $V_{IN} = 5.5\text{V}$



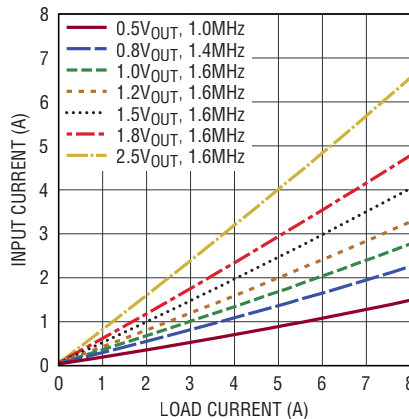
47101 G15

**Input vs Load Current**  
 $V_{IN} = 2.5\text{V}$ , Single Channel



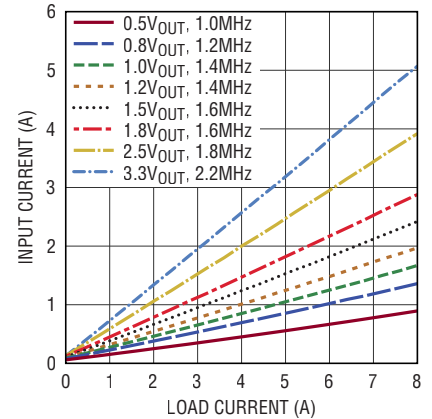
47101 G16

**Input vs Load Current**  
 $V_{IN} = 3.3\text{V}$ , Single Channel



47101 G17

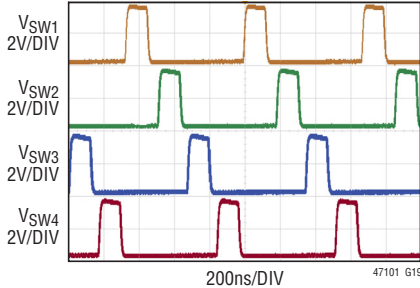
**Input vs Load Current**  
 $V_{IN} = 5.5\text{V}$ , Single Channel



47101 G18

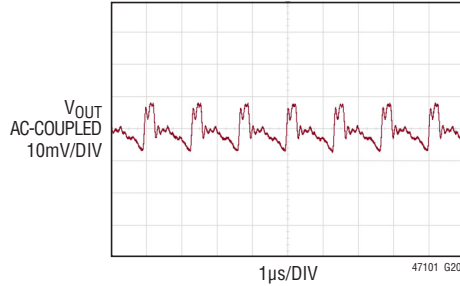
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Steady State  $V_{\text{SW}}$  with Persistence On**



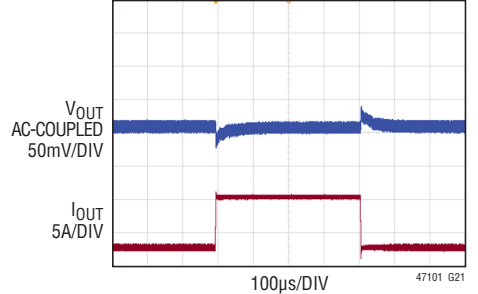
$V_{\text{IN}} = 3.3\text{V}$ ,  $V_{\text{OUT}} = 0.6\text{V}$ ,  $I_{\text{OUT}} = 30\text{A}$ ,  
 $f_{\text{SW}} = 1.5\text{MHz}$ ,  $C_{\text{OUT}} = 100\mu\text{F} \times 4$

**Steady State Voltage Ripple**



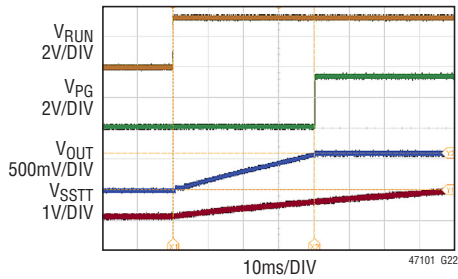
$V_{\text{IN}} = 3.3\text{V}$ ,  $V_{\text{OUT}} = 0.6\text{V}$ ,  $I_{\text{OUT}} = 30\text{A}$ ,  
 $f_{\text{SW}} = 1.5\text{MHz}$ ,  $C_{\text{OUT}} = 100\mu\text{F} \times 4$

**Load Transient Response**



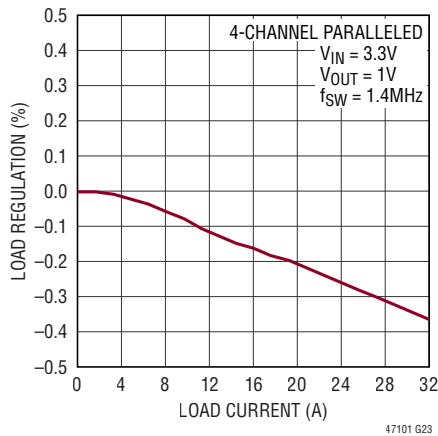
$V_{\text{IN}} = 3.3\text{V}$ ,  $V_{\text{OUT}} = 0.6\text{V}$ ,  $f_{\text{SW}} = 1.5\text{MHz}$ ,  
 $C_{\text{OUT}} = 100\mu\text{F} \times 4$ ,  $C_{\text{FF}} = 20\text{pF}$ ,  
 $0\text{A} \sim 7.5\text{A}$  (25%) LOAD STEP, 4-PHASE

**Start-Up**

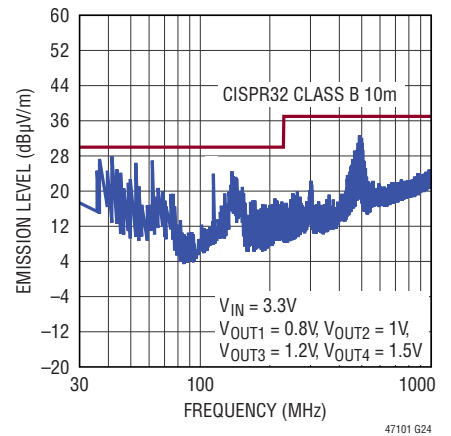


$V_{\text{IN}} = 3.3\text{V}$ ,  $V_{\text{OUT}} = 0.6\text{V}$ ,  
 $f_{\text{SW}} = 1.5\text{MHz}$ ,  $C_{\text{OUT}} = 100\mu\text{F} \times 4$

**Load Regulation, 1V  
DC3164A-B Demo Board**



**Radiated Emissions  
8A Load on Each Channel  
DC3164A-B, without Ferrite Bead**



## PIN FUNCTIONS



PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

**GND (Bank 1, Banks 10 – 12, Pin A9):** Power Ground Pins for All Input and Output Returns.

**$V_{IN1}$ ,  $V_{IN2}$ ,  $V_{IN3}$ ,  $V_{IN4}$  (Banks 2 – 5, Pin D9):** Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between  $V_{IN}$  pins and GND pins.

**$V_{OUT1}$ ,  $V_{OUT2}$ ,  $V_{OUT3}$ ,  $V_{OUT4}$  (Banks 6 – 9):** Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

**RUN1, RUN2, RUN3, RUN4 (Pins A5, F5, K5, R5):** Enables chip operation by connecting RUN above 0.4V. Connecting it to GND shuts down the device.

**FB1, FB2, FB3, FB4 (Pins A6, F6, K6, R6):** The negative input of the error amplifier for the switching mode regulator channel. The LTM4710-1 regulates the voltage between FB and AGND to 500mV. For FB1, this pin is internally connected to  $V_{OSNS1}$  with a 10k 0.5% precision resistor. Different output voltages can be programmed with an additional resistor between  $V_{OSNS1}$  and AGND. For FB2, FB3 and FB4, a resistor divider connecting to  $V_{OUT}$  sets the output voltage. In PolyPhase<sup>®</sup> operation, tie the FB pins to  $V_{IN}$  to disable the internal error amplifier. See the Applications Information section for details.

**SSTT1, SSTT2, SSTT3, SSTT4 (Pins B5, G5, L5, T5):** Soft-Start, Tracking and Temperature Monitor Pins. An internal 10 $\mu$ A current into an external capacitor on the soft-start pin programs the output voltage ramp rate during start-up. When SSTT is below 0.5V, the  $V_{FB}$  pin voltage will track the SSTT pin voltage. When SSTT is above 0.5V, the tracking function is disabled, the internal reference resumes control of the error amplifier and the SSTT pin servos to a voltage representative of a junction temperature. During shutdown and fault conditions, the SSTT pin is pulled to ground.

**COMP1b, COMP2b, COMP3b, COMP4b (Pins B6, G6, L6, T6):** Internal Compensation Network. These pins are to be connected to their respective COMPa pins. When utilizing specific external compensation, float these pins.

**PG1, PG2, PG3, PG4 (Pins C5, H5, M5, U5):** Output power good with open-drain logic of the switching mode regulator channel. PG is pulled to ground when the voltage on the FB pin is not within  $-2\%$  and  $+10\%$  of the internal 0.5V reference.

**COMP1a, COMP2a, COMP3a, COMP4a (Pins C6, H6, M6, U6):** Current control threshold and error amplifier compensation point of the switching mode regulator channel.

**MODE1, MODE2, MODE3, MODE4 (Pins D5, J5, N5, V5):** MODE pin facilitates multiphase operation and synchronization to an external clock. Depending on the mode of operation, the MODE either accepts a clock pulse or outputs a clock pulse at its operating frequency. See the Applications Information section for details.

**RT1, RT2, RT3, RT4 (Pins D6, J6, N6, V6):** The frequency pin sets the oscillator frequency with an external resistor to AGND or sets the phasing for multiphase operation. See the Applications Information of section for frequency adjustment.

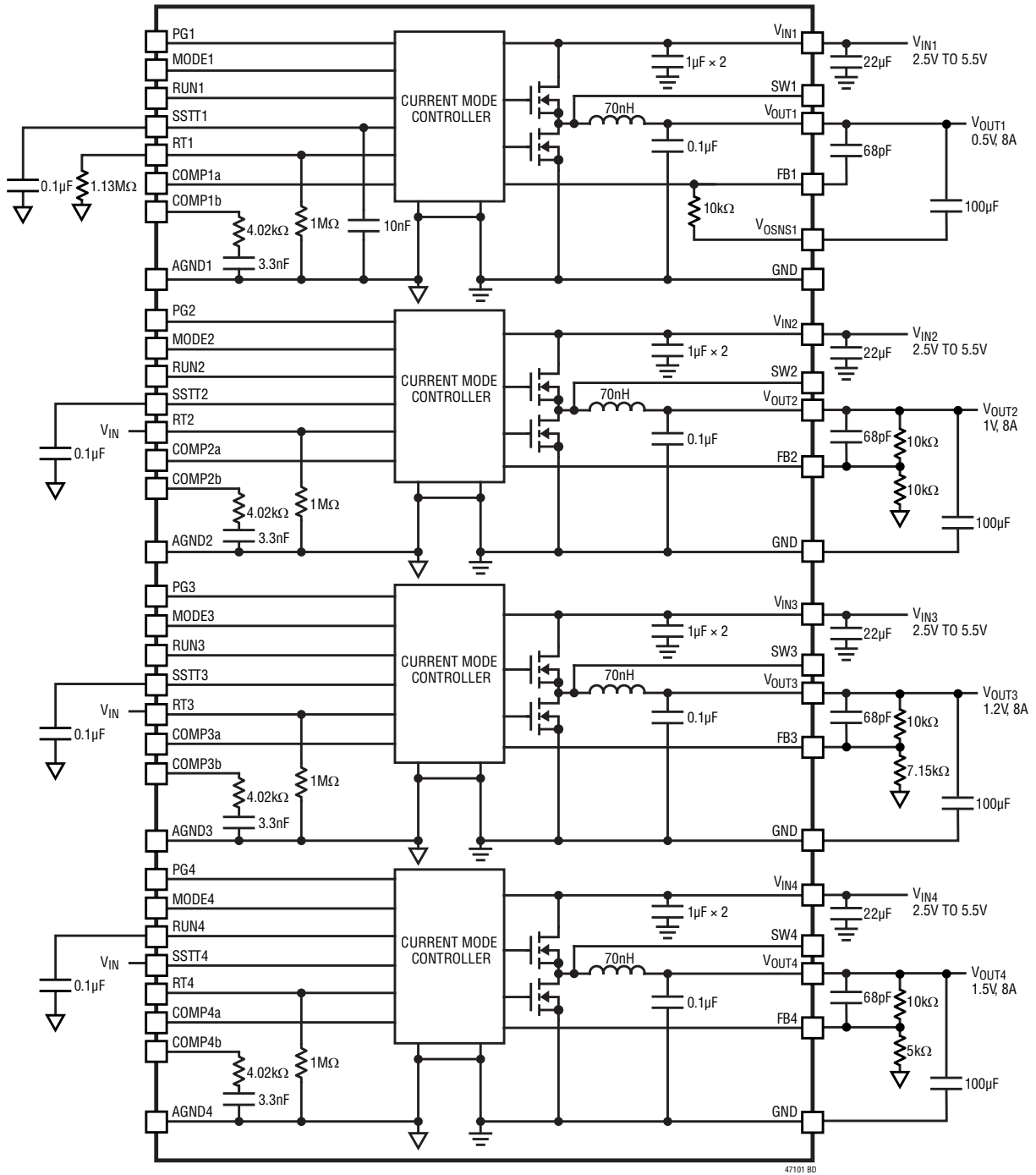
**$V_{OSNS1}$  (Pin D7):** Output Voltage Sense Pin of Channel 1. Internally, this pin is connected to the FB1 pin with a 10k, 0.5% precision resistor. It is very important to connect this pin to the  $V_{OUT1}$  since this is the feedback path and cannot be left open. See the Applications Information section for details.

**AGND1, AGND2, AGND3, AGND4 (Pins D8, H7, L7, U7):** The AGND pin is the output voltage remote ground sense. Connect the AGND pin directly to the negative terminal of the output capacitor at the load and to the feedback divider resistor.

**SW1, SW2, SW3, SW4 (Pins G2, K2, N2, T2):** Switching node waveform monitoring.

**NC (Pins A7, A8, B7, B8, B9, C7, C8, C9):** No Connection. Leave these pins open.

**BLOCK DIAGRAM**



**DECOUPLING REQUIREMENTS** (Per Channel)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN}$	External Input Capacitor Requirement ( $V_{IN} = 2.5V$ to $5.5V$ , $V_{OUT} = 0.5V$ )	$I_{OUT} = 8A$	22			$\mu F$
$C_{OUT}$	External Output Capacitor Requirement ( $V_{IN} = 2.5V$ to $5.5V$ , $V_{OUT} = 0.5V$ )	$I_{OUT} = 8A$	100			$\mu F$

Rev. 0



## OPERATION

The LTM4710-1 is a quad output step-down switch mode DC/DC power supply. It integrates four separate regulators, each capable of delivering up to 8A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable from 0.5V to 3.6V over a 2.5V to 5.5V input voltage range. See typical application schematic (Figure 1).

The LTM4710-1 integrates four separate constant-frequency peak current mode control regulators, power MOSFETs, inductors, and other supporting discrete components. It employs Silent Switcher 2 technology, which allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance. Ceramic Capacitors on  $V_{IN}$  keep all the fast AC current loops small, improving EMI performance.

With current mode control and internal feedback loop compensation, the LTM4710-1 has sufficient stability margins and fast transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

The switching frequency for LTM4710-1 can be adjusted by an external resistor from RT to AGND, or the LTM4710-1 can be externally synchronized to a clock. See the Applications Information section.

Current mode control provides cycle-by-cycle fast current limiting. Peak current limiting is provided in an overcurrent condition. The internal overvoltage and undervoltage comparators pull the open-drain PG output low if the output feedback voltage exits a  $-2\%$  and  $+10\%$  window around the regulation point. Furthermore, in an overvoltage condition, the internal top MOSFET is turned off, and the bottom MOSFET is turned on and held on until the overvoltage condition clears.

The multiphase operation can be easily configurable with synchronization and phase mode controls.

Pulling the RUN pin to GND forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry.

The SSTT pin is used for power supply tracking, soft-start programming and, and monitoring die temperature. See the Applications Information section.

Forced continuous mode (FCM) is the only operation mode recommended for low ripple and low noise consideration. The switching frequency of the four channels should always be synchronized regardless the output(s) are paralleled or independent. For multiphase paralleled output, phase-shift interleaving is recommended. For independent outputs, an aligned main-switch turn-on transition is recommended. See the Applications Information section and Typical Applications for more information.

## APPLICATIONS INFORMATION

The typical LTM4710-1 application circuit is shown in Figure 1. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. See Table 10 for specific external capacitor requirements for a particular application.

### $V_{IN}$ to $V_{OUT}$ Step-Down Ratios

There are restrictions in the minimum  $V_{OUT}$  step-down ratio that can be achieved for a given input voltage due to the minimum on-time limits of the regulator.

The minimum on-time limit imposes a minimum duty cycle of the converter, which can be calculated with Equation 1.

$$D_{(MIN)} = t_{ON(MIN)} \cdot f_{SW} \quad (1)$$

where  $t_{ON(MIN)}$  is the minimum on-time, 40ns typical for LTM4710-1. In the rare cases where the minimum duty cycle is surpassed, the output voltage will remain in regulation, but the switching frequency will decrease from its programmed value.

## APPLICATIONS INFORMATION

### Output Voltage Programming

The PWM controller has an internal 0.5V reference voltage. As shown in the Block Diagram, a 10k (0.5% tolerance) internal feedback resistor is included in channel 1 only. The 10k resistor connects FB1 to  $V_{OSNS1}$ , which should be directly connected to the  $V_{OUT1}$  sense point. 10k external top feedback resistor is recommended for  $V_{OUT2,3,4}$  if operating independently. Adding a resistor  $R_{BOT}$  from FB pin to the AGND pin programs the output voltage (Equation 2).

$$V_{OUT}(V) = 0.5V \cdot \frac{10k + R_{BOT}}{R_{BOT}} \quad (2)$$

### Input Decoupling Capacitors

Each channel of the LTM4710-1 module should be connected to a low AC-impedance DC source. For the regulator, at least 22 $\mu$ F input ceramic capacitor is recommended for RMS ripple current decoupling. Bulk input capacitors are needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor or polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated with Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)} \quad (3)$$

where  $\eta$  is the estimated efficiency of the power module.

### Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only a 100 $\mu$ F low ESR output ceramic capacitor is required for each channel to achieve low output voltage ripple and a very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 10 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2A (25%) load step transient.

The multiphase operation will reduce effective output ripple as a function of the number of phases. [Application Note 77](#)

discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The [LTpowerCAD](#)<sup>®</sup> design tool is available to download on-line for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

### Mode of Operation

The MODE pin is either a clock input or a clock output. When configured as clock input, it synchronizes the switching frequency to an external clock (see Table 1).

The LTM4710-1 should operate in forced continuous mode (FCM) for low-noise applications.

**Table 1. LTM4710-1 Single Phase Configuration**

RT PIN CONNECTION	MODE PIN CONNECTION	MODE OF OPERATION	SWITCHING FREQUENCY
$V_{IN}$	Clock Input	Forced Continuous	External Clock
Float/Resistor to AGND	Clock Output	Forced Continuous	$R_T$ Programmed

### Setting the Operating Frequency

The frequency can be programmed by tying a resistor from RT to AGND pins (Equation 4).

$$R_T = 1113 \cdot f_{(SW)}^{-1.64} \quad (4)$$

where  $R_T$  is in k $\Omega$  and  $f_{SW}$  is the desired switching frequency in MHz.

The frequency can be programmed to switch from 1 MHz to 5 MHz. Table 2 shows the necessary  $R_T$  value for a desired switching frequency.

**Table 2. SW Frequency vs  $R_{FREQ}$  Value**

$f_{SW}$ (MHz)	$R_T$ (k $\Omega$ )
1	1130
1.5	536
2	340
2.2	301
3	196
4	140
5	105

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### Frequency Synchronization and Clock Input

The LTM4710-1 switching frequency can be adjusted by synchronizing the internal PLL circuit to an external square wave clock applied at the MODE pin. The synchronization frequency range is 1.2MHz to 2.6MHz. The external clock amplitude must be greater than 1.2V and less than 0.4V.

The internal PLL starts up at the 2MHz default frequency. After detecting an external clock on the first rising edge of the MODE pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the MODE signal.

### Multiphase Operation

For output loads that demand more than 8A of current, multiple LTM4710-1 channels can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. Table 3 shows the configuration for multiphase operation.

**Table 3. LTM4710-1 Multiphase Configuration**

PHASE	RT PIN	FB PIN	MODE PIN	SWITCHING FREQUENCY
Main	$V_{IN}$	$V_{OUT}$ Divider	Clock Input	External Clock
Main	Resistor to AGND	$V_{OUT}$ Divider	Clock Output	$R_T$ Programmed
Subordinate	$V_{IN}$ Divider	$V_{IN}$	Clock Input	External Clock

To parallel multiple LTM4710-1 channels to achieve the same switching frequency, perfect interleaved phase shift and accurate current sharing between different channels, one of the LTM4710-1 channels will become the main channel, and the rest of the LTM4710-1 channels need to be programmed as the subordinate channels.

Connecting the RT pin of the main phase to a resistor to AGND programs the frequency and configures the MODE pin to become the clock output used to drive the MODE pin of the subordinate phase(s).

Connecting the RT pin of the main phase to  $V_{IN}$  configures the MODE pin to become an input capable of accepting an external clock.

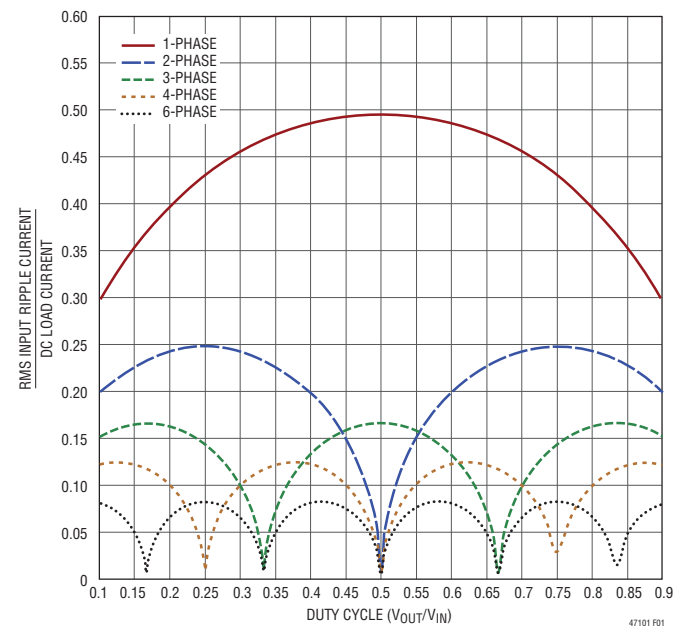
Connecting the  $V_{FB}$  pin to  $V_{IN}$  configures a phase as a subordinate phase. The MODE becomes a clock input, and the voltage control loop is disabled. The subordinate phase current control loop is still active, and the peak current is controlled via the shared COMP node.

The phasing of a subordinate phase relative to the main phase is programmed with a resistor divider on the RT pin. The use of 1% resistors is recommended. See Table 4 for more information. Figure 17 shows an example.

**Table 4. Subordinate Phase Shift Related to MODE Input**

PHASE ANGLE BETWEEN SUBORDINARY MODULE AND MODE INPUT (°)	$R_T$ RESISTOR TO $V_{IN}$ ( $\Omega$ )
0	0
90	3M
120	1.4M
180	( $R_T = GND$ )
240	715k
270	332k

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivation are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 1).



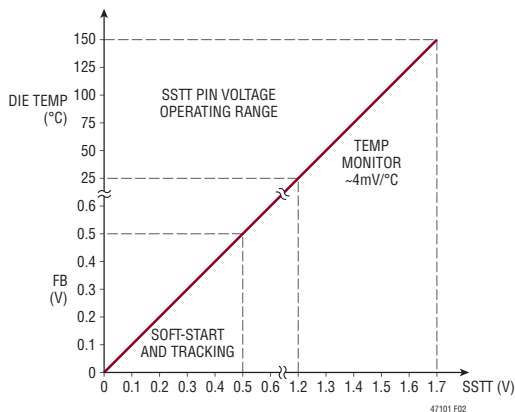
**Figure 1. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle**

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The LTM4710-1 device is an inherently current mode-controlled device, so that parallel modules will have very good current sharing. This will balance the thermals on all channels. Connect the RUN, COMP and PG pin of each paralleling channel together and connect FB to  $V_{IN}$  for subordinary channels. Figure 17 shows an example of parallel operation and pin connection.

### Soft-Start/Output Voltage Tracking/ Temperature Monitoring

The SSTT pin function facilitates supply sequencing, limits  $V_{IN}$  inrush current and reduces start-up output overshoot. An internal  $10\mu\text{A}$  charge up a capacitor on the SSTT pin hence program the ramp rate of the output voltage. SSTT pin can also be externally driven by another voltage source. During the soft-start ramp, when the SSTT voltage is below  $0.5\text{V}$ , the output voltage will proportionally track the SSTT pin voltage. When the SSTT voltage is above  $0.5\text{V}$ , the SSTT pin will servo to a voltage proportional to the LTM4710-1 die junction temperature (see Figure 2). The SSTT capacitor is reset during shutdown,  $V_{IN}$  UVLO and over thermal shutdown.



**Figure 2. Soft-Start and Temperature Monitor Operation**

The total soft-start time can be calculated with Equation 5.

$$t_{SS} = C_{SS} \cdot \frac{500\text{mV}}{10\mu\text{A}} \quad (5)$$

where  $C_{SS}$  is the capacitance on the SSTT pin. FCM is disabled during the soft-start process to prevent the current from reversing.

A default  $10\text{nF}$  soft-start cap is connected to SSTT1 inside the module, resulting in a  $0.5\text{ms}$  default start-up time on channel 1. The presence of this cap is to simplify customers' design in most cases.

### Output Power Good

When the LTM4710-1's output voltage is within the  $-2\%$  and  $+10\%$  window of the nominal regulation voltage, the output is considered good, and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds, include  $1\%$  of hysteresis as well as a built-in time delay, typically  $100\mu\text{s}$ . The PG pin is also actively pulled low during fault conditions: RUN pin is low,  $V_{IN}$  is too low or in thermal shutdown.

For multiphase applications, the PG pin is used for communication between the main and sub-ordinary phases. Connect the PG pins together and pull-up to  $V_{IN}$  or  $V_{OUT}$  with an external resistor. PG pins MUST be pulled higher than  $490\text{mV}$ .

### Stability Compensation

The LTM4710-1 has already been internally optimized and compensated for all output voltages and capacitor combinations including all ceramic capacitor applications when COMPb is tied to COMPa.

Table 10 is provided for most application requirements using the optimized internal compensation. For applications that need to achieve high bandwidth control loop compensation with enough phase margin, a  $68\text{pF}$  feed-forward capacitor is recommended from  $V_{OUT}$  to  $V_{FB}$  pin. For specific optimized requirement, disconnect COMPb from COMPa and apply a Type II C-R-C compensation network from COMPa to AGND to achieve external compensation. The LTpowerCAD design tool can be downloaded online to perform specific control loop optimization and analyze the control stability and load transient performance.

### RUN Enable

The LTM4710-1 has a precision threshold RUN pin to enable or disable the switching. When forced low, the RUN pin puts the LTM4710-1 into a low current shutdown

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mode. The rising threshold of the RUN comparator is 400mV, with 75mV of hysteresis. It can be tied to  $V_{IN}$  if the shutdown feature is not used. Adding a resistor divider from  $V_{IN}$  to RUN programs the LTM4710-1 to regulate the output only when  $V_{IN}$  is above a desired voltage. Typically, this threshold,  $V_{IN(EN)}$ , is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so the source current increases as the source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The  $V_{IN(EN)}$  threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 6.

$$V_{IN(EN)} = \left( \frac{R1}{R2} + 1 \right) \cdot 400\text{mV} \quad (6)$$

where the LTM4710-1 will remain off until  $V_{IN}$  is above  $V_{IN(EN)}$ . Due to the comparator's hysteresis, switching will not stop until the input falls slightly below  $V_{IN(EN)}$ .

Alternatively, a resistor divider from an output of another channel to the RUN pin of the LTM4710-1 provides event-based power-up sequencing, enabling the LTM4710-1 when the output of the other regulator reaches a predetermined level.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a  $\mu$ Module package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may use laboratory equipment and a test vehicle, such as the demo board, to anticipate the  $\mu$ Module regulator's thermal performance in their application at various electrical and environmental operating

conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in-and-of themselves, not relevant to providing guidance on thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives three thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below.

1.  $\theta_{JA}$ , the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air", although natural convection causes the air to move. This value is determined with the part mounted to the demo board DC3164A-B.
2.  $\theta_{JCbottom}$ , the thermal resistance from junction to bottom of the product case, is determined with all the component power dissipation flowing through the bottom of the package. In the typical module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value maybe useful for comparing packages, but the test conditions don't generally match the user's application.
3.  $\theta_{JCtop}$ , the thermal resistance from the junction to the top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical  $\mu$ Module are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of  $\theta_{JCbottom}$ , this value may be useful for comparing packages, but the test conditions don't generally match the user's application.

A graphical representation of the aforementioned thermal resistances is shown in Figure 3; blue resistances are contained within the  $\mu$ Module regulator, whereas green resistances are external to the  $\mu$ Module.

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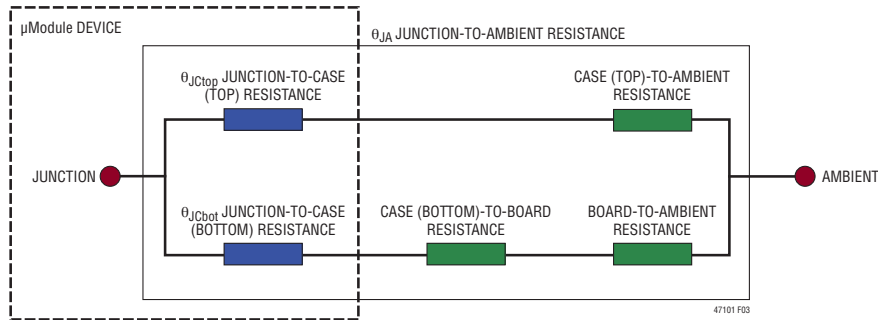


Figure 3. Graphical Representation of JEDEC Thermal Coefficients

Within the LTM4710-1 module, be aware that there are multiple power devices and components dissipating power, with the consequence that the thermal resistances relative to different junctions of components or die are not exactly linear to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the  $\mu$ Module and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4710-1 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields a set of derating curves, as shown in this datasheet.

After these laboratory tests have been performed and correlated to the LTM4710-1 model, then the  $\theta_{JB}$  and  $\theta_{BA}$  are

summed together to provide a value that should closely equal the  $\theta_{JA}$  value because approximately 100% of the power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

Figure 5 and Figure 6 (3.3V and 5V) power loss curves can be used in coordination with Figure 7 through Figure 15 load current derating curves for calculating an approximate  $\theta_{JA}$  thermal resistance for the LTM4710-1 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature and are increased with multiplicative factors according to the junction temperature. This approximate factor is 1.2 for 120°C at junction temperature. The maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is 5°C guard band from The maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing the ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 36A and the ambient temperature at 30°C. The output voltages are 0.5V, 0.8V, 1V, 1.2V, and 1.5V. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power

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with increasing the ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 13, the load current is derated to be 19.2A at 86.4°C with no air or heat sink, and the total power loss for 3.3V<sub>IN</sub> to 1.2V<sub>OUT</sub> at 19.2A is 2.6W (Figure 5), then multiply by the 1.2 coefficient for 120°C junction temperature, the total power loss for 4 channels is 3.2W, if 86.4°C ambient temperature is subtracted from 120°C junction temperature, the difference of the 33.6°C divided by 3.2W equals 10.5°C/W. Table 5 specifies an 11°C/W value which is very close. Table 5 to Table 9 provide equivalent thermal resistances for 0.5V, 0.8V, 1V, 1.2V and 1.5V outputs with and without airflow. The derived thermal resistances in Table 5 to Table 9 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss

can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick six-layer board with two-ounce copper on all six layers. The PCB dimensions are 4.25-inch × 4.48-inch.

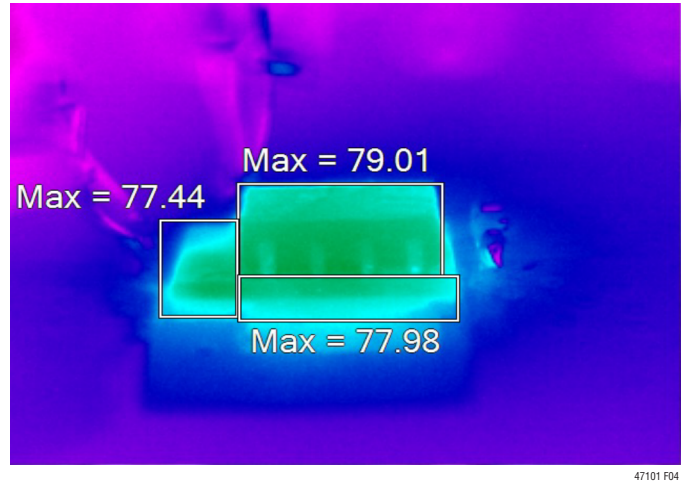


Figure 4. Thermal Image, LTM4710-1 Running from 3.3V Input to 0.5V, Paralleled 32A Output with No Airflow, No Heat Sink

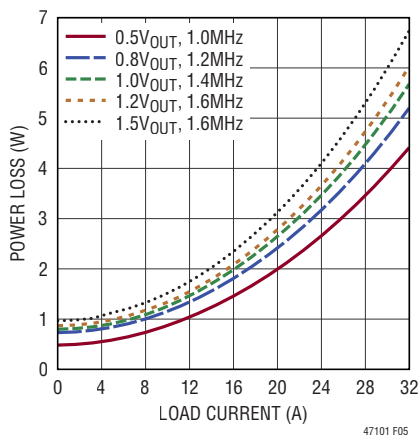


Figure 5. Power Loss, 4-Channel Paralleled V<sub>IN</sub> = 3.3V

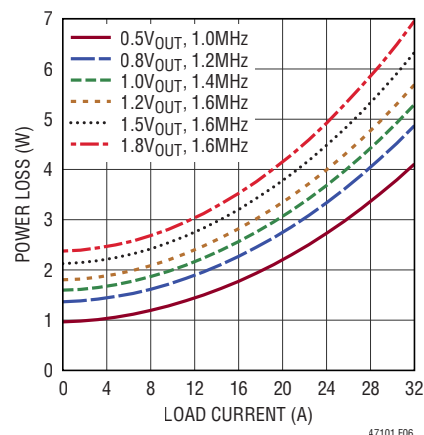


Figure 6. Power Loss, 4-Channel Paralleled V<sub>IN</sub> = 5.5V

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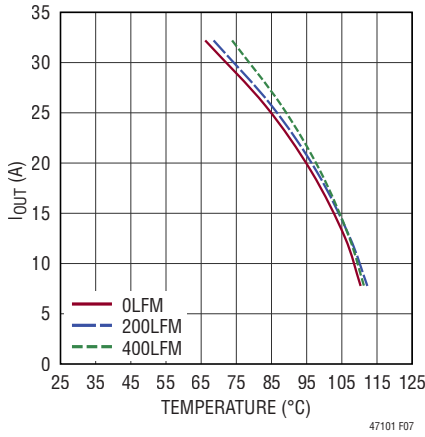


Figure 7. Derating, 4-Channel Paralleled  $V_{IN} = 3.3V$ ,  $V_{OUT} = 0.5V$  DC3164A-B Demo Board

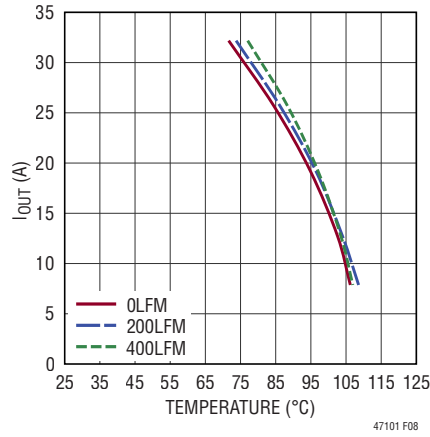


Figure 8. Derating, 4-Channel Paralleled  $V_{IN} = 5V$ ,  $V_{OUT} = 0.5V$  DC3164A-B Demo Board

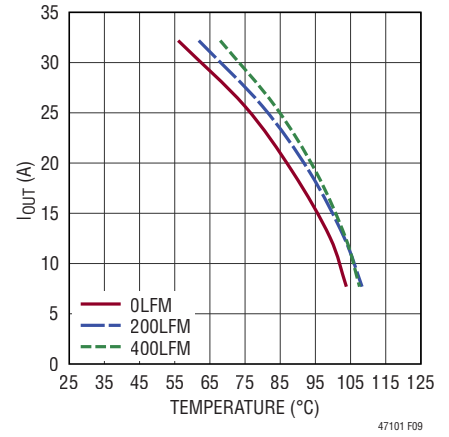


Figure 9. Derating, 4-Channel Paralleled  $V_{IN} = 3.3V$ ,  $V_{OUT} = 0.8V$  DC3164A-B Demo Board

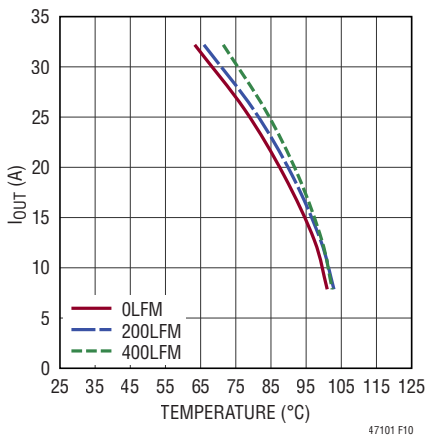


Figure 10. Derating, 4-Channel Paralleled  $V_{IN} = 5V$ ,  $V_{OUT} = 0.8V$  DC3164A-B Demo Board

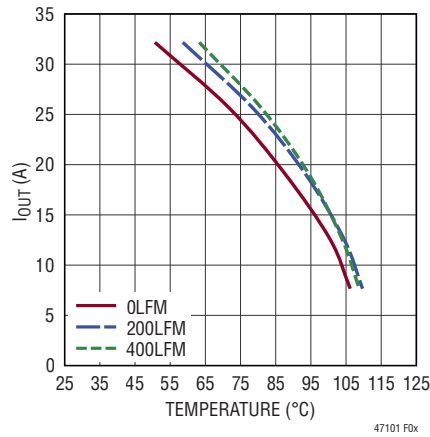


Figure 11. Derating, 4-Channel Paralleled  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1V$  DC3164A-B Demo Board

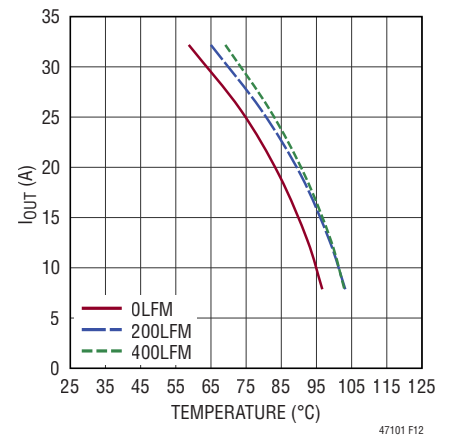


Figure 12. Derating, 4-Channel Paralleled  $V_{IN} = 5V$ ,  $V_{OUT} = 1V$  DC3164A-B Demo Board

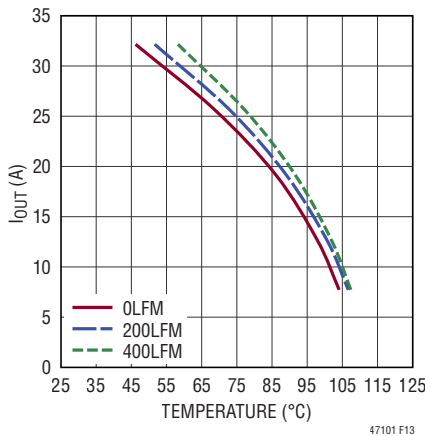


Figure 13. Derating, 4-Channel Paralleled  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$  DC3164A-B Demo Board

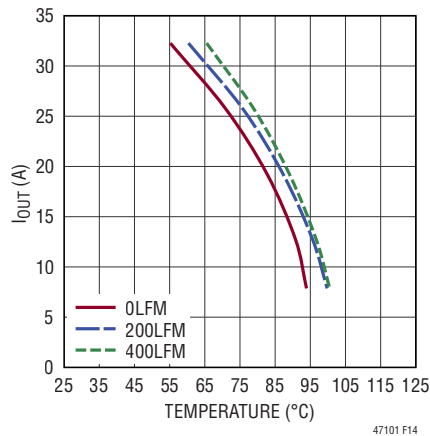


Figure 14. Derating, 4-Channel Paralleled  $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$  DC3164A-B Demo Board

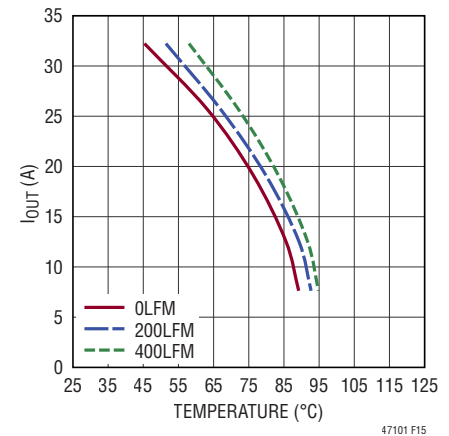


Figure 15. Derating, 4-Channel Paralleled  $V_{IN} = 5V$ ,  $V_{OUT} = 1.5V$  DC3164A-B Demo Board



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**Table 5. 0.5V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figure 7, Figure 8	3.3, 5	Figure 5, Figure 6	0	None	11
Figure 7, Figure 8	3.3, 5	Figure 5, Figure 6	200	None	9
Figure 7, Figure 8	3.3, 5	Figure 5, Figure 6	400	None	10

**Table 6. 0.8V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figure 9, Figure 10	3.3, 5	Figure 5, Figure 6	0	None	14
Figure 9, Figure 10	3.3, 5	Figure 5, Figure 6	200	None	10
Figure 9, Figure 10	3.3, 5	Figure 5, Figure 6	400	None	11

**Table 7. 1.0V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figure 11, Figure 12	3.3, 5	Figure 5, Figure 6	0	None	12
Figure 11, Figure 12	3.3, 5	Figure 5, Figure 6	200	None	9
Figure 11, Figure 12	3.3, 5	Figure 5, Figure 6	400	None	9

**Table 8. 1.2V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figure 13, Figure 14	3.3, 5	Figure 5, Figure 6	0	None	12
Figure 13, Figure 14	3.3, 5	Figure 5, Figure 6	200	None	9
Figure 13, Figure 14	3.3, 5	Figure 5, Figure 6	400	None	9

**Table 9. 1.5V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figure 15	5	Figure 5, Figure 6	0	None	12
Figure 15	5	Figure 5, Figure 6	200	None	11
Figure 15	5	Figure 5, Figure 6	400	None	10

**Table 10. Output Voltage Response vs Component Matrix, 6A to 8A Load Step Typical Measured Values, Freq = 1.5MHz**

V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	C <sub>IN</sub> CERAMIC (μF)	C <sub>OUT1,2,3,4</sub> CERAMIC (μF)	C <sub>FF</sub> (pF)	PEAK-PEAK DERIVATION (mV)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/μs)	R <sub>FB</sub> (kΩ)	COMPENSATION
2.5	0.5	22 ×2 + 47	22 + 47 + 100	68	42.2	2	2	Open	Module Internal Compensation
3.3	0.5	22 ×2 + 47	22 + 47 + 100	68	44.9	2	2	Open	Module Internal Compensation
5	0.5	22 ×2 + 47	22 + 47 + 100	68	48.9	2	2	Open	Module Internal Compensation
5.5	0.5	22 ×2 + 47	22 + 47 + 100	68	49.5	2	2	Open	Module Internal Compensation
2.5	0.8	22 ×2 + 47	22 + 47 + 100	68	54.9	2	2	16.5	Module Internal Compensation
3.3	0.8	22 ×2 + 47	22 + 47 + 100	68	56.9	2	2	16.5	Module Internal Compensation
5	0.8	22 ×2 + 47	22 + 47 + 100	68	60.3	2	2	16.5	Module Internal Compensation
5.5	0.8	22 ×2 + 47	22 + 47 + 100	68	60.3	2	2	16.5	Module Internal Compensation
2.5	1	22 ×2 + 47	22 + 47 + 100	68	58.2	2	2	10	Module Internal Compensation
3.3	1	22 ×2 + 47	22 + 47 + 100	68	59.6	2	2	10	Module Internal Compensation

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**Table 10. Output Voltage Response vs Component Matrix, 6A to 8A Load Step Typical Measured Values, Freq = 1.5MHz**

$V_{IN}$ (V)	$V_{OUT}$ (V)	$C_{IN}$ CERAMIC ( $\mu$ F)	$C_{OUT1,2,3,4}$ CERAMIC ( $\mu$ F)	$C_{FF}$ (pF)	PEAK-PEAK DERIVATION (mV)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/ $\mu$ s)	$R_{FB}$ (k $\Omega$ )	COMPENSATION
5	1	22 $\times$ 2 + 47	22 + 47 + 100	68	62.9	2	2	10	Module Internal Compensation
5.5	1	22 $\times$ 2 + 47	22 + 47 + 100	68	61.6	2	2	10	Module Internal Compensation
2.5	1.2	22 $\times$ 2 + 47	22 + 47 + 100	68	71.6	2	2	7.15	Module Internal Compensation
3.3	1.2	22 $\times$ 2 + 47	22 + 47 + 100	68	73	2	2	7.15	Module Internal Compensation
5	1.2	22 $\times$ 2 + 47	22 + 47 + 100	68	79	2	2	7.15	Module Internal Compensation
5.5	1.2	22 $\times$ 2 + 47	22 + 47 + 100	68	82	2	2	7.15	Module Internal Compensation
2.5	1.5	22 $\times$ 2 + 47	22 + 47 + 100	68	78	2	2	4.99	Module Internal Compensation
3.3	1.5	22 $\times$ 2 + 47	22 + 47 + 100	68	80	2	2	4.99	Module Internal Compensation
5	1.5	22 $\times$ 2 + 47	22 + 47 + 100	68	90	2	2	4.99	Module Internal Compensation
5.5	1.5	22 $\times$ 2 + 47	22 + 47 + 100	68	90	2	2	4.99	Module Internal Compensation

### Safety Considerations

The LTM4710-1 modules do not provide galvanic isolation from  $V_{IN}$  to  $V_{OUT}$ . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current must be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

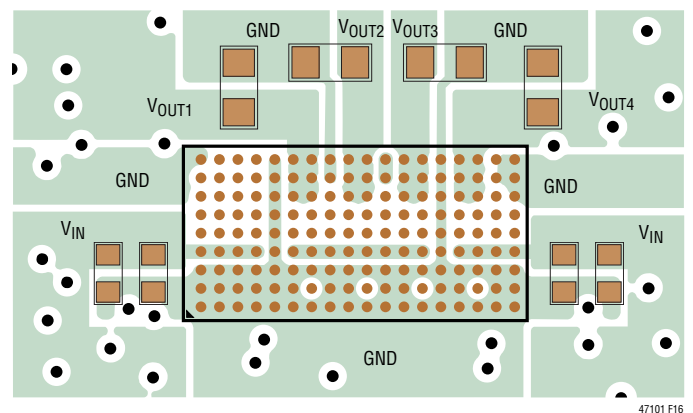
### Layout Checklist/Example

The high integration of LTM4710-1 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

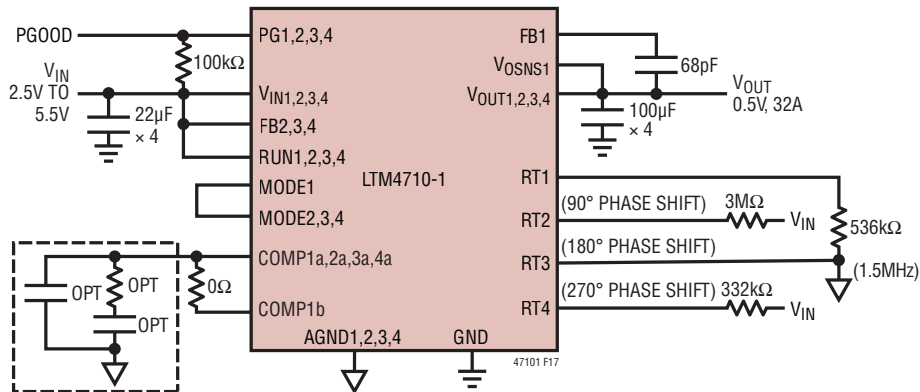
- Use large PCB copper areas for high current paths, including  $V_{IN}$ , GND and  $V_{OUT}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high-frequency ceramic input and output capacitors next to the  $V_{IN}$ , GND and  $V_{OUT}$  pins to minimize high-frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated AGND ground copper area for components connected to signal pins. See AGND in Figure 17.
- For parallel modules, tie the  $V_{OUT}$ , FB, and COMP pins together. Use an internal layer to closely connect these pins together. The SSTT pin should NOT be tied together for temperature monitoring of each silicon independently.
- Bring out test points on the signal pins for monitoring.
- Solder mask-defined pin pads are recommended.

Figure 16 gives a good example of the recommended layout.

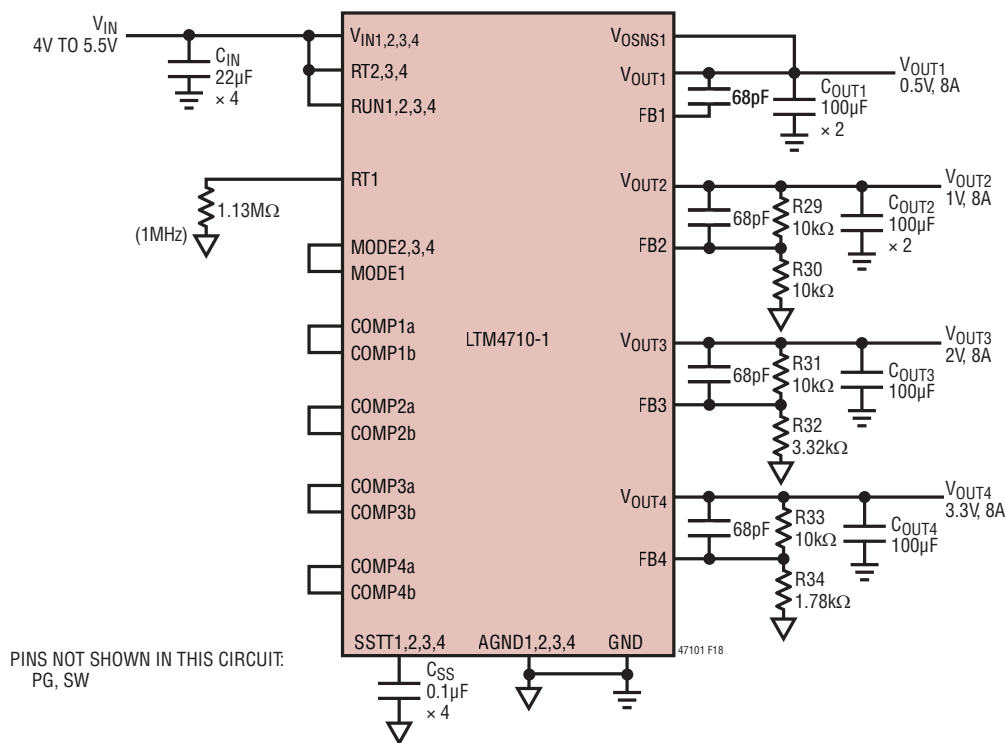

**Figure 16. Recommended PCB Layout**

# TYPICAL APPLICATIONS



PINS NOT SHOWN IN THIS CIRCUIT: SSTT, SW

Figure 17. Paralleled Single Output, 32A DC/DC μModule Regulator



PINS NOT SHOWN IN THIS CIRCUIT:  
PG, SW

Figure 18. 0.5V, 8A; 1V, 8A; 2V, 8A; and 3.3V, 8A Outputs from 4V to 5.5V Input, Switching Frequency Synchronized

## TYPICAL APPLICATION

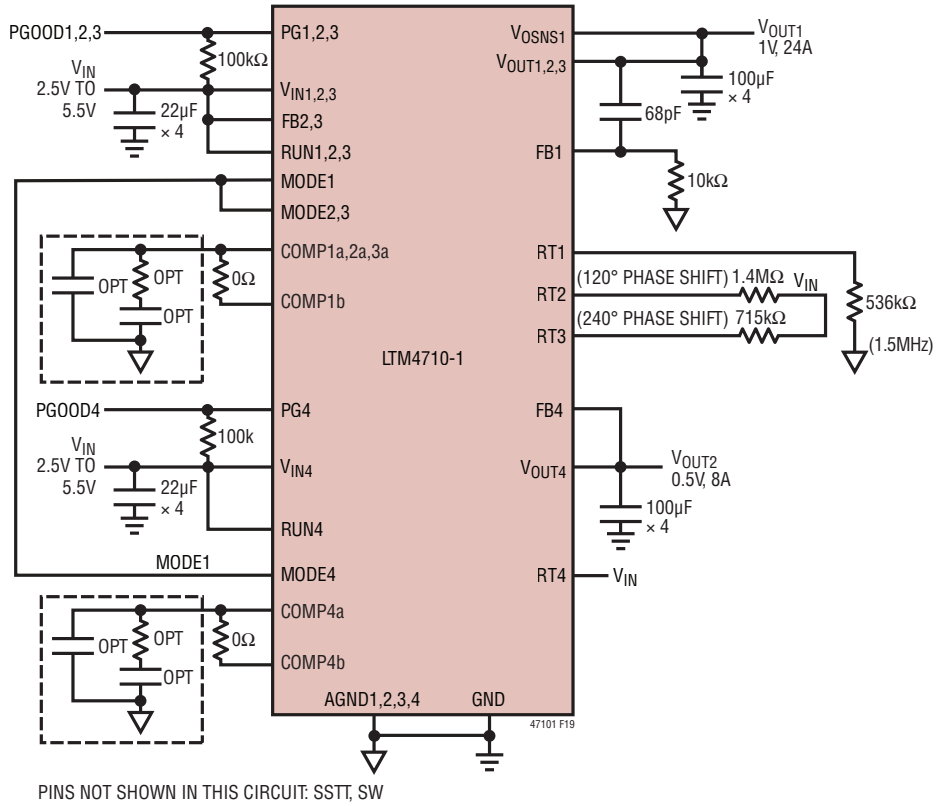


Figure 19. 1V, 24A; 0.5V, 8A; Outputs from 2.5V to 5.5V Input

## PACKAGE PINOUT DESCRIPTION

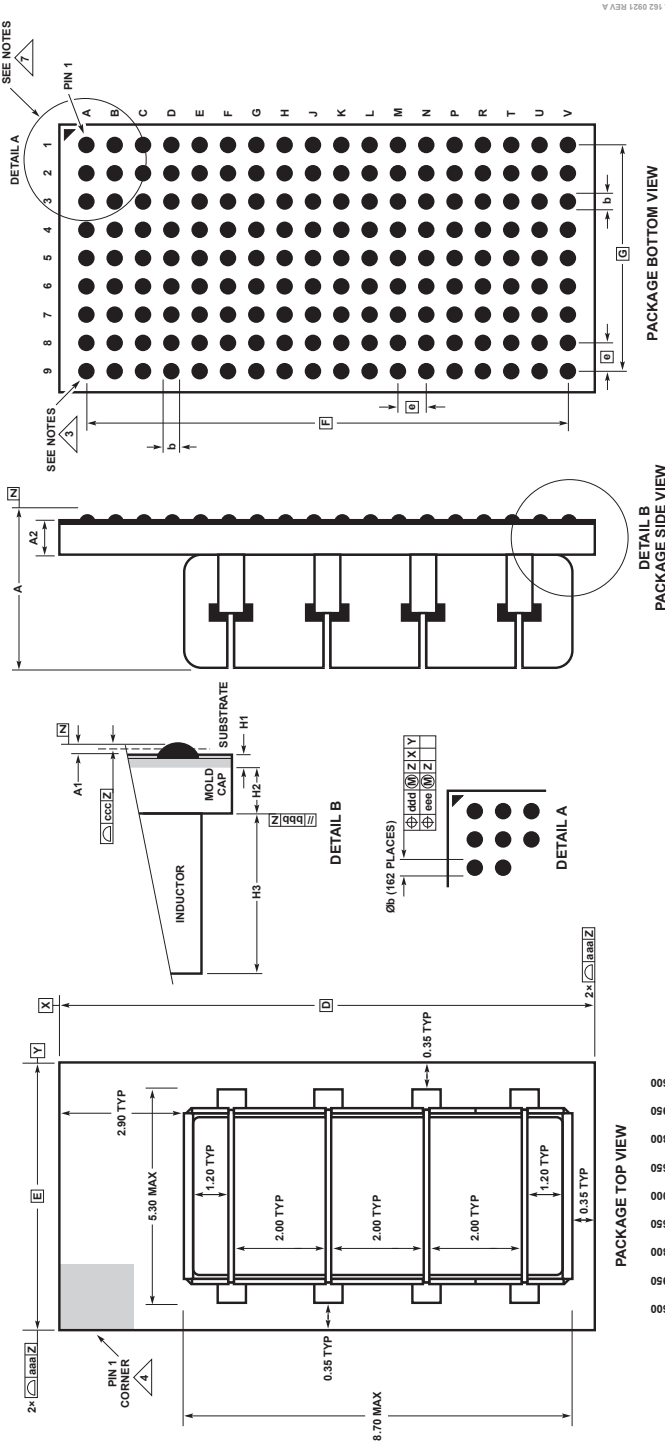


PACKAGE ROW AND COLUMN LABELING MAY VARY  
AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE  
LAYOUT CAREFULLY.

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
A9	GND	B9	NC	C9	NC	D9	V <sub>IN1</sub>	E9	GND	F9	V <sub>OUT1</sub>
A8	NC	B8	NC	C8	NC	D8	AGND1	E8	GND	F8	V <sub>OUT1</sub>
A7	NC	B7	NC	C7	NC	D7	V <sub>OSNS1</sub>	E7	GND	F7	V <sub>OUT1</sub>
A6	FB1	B6	COMP1b	C6	COMP1a	D6	RT1	E6	GND	F6	FB2
A5	RUN1	B5	SSTT1	C5	PG1	D5	MODE1	E5	GND	F5	RUN2
A4	V <sub>IN1</sub>	B4	V <sub>IN1</sub>	C4	V <sub>IN1</sub>	D4	V <sub>IN1</sub>	E4	GND	F4	V <sub>IN2</sub>
A3	GND	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND
A2	GND	B2	GND	C2	GND	D2	GND	E2	GND	F2	GND
A1	GND	B1	GND	C1	GND	D1	GND	E1	GND	F1	GND
G9	V <sub>OUT1</sub>	H9	GND	J9	V <sub>OUT2</sub>	K9	V <sub>OUT2</sub>	L9	GND	M9	V <sub>OUT3</sub>
G8	V <sub>OUT1</sub>	H8	GND	J8	V <sub>OUT2</sub>	K8	V <sub>OUT2</sub>	L8	GND	M8	V <sub>OUT3</sub>
G7	V <sub>OUT1</sub>	H7	AGND2	J7	V <sub>OUT2</sub>	K7	V <sub>OUT2</sub>	L7	AGND3	M7	V <sub>OUT3</sub>
G6	COMP2b	H6	COMP2a	J6	RT2	K6	FB3	L6	COMP3b	M6	COMP3a
G5	SSTT2	H5	PG2	J5	MODE2	K5	RUN3	L5	SSTT3	M5	PG3
G4	V <sub>IN2</sub>	H4	V <sub>IN2</sub>	J4	V <sub>IN2</sub>	K4	V <sub>IN3</sub>	L4	V <sub>IN3</sub>	M4	V <sub>IN3</sub>
G3	GND	H3	GND	J3	GND	K3	GND	L3	GND	M3	GND
G2	SW1	H2	GND	J2	GND	K2	SW2	L2	GND	M2	GND
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
N9	V <sub>OUT3</sub>	P9	GND	R9	V <sub>OUT4</sub>	T9	V <sub>OUT4</sub>	U9	GND	V9	GND
N8	V <sub>OUT3</sub>	P8	GND	R8	V <sub>OUT4</sub>	T8	V <sub>OUT4</sub>	U8	GND	V8	GND
N7	V <sub>OUT3</sub>	P7	GND	R7	V <sub>OUT4</sub>	T7	V <sub>OUT4</sub>	U7	AGND4	V7	GND
N6	RT3	P6	GND	R6	FB4	T6	COMP4b	U6	COMP4a	V6	RT4
N5	MODE3	P5	GND	R5	RUN4	T5	SSTT4	U5	PG4	V5	MODE4
N4	V <sub>IN3</sub>	P4	GND	R4	V <sub>IN4</sub>	T4	V <sub>IN4</sub>	U4	V <sub>IN4</sub>	V4	V <sub>IN4</sub>
N3	GND	P3	GND	R3	GND	T3	GND	U3	GND	V3	GND
N2	SW3	P2	GND	R2	GND	T2	SW4	U2	GND	V2	GND
N1	GND	P1	GND	R1	GND	T1	GND	U1	GND	V1	GND

# PACKAGE DESCRIPTION

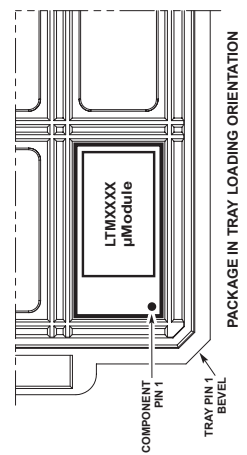
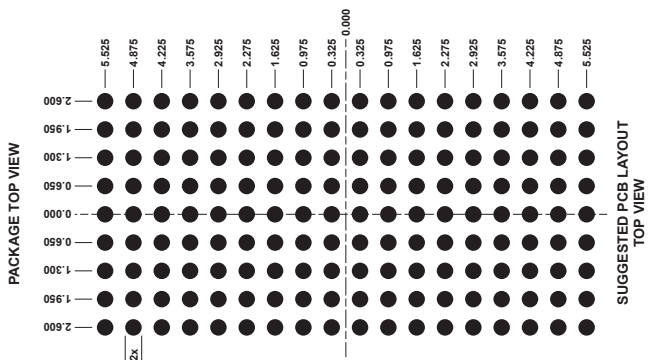
**LGA Package**  
**162-Lead (6mm x 12mm x 3.54mm)**  
 (Reference DWG# 05-08-7101 Rev A)



BGA 162 0921 REV A

- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. LAND DESIGNATION PER JEP95
  4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	3.21	3.54	3.87
A1			0.08
A2	0.86	0.95	1.04
b	0.32	0.35	0.38
D		12.00	
E		6.00	
e		0.65	
F		11.05	
G		5.20	
H1		0.25 REF	SUBSTRATE THK
H2		0.70 REF	MOLD CAP HT
H3		2.525	INDUCTOR HT
aaa			0.15
bbb			0.10
ccc			0.20
ddd			0.25
eee			0.10

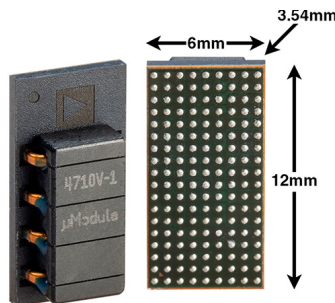


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## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	07/23	Initial Release.	—

## PACKAGE PHOTOS Part marking is either ink mark or laser mark



## DESIGN RESOURCES

SUBJECT	DESCRIPTION
<a href="#">µModule Design and Manufacturing Resources</a>	<p>Design:</p> <ul style="list-style-type: none"> <li>• Selector Guides</li> <li>• Demo Boards and Gerber Files</li> <li>• Free Simulation Tools</li> </ul> <p>Manufacturing:</p> <ul style="list-style-type: none"> <li>• Quick Start Guide</li> <li>• PCB Design, Assembly and Manufacturing Guidelines</li> <li>• Package and Board Level Reliability</li> </ul>
<a href="#">µModule Regulator Products Search</a>	<ol style="list-style-type: none"> <li>1. Sort table of products by parameters and download the result as a spread sheet.</li> <li>2. Search using the Quick Power Search parametric table.</li> </ol> <div style="border: 1px solid #ccc; padding: 10px; margin-top: 10px;"> <p><b>Quick Power Search</b></p> <p>INPUT   <math>V_{in}(\text{Min})</math> <input type="text"/> V <math>V_{in}(\text{Max})</math> <input type="text"/> V</p> <p>OUTPUT   <math>V_{out}</math> <input type="text"/> V <math>I_{out}</math> <input type="text"/> A</p> <p>FEATURES   <input type="checkbox"/> Low EMI <input type="checkbox"/> Ultrathin <input type="checkbox"/> Internal Heat Sink</p> <p style="text-align: center;"><input type="button" value="Multiple Outputs"/> <input type="button" value="Search"/></p> </div>
<a href="#">Digital Power System Management</a>	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTM4691</a>	Low $V_{IN}$ , Ultrathin, Dual 2A µModule Regulator	$2.25V \leq V_{IN} \leq 3.6V$ , $0.5V \leq V_{OUT} \leq 2.5V$ , 3mm × 4mm × 1.18mm LGA, 3mm × 4mm × 1.48mm BGA
<a href="#">LTM4693</a>	Low $V_{IN}$ , Ultrathin, 2A Buck-Boost µModule Regulator	$2.6V \leq V_{IN} \leq 5.5V$ , $1.8V \leq V_{OUT} \leq 5.5V$ , 3.5mm × 4mm × 1.25mm LGA
<a href="#">LTM4663</a>	Ultrathin, 1.5A µModule TEC Controller	$2.7V \leq V_{IN} \leq 5.5V$ , 3.5mm × 4mm × 1.3mm LGA
<a href="#">LTM4658</a>	Low $V_{IN}$ , 10A µModule Regulator	$2.25V \leq V_{IN} \leq 5.5V$ , $0.5V \leq V_{OUT} \leq V_{IN}$ , 4mm × 4mm × 4.32mm LGA
<a href="#">LTM4670</a>	Low $V_{IN}$ , Quad 10A µModule Regulator	$2.25V \leq V_{IN} \leq 5.5V$ , $0.5V \leq V_{OUT} \leq V_{IN}$ , 7.5mm × 15mm × 4.65mm BGA
<a href="#">LTM4611</a>	Ultralow $V_{IN}$ , 15A µModule Regulator	$1.5V \leq V_{IN} \leq 5.5V$ , $0.8V \leq V_{OUT} \leq 5V$ , 15mm × 15mm × 4.32mm LGA
<a href="#">LTM4643</a>	Low $V_{IN}$ with External Bias Voltage, Quad 3A µModule Regulator	$2.375V \leq V_{IN} \leq 20V$ , $0.6V \leq V_{OUT} \leq 3.3V$ , 9mm × 15mm × 1.82mm BGA, 9mm × 15mm × 2.42mm BGA
<a href="#">LTM4702</a>	16 $V_{IN}$ , 8A Ultralow Noise Silent Switcher µModule Regulator	$3V \leq V_{IN} \leq 16V$ , $0.3V \leq V_{OUT} \leq 5.7V$ , 6.25mm × 6.25mm × 5.07mm BGA
<a href="#">LTM8060</a>	Quad 40 $V_{IN}$ , Silent Switcher µModule Regulator with Configurable 3A Output Array	$3V \leq V_{IN} \leq 40V$ , $0.8V \leq V_{OUT} \leq 8V$ , 11.9mm × 16mm × 3.32mm BGA
<a href="#">LTM8051</a>	Quad 40 $V_{IN}$ Silent Switcher µModule Regulator with Configurable 1.2A Output Array	$3V \leq V_{IN} \leq 40V$ , $0.8V \leq V_{OUT} \leq 8V$ , 6.25mm × 11.25mm × 2.22mm BGA