Quad DC/DC µModule Regulator with Configurable 1.2A Output Array

FEATURES

- Quad Output Step-Down µModule Regulator with 1.2A per Output Channel
- Wide Input Voltage Range: 2.7V to 17V
- 0.6V to 1.8V Output Voltage
- 1.2A DC, Parallelable, Output Current Each Channel
- ±1.5% Total Output Voltage Regulation
- 100% Duty-Cycle Operation
- Current Mode Control, Fast Transient Response
- External Frequency Synchronization
- Selectable Burst Mode® Operation
- Power Good Indicator
- Over Voltage, Current and Temperature Protection
- 6.25mm × 6.25mm × 2.1mm BGA Package
- Pin Compatible with LTM4668A (0.6V to 5.5V Output, 2.25MHz).

APPLICATIONS

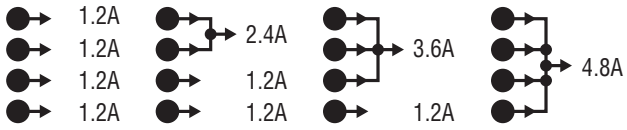
- Telecom, Networking and Industrial Equipment
- Multi-Rail Point of Load Regulation
- FPGAs, DSPs and ASICs Application

DESCRIPTION

The LTM®4668 is a quad DC/DC step-down µModule (micromodule) regulator with 1.2A DC current per output. Outputs can be paralleled in an array for up to 4.8A capability. Included in the package are the switching controllers, power FETs, inductors and support components. Operating over an input voltage range of 2.7V to 17V, the LTM4668 supports an output voltage range of 0.6V to 1.8V. Only bulk input and output capacitors are needed. The device supports frequency synchronization, poly-phase operation, selectable Burst Mode operation, 100% duty cycle and low I_Q operation. Its high switching frequency and a current mode architecture enables a very fast transient response to line and load changes without sacrificing stability.

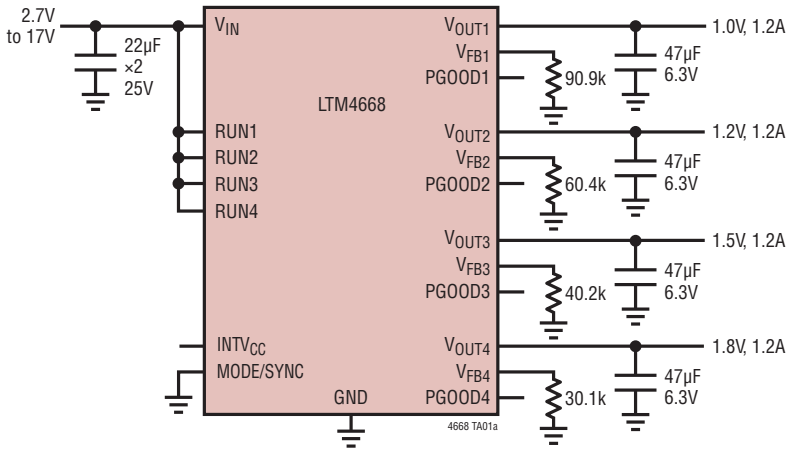
Fault protection features include overvoltage, overcurrent and overtemperature protection. The power module is offered in a space saving and thermally enhanced 6.25mm × 6.25mm × 2.1mm BGA package. The LTM4668 is available with RoHS compliant terminal finish.

Configurable Output Array

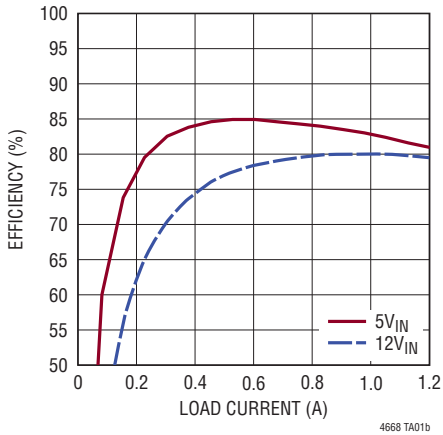


TYPICAL APPLICATION

2.7V to 17V Input, Quad 1.0V, 1.2V, 1.5V, 1.8V Output DC/DC µModule Regulator



1.5V Output Efficiency (Each Channel)



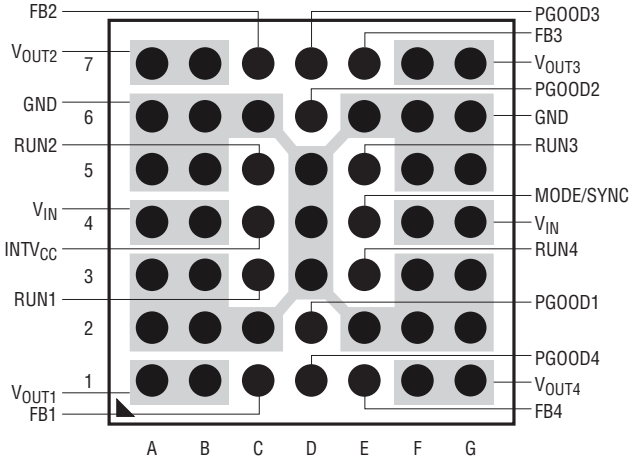
Rev. D

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 17V
V_{OUT} (per Channel) ..... –0.3V to 6V
RUN (per Channel) ..... –0.3V to 17V
$INTV_{CC}$ (Note 3) ..... –0.3V to 6V
PGOOD (per Channel) ..... –0.3V to 6V
FB (per Channel) ..... –0.3V to $INTV_{CC}$
MODE/SYNC ..... –0.3V to $INTV_{CC}$ + 0.3V
Operating Junction Temperature (Note 2) .. –40 to 125°C
Storage Temperature Range ..... –55 to 125°C
Peak Solder Reflow Body Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
49-PIN (6.25mm × 6.25mm × 2.1mm)
T_{JMAX} = 125°C, θ_{JCtop} = 30.5°C/W,
$\theta_{JCbottom}$ = 7.4°C/W, θ_{JA} = 29.3°C/W
WEIGHT = 0.7g
θ VALUES DETERMINED PER JESD51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING	FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
LTM4668EY#PBF	SAC305 (RoHS)	4668 1Y	e1	BGA	4	–40°C to 125°C
LTM4668IY#PBF	SAC305 (RoHS)	4668 1Y	e1	BGA	4	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: (Per Channel)							
V_{IN}	Input DC Voltage		●	2.7		17	V
$V_{OUT(RANGE)}$	Output Voltage Range	V_{IN} = 2.7V to 17V (Step-Down Only)	●	0.6		1.8	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF, C_{OUT} = 47µF Ceramic, R_{FB} = 40.2k, MODE = $INTV_{CC}$/2, V_{IN} = 2.7V to 17V, I_{OUT} = 0A to 1.2A	●	1.477	1.50	1.523	V
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		0.35	0.7	1	V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$/2 (CCM) V_{IN} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$ (Burst) V_{IN} = 12V, V_{OUT} = 1.5V, MODE = GND (PS) Shutdown, RUN = 0, V_{IN} = 12V			50 300 200 1		mA µA µA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 1.2A			0.2		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		1.2	A
$\frac{\Delta V_{OUT}\ (Line)}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 2.7V to 17V, I_{OUT} = 0A	●		0.01	0.1	%/V
$\frac{\Delta V_{OUT}\ (Load)}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 1.2A	●		0.1	0.75	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 47µF Ceramic V_{IN} = 12V, V_{OUT} = 1.5V			7		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			30		mV
t_{START}	Turn-On Time	C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V, No Load			0.8		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			50		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V			2		A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.591	0.60	0.609	V
I_{FB}	Current at V_{FB} Pin	(Note 3)				±10	nA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			60.05	60.40	60.75	kΩ
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			60		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –12	 –8 8	 12	 % %
R_{PGOOD}	PGOOD Resistance				275		Ω
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN} = 6V to 17V		4.7	5	5.3	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Up		2.3	2.5	2.7	V
UVLO(HYS)	UVLO Hysteresis				250		mV
f_{OSC}	Oscillator Frequency				1		MHz
SYNC	SYNC Capture Range			500		1500	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4668 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4668E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4668I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

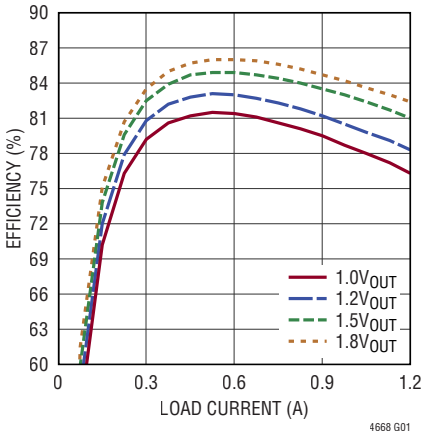
Note 3: 100% tested at wafer level

Note 4: See Thermal Considerations and Output Current Derating for different V_{IN}, V_{OUT} and T_A.

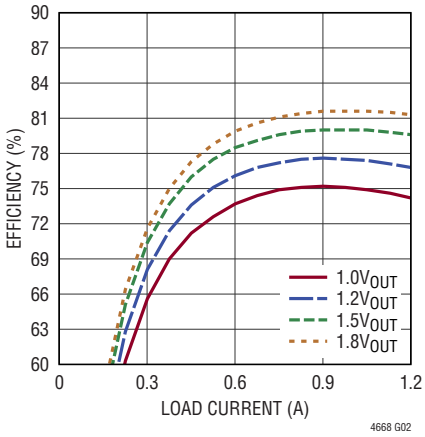
Note 5: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

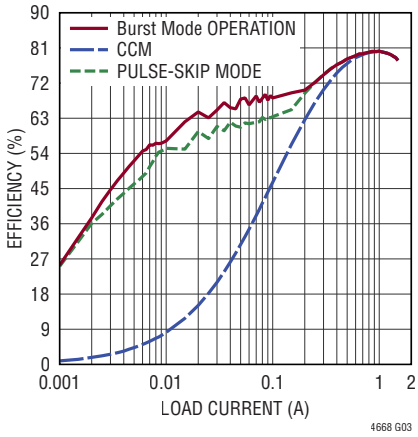
Efficiency vs Load Current at $5V_{IN}$



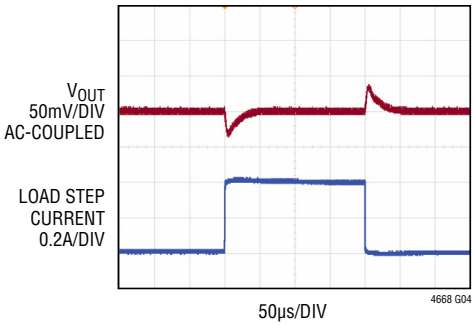
Efficiency vs Load Current at $12V_{IN}$



Burst Mode Operation and Pulse Skip Mode Efficiency, V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 1MHz

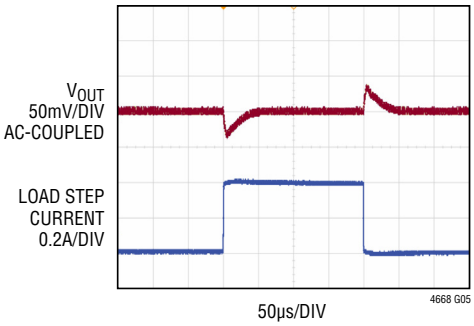


1V Output Transient Response



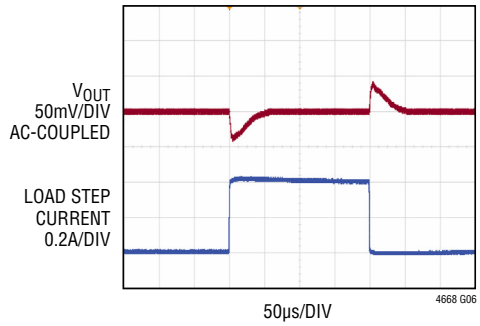
$12V_{IN}$, $1V_{OUT}$, 1MHz
C_{OUT} = 47µF CERAMIC, C_{FF} = 150pF
0.4A LOAD STEP, 10A/µs

1.2V Output Transient Response



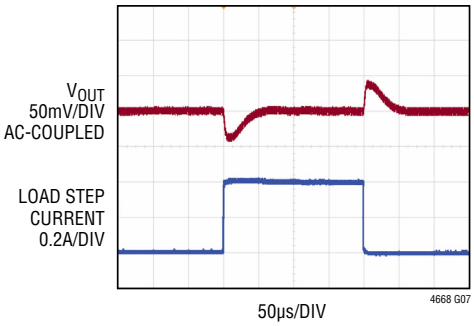
$12V_{IN}$, $1.2V_{OUT}$, 1MHz
C_{OUT} = 47µF CERAMIC, C_{FF} = 150pF
0.4A LOAD STEP, 10A/µs

1.5V Output Transient Response



$12V_{IN}$, $1.5V_{OUT}$, 1MHz
C_{OUT} = 47µF CERAMIC, C_{FF} = 150pF
0.4A LOAD STEP, 10A/µs

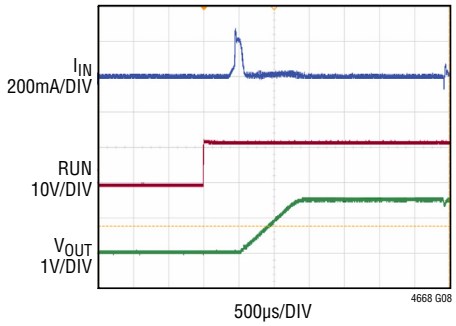
1.8V Output Transient Response



$12V_{IN}$, $1.8V_{OUT}$, 1MHz
C_{OUT} = 47µF CERAMIC, C_{FF} = 150pF
0.4A LOAD STEP, 10A/µs

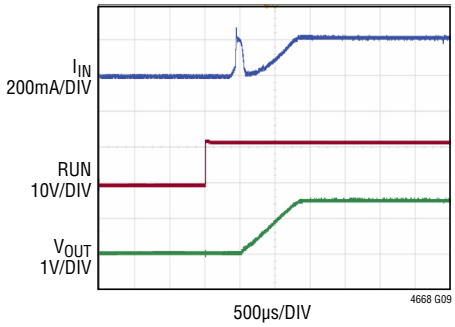
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with No Load



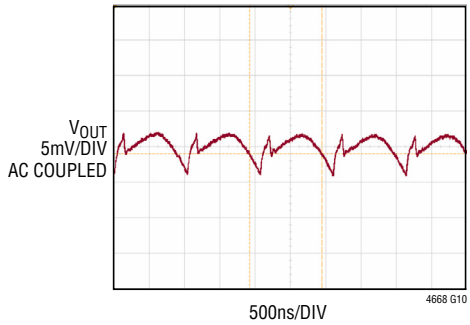
V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 2.0MHz
INPUT CAPACITOR = 2× 22µF + 1× 10µF + 1× 4.7µF CERAMIC
OUTPUT CAPACITOR = 1× 47µF CERAMIC

Start-Up with 1.5A Load



V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 1MHz
INPUT CAPACITOR = 2× 22µF + 1× 10µF + 1× 4.7µF CERAMIC
OUTPUT CAPACITOR = 1× 47µF CERAMIC

Output Ripple



V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 1MHz
INPUT CAPACITOR = 2× 22µF + 1× 10µF + 1× 47µF CERAMIC
OUTPUT CAPACITOR = 1× 47µF CERAMIC
C_{FF} = 150pF

PIN FUNCTIONS

V_{OUT1} (A1, B1), V_{OUT2} (A7, B7), V_{OUT3} (F7, G7), V_{OUT4} (F1, G1): Power Output Pins of each switching mode regulator channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

GND (A2–A3, A5–A6, B2–B3, B5–B6, C2, C6, D3–D5, E2, E6, F2–F3, F5–F6, G2–G3, G5–G6): Power Ground Pins for both Input and Output Returns. Use large PCB copper areas to connect all GND together.

V_{IN} (A4, B4, F4, G4): Power Input Pins connect to the drain of the internal top MOSFET for each switching mode regulator channel and the internal 3.3V regulator for the control circuitry. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of V_{IN} pins and GND pins.

FB1 (C1), FB2 (C7), FB3 (E7), FB4 (E1): The Negative Input of the Error Amplifier for each switching mode regulator channel. Internally, this pin is connected to V_{OUT} of each channel with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase® operation, connect FB pins for all slaves to $INTV_{CC}$ and connect V_{OUT} for all paralleled phases together. See the Applications Information section for details.

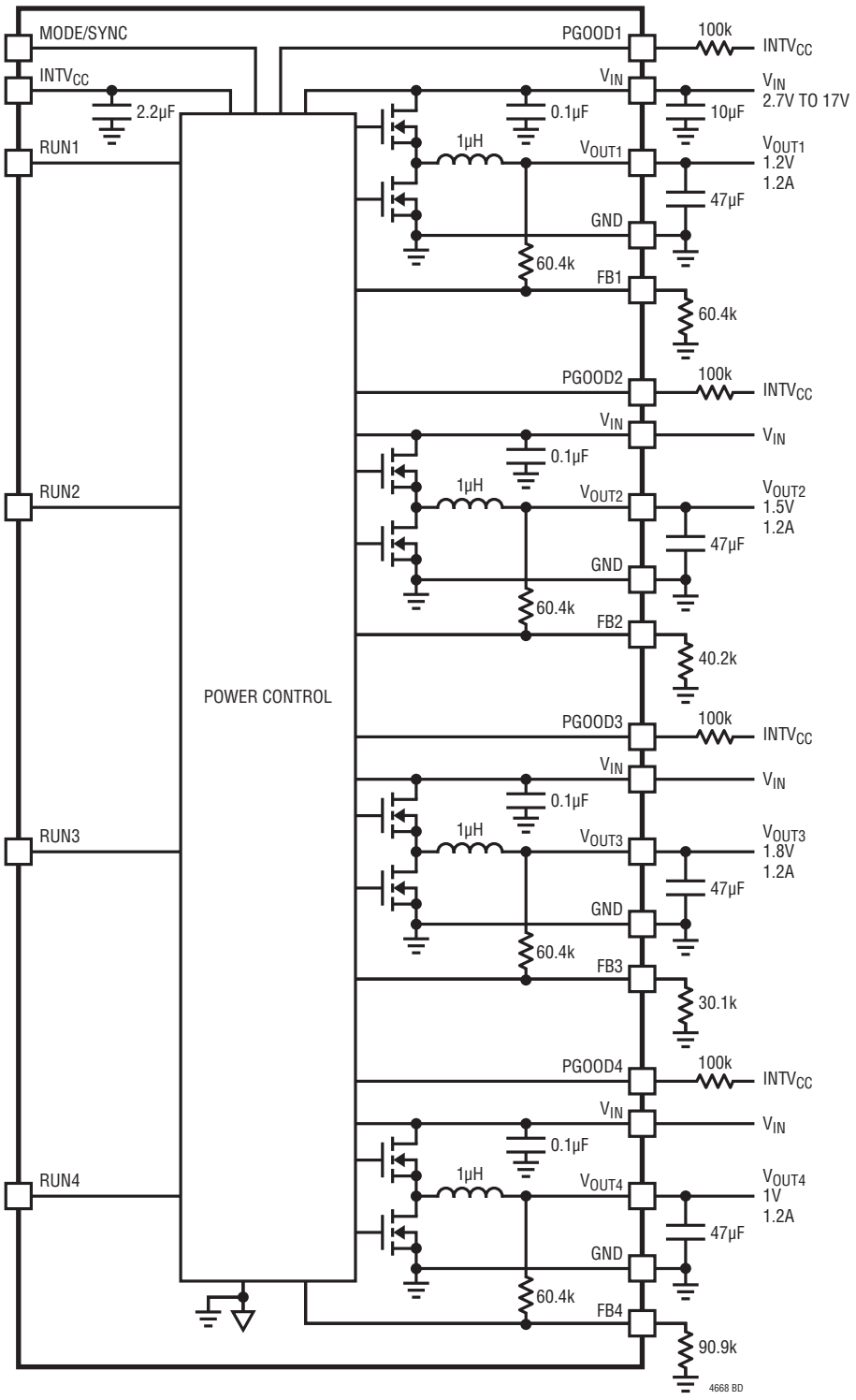
RUN1 (C3), RUN2 (C5), RUN3 (E5), RUN4 (E3): Run Control Input of each switching mode regulator channel. Enable regulator operation by tying the specific RUN pin above 1V. Tying it below 0.35V shuts down the specific regulator channel.

$INTV_{CC}$ (C4): Internal 5V Regulator Output. The internal power drivers and control circuits are powered from this voltage. This pin is internally decoupled to GND with a 2.2µF low ESR ceramic capacitor. No additional external decoupling capacitor is needed. $INTV_{CC}$ only starts up if at least one of the RUN pins is high.

PGOOD1 (D2), PGOOD2 (D6), PGOOD3 (D7), PGOOD4 (D1): Output Power Good with Open-Drain Logic of each switching mode regulator channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±7.5% of the internal 0.6V reference.

MODE/SYNC (E4): Burst Mode Select and External Clock Synchronization of the switching mode regulator. Tie MODE/SYNC to $INTV_{CC}$ for Burst Mode operation with a 400mA peak current clamp. Tie MODE/SYNC to GND for pulse-skipping operation, and tie MODE/SYNC to a voltage between 1V and $INTV_{CC}$ – 1.2V for forced continuous mode. Furthermore, connecting this pin to an external clock will synchronize the switch clock to the external clock and put the part in forced continuous mode. Do not float this pin.

BLOCK DIAGRAM



DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Regulator Section: (Per Channel)						
C_{IN}	External Input Capacitor Requirement (V_{IN} = 2.7V to 17V, V_{OUT} = 1.5V)	I_{OUT} = 1.2A	4.7	10		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 2.7V to 17V, V_{OUT} = 1.5V)	I_{OUT} = 1.2A	22	47		µF

OPERATION

The LTM4668 is a quad output standalone non-isolated switch mode DC/DC power supply. It has built-in four separate regulator channels and each of them can deliver 1.2A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable via a single external resistor over 2.7V to 17V input voltage range. The LTM4668 supports output voltages of 0.6V to 1.8V. The typical application schematic is shown in Figure 17.

The LTM4668 uses a constant frequency, peak current mode architecture and has integrated power MOSFETs, inductors, and other supporting discrete components. The typical switching frequency is set to 1MHz. For switching noise-sensitive applications, the µModule can be externally synchronized to a clock from 500kHz to 1.5MHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4668 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides the flexibility of paralleling any of the separate regulator channels with accurate current sharing. With a built-in clock interleaving between each two regulator channels, the LTM4668 could easily employ a 2+2, 3+1 or 4 channels parallel operation which is more than flexible in a multi-rail POL application.

Current mode control also provides cycle-by-cycle fast overcurrent protection. An internal overvoltage and undervoltage comparator pulls the open-drain PGOOD output low if the output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET is turned off and bottom FET is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 0.35V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, pulse-skipping mode or Burst Mode operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting MODE/SYNC pin to GND or $INTV_{CC}$ accordingly. The LTM4668 has internal 800µs soft-start ramp on each output channel.

The pin compatible µModule part LTM4668A is recommended when operating at a higher output voltage range of 0.6V to 5.5V and has a typical switching frequency of 2.25MHz. The differences between LTM4668 and LTM4668A are shown in Table 1.

Table 1. Recommended Part Selection

	RECOMMENDED V_{OUT} RANGE	SWITCHING FREQUENCY
LTM4668	0.6V to 1.8V	1MHz
LTM4668A	0.6V to 5.5V	2.25MHz

APPLICATIONS INFORMATION

The typical LTM4668 application circuit is shown in Figure 17. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 8 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage due to the minimum on-time limits of each regulator channel. The minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$D_{MIN} = T_{ON(MIN)} \bullet f_{SW}$$

where $T_{ON(MIN)}$ is the minimum on-time, 60ns typical for LTM4668. In the rare cases where the minimum duty cycle is surpassed, the output voltage will remain in regulation, but the switching frequency will decrease from its programmed value.

The LTM4668 is able to run at 100% duty cycle operation. As the duty cycle approaches 100%, the LTM4668 enters dropout operation. During dropout, the top PMOS switch is turned on continuously, and all active circuitry is kept alive.

Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k 0.5% internal feedback resistor connects each regulator channel V_{OUT} and FB pin together. Adding a resistor R_{FB} from FB pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 2. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8
R_{FB}(k)	OPEN	90.9	60.4	40.2	30.1

For parallel operation, a single resistor as determined by the previous equation is used for R_{FB} and is connected from a master channel's FB pin to GND. Tie the FB pins of the slave channels to $INTV_{CC}$ and tie the V_{OUT} pins and the RUN pins together for all channels in parallel. See the Multi-Channel Parallel Operation section.

Input Decoupling Capacitors

The LTM4668 module should be connected to a low AC-impedance DC source. One piece of 4.7µF input ceramic capacitor is required to be placed on each side of the module for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 8 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 0.4A load step transient. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The LTpowerCAD® design tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

APPLICATIONS INFORMATION

Burst Mode Operation

The LTM4668 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply tie the MODE/SYNC pin to $INTV_{CC}$.

During Burst Mode operation, the peak current of the inductor is set to approximately 400mA in normal operation even though the output of the error amplifier (COMP) indicates a lower value. The COMP voltage drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.2V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP voltage to rise, the internal sleep line goes low, and the LTM4668 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

When all channels are in sleep mode, the LTM4668 module draws only 8µA of quiescent current from V_{IN}.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used by grounding the MODE/SYNC pin. In LTM4668, pulse-skipping mode is implemented similarly to Burst Mode operation with the peak inductor current set to be at least 66mA. This results in lower ripple than in Burst Mode operation with the trade-off of slightly lower efficiency.

Both modes, Burst Mode operation and pulse-skipping mode, automatically switch from continuous operation to the selected mode when the load current is low.

Forced Continuous Current Mode (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to $INTV_{CC}/2$. In this mode, inductor current is allowed to reverse during low output loads, the output of the error amplifier is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse.

During start-up, the module operates in pulse-skipped mode regardless of the mode programmed on the MODE/SYNC pin to prevent inductor current from reversing until the LTM4668's output voltage is in regulation.

Operating Frequency

The operating frequency of the LTM4668 is optimized to achieve the compact package size and the minimum output ripple voltage while keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required.

If any operating frequency other than 1MHz is required by application, the µModule can be externally synchronized to a clock from 500kHz to 1.5MHz.

Frequency Synchronization and Clock In

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±50% around the 1MHz set frequency. A pulse detection circuit is used to detect a clock on the MODE/SYNC pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns. The clock high level must be above 2V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled. And once engaged in frequency sync, the LTM4668 runs in forced continuous mode at the external clock frequency.

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Multi-Channel Parallel Operation

For the application that demands more than 1.2A of output current, the LTM4668 multiple regulator channels can be easily paralleled to provide more output current without increasing input and output voltage ripples. The LTM4668 has preset built-in 180° phase shift between channel 1, 2 and 3, 4 which is suitable to employ a 2+2, 3+1 or 4 channel parallel operation. Table 3 gives the phase difference between regulator channels.

Table 3. Phase Difference Between Regulator Channels

CHANNEL	CH1	CH2	CH3	CH4
PHASE DIFF.	0°	180°	0°	

Figure 1 shows a 2+2 and a 4-channels parallel concept schematics for clock phasing.

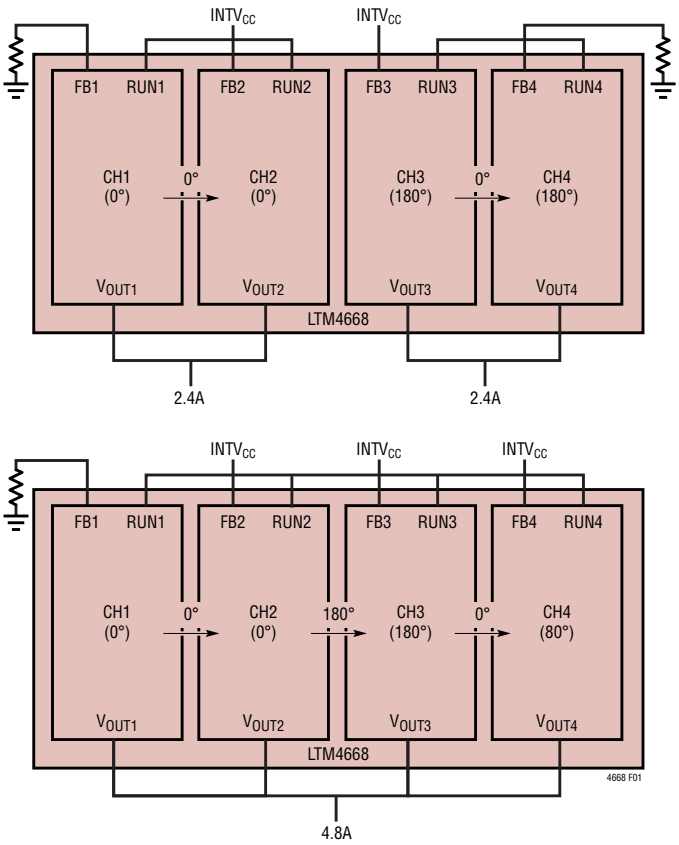

Figure 1. 2+2 and 4-Channel Parallel Concept Schematic

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4668 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. When configuring the LTM4668 for parallel operation, channels 1 and 4 serve as master channels to slave channels 2 and 3, respectively. To configure a channel as a slave, tie its FB pin to $INTV_{CC}$ to shut down its control circuitry. The master channel's drive signal is used instead to drive the slave channel's power switches. Then, to complete configuration, tie its V_{OUT} to the master channel V_{OUT} and its RUN pin to the master channel's RUN pin. Channel 2 and 3 cannot be tied together to provide a dual channel single output. For a three-channel single-output, or four-channel single-output, channel 1 is used as the master channel. Table 4 lists the recommended channel combinations for multi-channel parallel operation. See Figure 18 and Figure 19 for paralleling operation. In parallel operation, use the master channel's PGOOD signal as the power good indicator. Do not tie PGOOD pins together.

Table 4. Configuration of Multi-Channel Parallel Operation

NUMBER OF OUTPUT VOLTAGE RAILS	PARALLELING CHANNEL	MASTER CHANNEL	POWER GOOD INDICATOR
QUAD	1/2/3/4		
TRIPLE	1+2/3/4	1	PGOOD1
DUAL	1+2/3+4	1, 4	PGOOD1,4
DUAL	1+2+4/3	1	PGOOD1
SINGLE	1+2+3+4	1	PGOOD1

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and

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a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 2 shows this graph.

Soft-Start and Output Voltage Tracking

The LTM4668 has an internal 800µs soft-start ramp for each channel. During soft-start operation, the switcher operates in pulse-skipping mode regardless of the mode programmed on the MODE/SYNC pin. Once the soft-start period is complete, the part will transition into the desired mode of operation.

Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±7.5% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4668's PGOOD falling edge includes a blanking delay of approximately 32 switching cycles.

Stability Compensation

The LTM4668 module internal compensation loop of each regulator channel is designed and optimized for low ESR ceramic output capacitors only application. Table 6 is provided for most application requirements. In cases that require bulk output capacitors for output ripple or dynamic transient spike reduction, an additional 10pF to 15pF phase boost cap is required between V_{OUT} and FB pins. The LTpowerCAD design tool is available to download for control loop optimization.

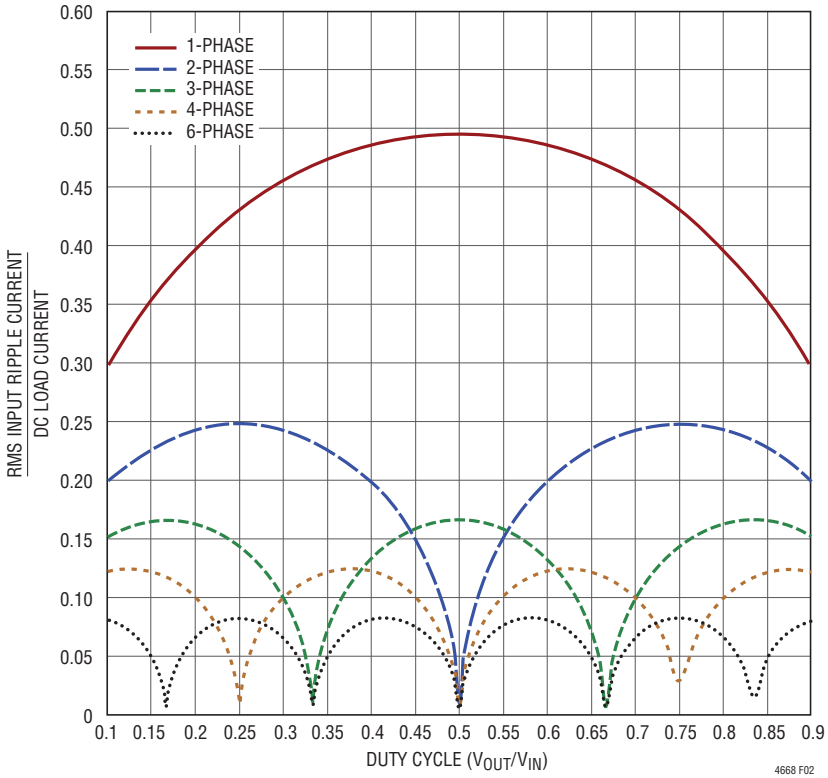

Figure 2. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

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Run Enable

Pulling the RUN pin of each regulator channel to ground forces the regulator into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 1V will turn on the entire regulator channel.

V_{IN} Overvoltage Protection

The LTM4668 module constantly monitors the V_{IN} pins for an overvoltage condition. When V_{IN} rises above 19V, the corresponding regulator suspends operation by shutting off both power MOSFETs. Once V_{IN} drops below 18.7V, the regulator immediately resumes normal operation. The regulators execute soft-start function when exiting an overvoltage condition.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

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A graphical representation of the aforementioned thermal resistances is given in Figure 3; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

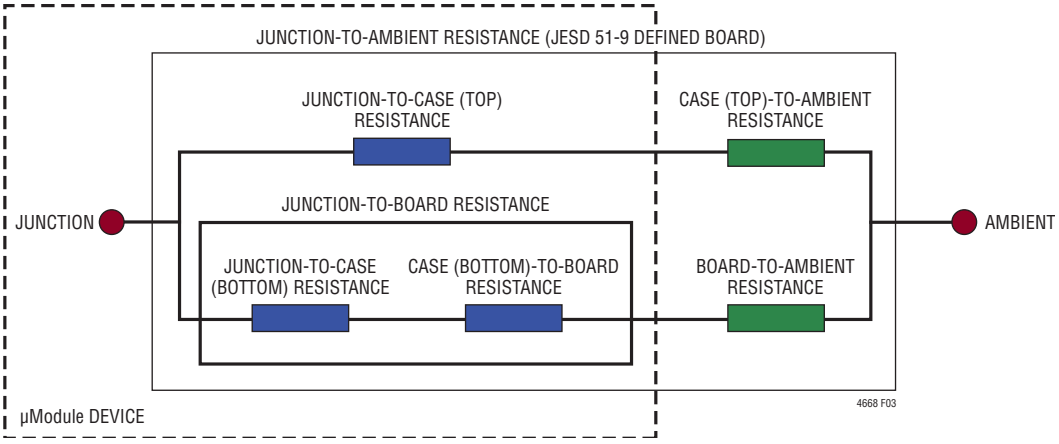

Figure 3. Graphical Representation of JESD51-12 Thermal Coefficients

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The 0.8V, 1.2V and 1.8V power loss curves in Figure 4 to Figure 6 can be used in coordination with the load current derating curves in Figure 7 to Figure 15 for calculating an approximate θ_{JA} thermal resistance for the LTM4668 with various airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.3 considering both MOSFET $R_{DS(ON)}$ and inductor DCR increases at 120°C junction temperature when the derating starts. The derating curves are plotted with the output current starting at 4.8A with all 4 channels paralleled together and the ambient temperature at 30°C. The output voltages are 0.8V, 1.2V and 1.8V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 13 the load current is derated to ~4.5A at ~90°C with no air or heat sink and the power loss for the 12V to 0.8V at 4.5A output is about 2W. The 2W loss is calculated with the ~1.5W room temperature loss from the 12V to 0.8V power loss curve at 4.5A, and the 1.3 multiplying factor at 120°C junction. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided by 2W equals a 15°C/W θ_{JA} thermal resistance. Table 5 specifies a 15°C/W value which is very close. Table 5 to Table 7 provide equivalent thermal resistances for 0.8V, 1.2V and 1.8V outputs with and without airflow. The derived thermal resistances in Table 5 and Table 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick six layer board with two ounce copper for the two outer layers and one ounce copper for the four inner layers. The PCB dimensions are 94mm × 100mm.

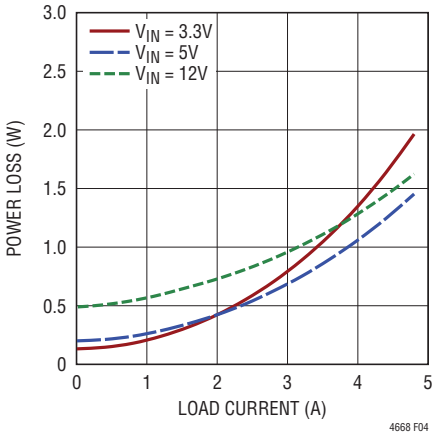


Figure 4. 0.8V Output Power Loss

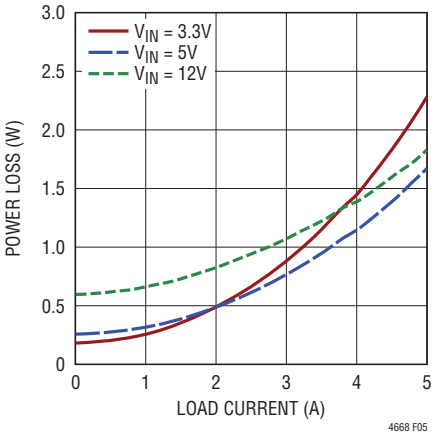


Figure 5. 1.2V Output Power Loss

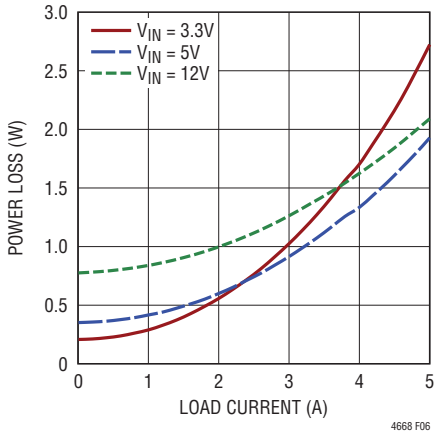


Figure 6. 1.8V Output Power Loss

APPLICATIONS INFORMATION

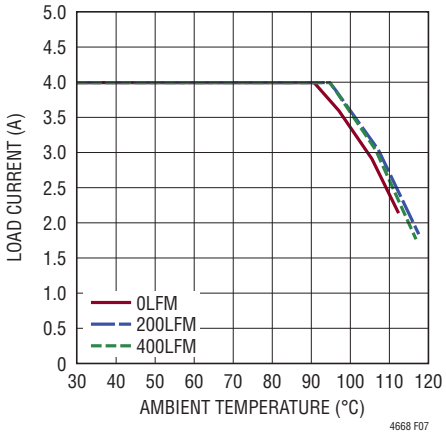


Figure 7. 3.3V to 0.8V Derating Curve, No Heat Sinking

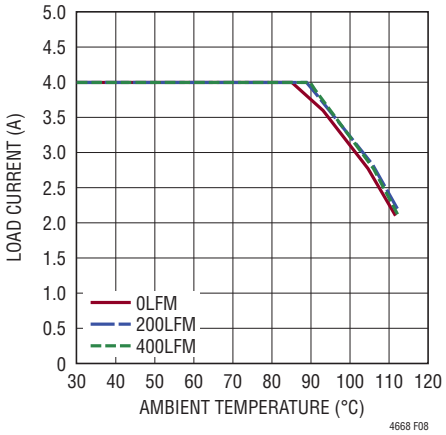


Figure 8. 3.3V to 1.2V Derating Curve, No Heat Sinking

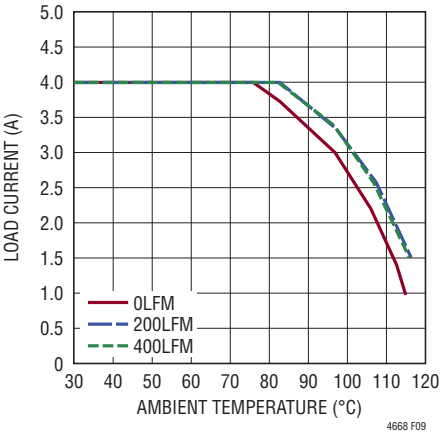


Figure 9. 3.3V to 1.8V Derating Curve, No Heat Sinking

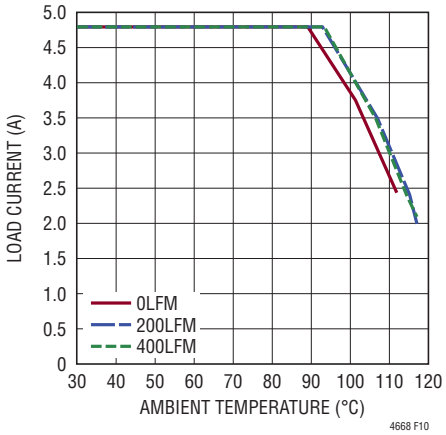


Figure 10. 5V to 0.8V Derating Curve, No Heat Sinking

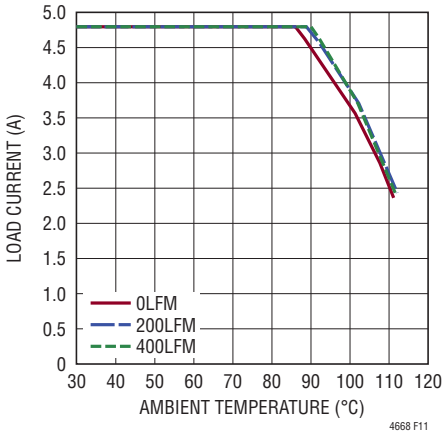


Figure 11. 5V to 1.2V Derating Curve, No Heat Sinking

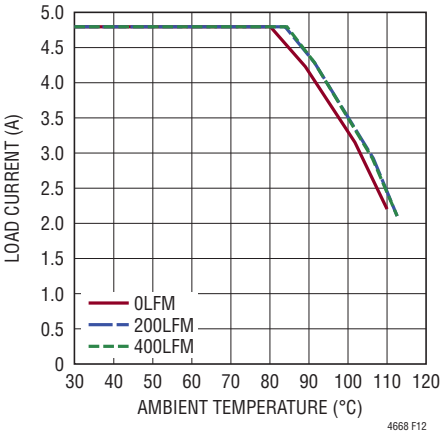


Figure 12. 5V to 1.8V Derating Curve, No Heat Sinking

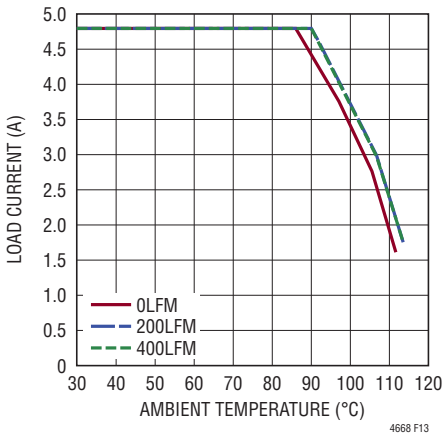


Figure 13. 12V to 0.8V Derating Curve, No Heat Sinking

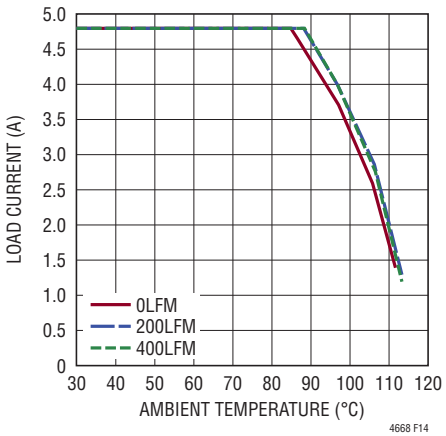


Figure 14. 12V to 1.2V Derating Curve, No Heat Sinking

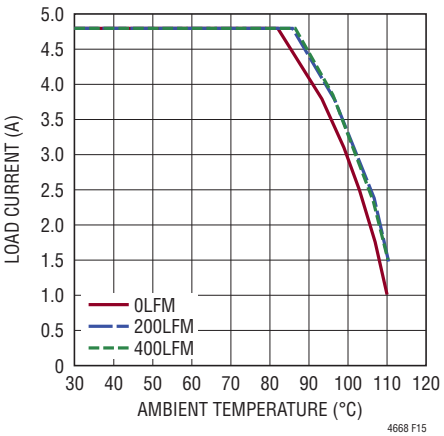


Figure 15. 12V to 1.8V Derating Curve, No Heat Sinking

APPLICATIONS INFORMATION

Table 5. 0.8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 7, 10, 13	3.3, 5, 12	Figure 4	0	None	15
Figures 7, 10, 13	3.3, 5, 12	Figure 4	200	None	13
Figures 7, 10, 13	3.3, 5, 12	Figure 4	400	None	12

Table 6. 1.2V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figures 8, 11, 14	3.3, 5, 12	Figure 5	0	None	15
Figures 8, 11, 14	3.3, 5, 12	Figure 5	200	None	13
Figures 8, 11, 14	3.3, 5, 12	Figure 5	400	None	12

Table 7. 1.8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figures 9, 12, 15	3.3, 5, 12	Figure 6	0	None	15
Figures 9, 12, 15	3.3, 5, 12	Figure 6	200	None	13
Figures 9, 12, 15	3.3, 5, 12	Figure 6	400	None	12

Table 8. Output Voltage Response vs Component Matrix (See Typical Performance Characteristics) 0A to 0.4A Load Step Typical Measured Values

C_{IN} CERAMIC VENDORS	VALUE	PART NUMBER	C_{OUT} CERAMIC VENDORS	VALUE	PART NUMBER
MURATA	22µF, 25V	GRM21BR61E226ME44L	MURATA	47µF, 6.3V	GRM21BR60J476ME15
TAIYO YUDEN	22µF, 25V	TMK316BBJ226ML-T	TAIYO YUDEN	47µF, 6.3V	JMK212BJ476MG-T

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	RFB (kΩ)
1	10µF		47µF		150	5, 12	0	75	50	0.4	10	90.9
1.2	10µF		47µF		150	5, 12	0	76	50	0.4	10	60.4
1.5	10µF		47µF		150	5, 12	0	84	50	0.4	10	40.2
1.8	10µF		47µF		150	5, 12	0	86	50	0.4	10	30.1

APPLICATIONS INFORMATION

Safety Considerations

The LTM4668 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

Layout Checklist/Example

The high integration of LTM4668 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, and respective V_{OUTS}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel operation, tie the V_{OUTS} and RUNs together, and the subordinate channels are connected to $INTV_{CC}$. See Figure 1 for explanation.
- Bring out test points on the signal pins for monitoring.

Figure 16 gives a good example of the recommended layout.

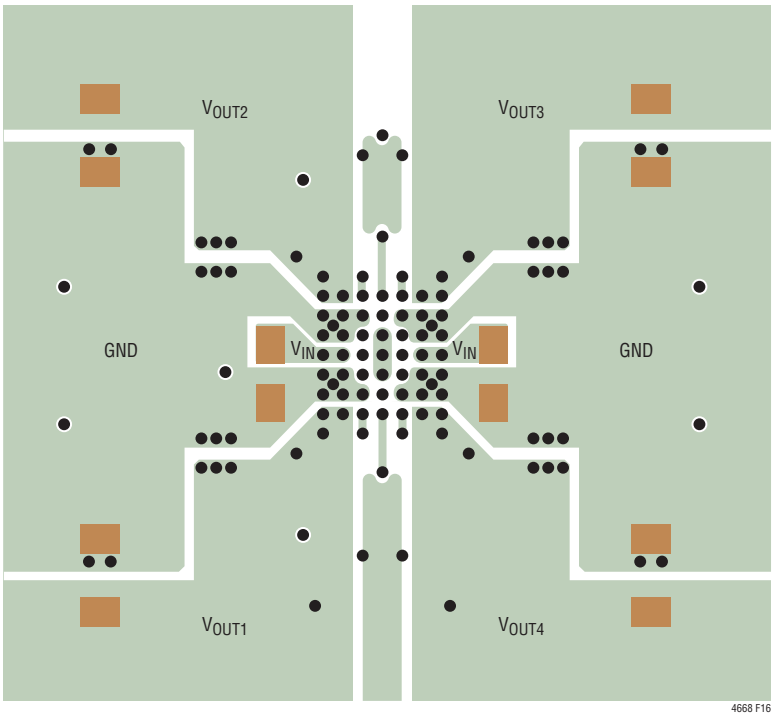


Figure 16. Recommended PCB Layout

TYPICAL APPLICATIONS

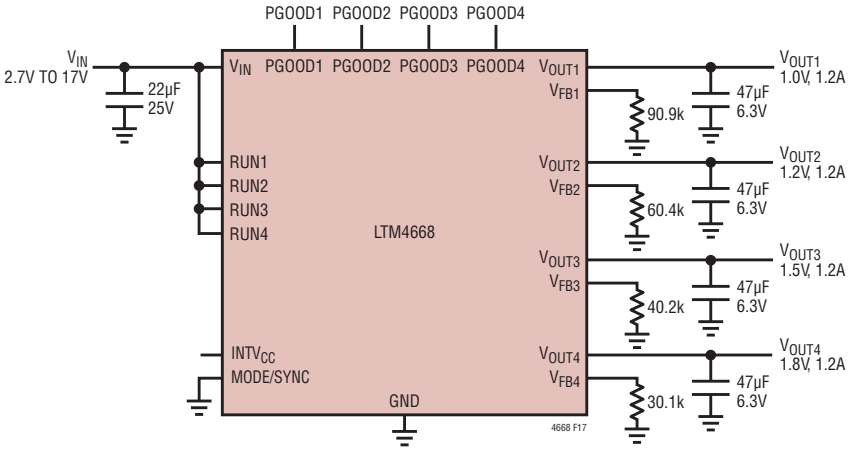


Figure 17. 2.7V to 17V Input, 1V, 1.2V, 1.5V, 1.8V Output at 1.2A Design

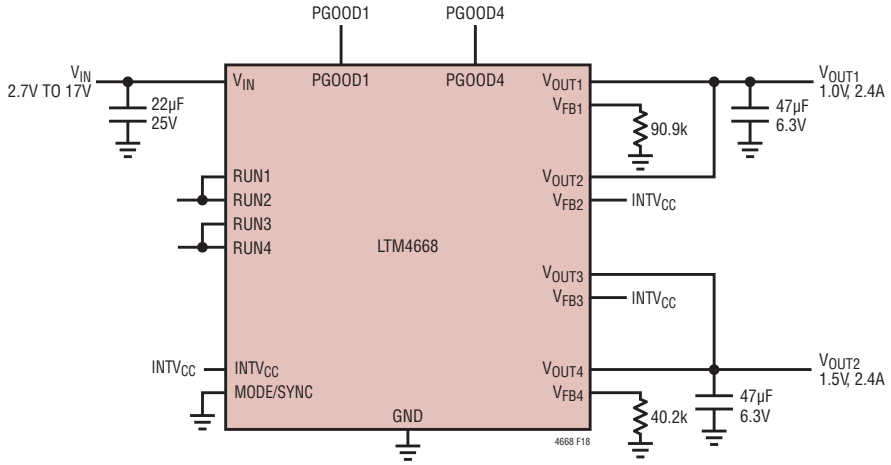


Figure 18. 2.7V to 17V Input, 1V and 1.5V Output at 2.4A

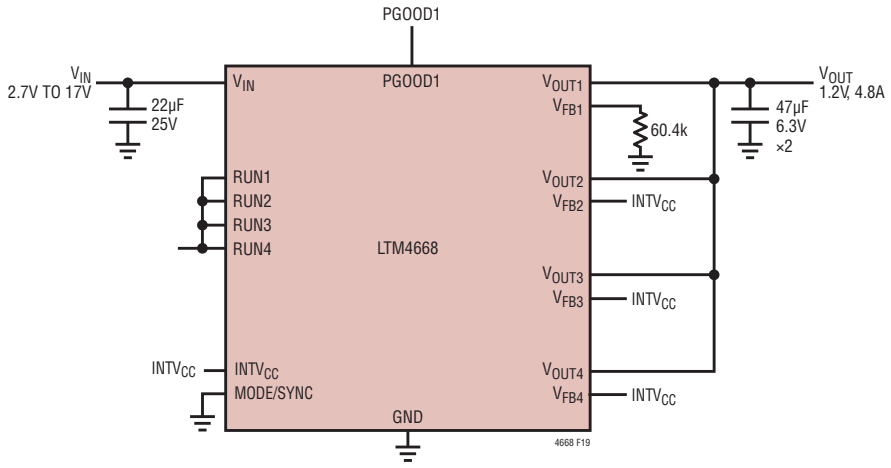


Figure 19. 2.7V to 17V Input, Four Phase Parallel Single Output 1.2V at 4.8A Design

PACKAGE DESCRIPTION

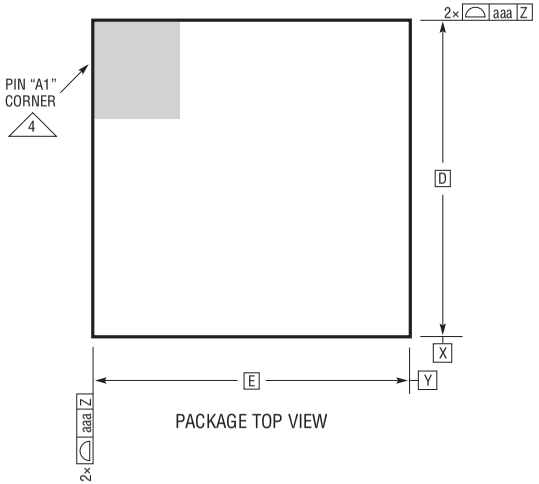
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 9. LTM4668 Component LGA/BGA Pinout

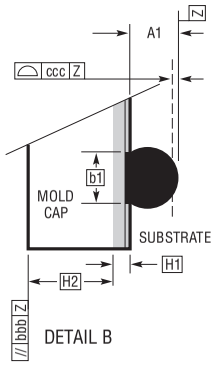
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	V_{OUT1}	B1	V_{OUT1}	C1	FB1	D1	PGOOD4	E1	FB4	F1	V_{OUT4}	G1	V_{OUT4}
A2	GND	B2	GND	C2	GND	D2	PGOOD1	E2	GND	F2	GND	G2	GND
A3	GND	B3	GND	C3	RUN1	D3	GND	E3	RUN4	F3	GND	G3	GND
A4	V_{IN}	B4	V_{IN}	C4	$INTV_{CC}$	D4	GND	E4	MODE/SYNC	F4	V_{IN}	G4	V_{IN}
A5	GND	B5	GND	C5	RUN2	D5	GND	E5	RUN3	F5	GND	G5	GND
A6	GND	B6	GND	C6	GND	D6	PGOOD2	E6	GND	F6	GND	G6	GND
A7	V_{OUT2}	B7	V_{OUT2}	C7	FB2	D7	PGOOD3	E7	FB3	F7	V_{OUT3}	G7	V_{OUT3}

PACKAGE DESCRIPTION

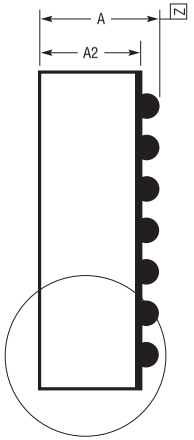
BGA Package
49-Lead (6.25mm × 6.25mm × 2.10mm)
(Reference LTC DWG# 05-08-1600 Rev Ø)



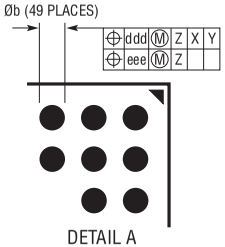
PACKAGE TOP VIEW



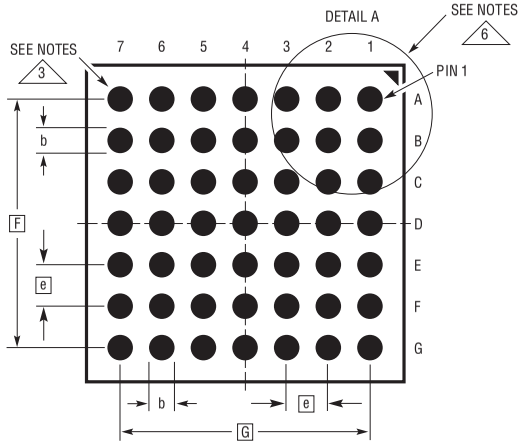
DETAIL B



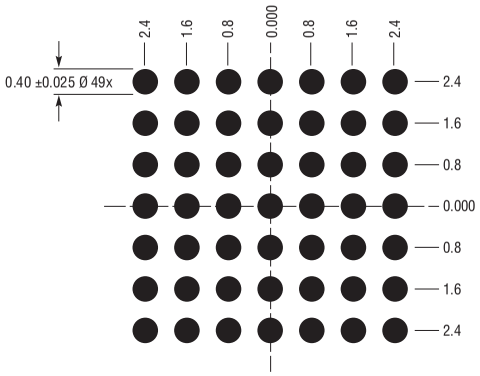
DETAIL B
PACKAGE SIDE VIEW



DETAIL A



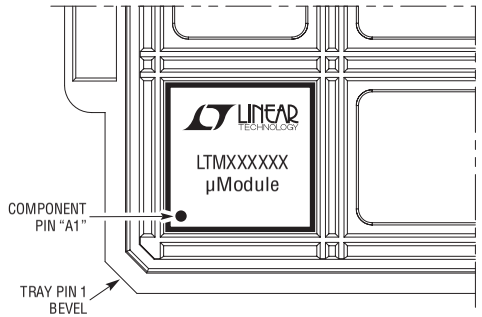
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	1.90	2.10	2.30	
A1	0.30	0.40	0.50	BALL HT
A2	1.60	1.70	1.80	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		6.25		
e		0.80		
F		4.80		
G		4.80		
H1		0.20		SUBSTRATE THK
H2		1.50		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 49				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

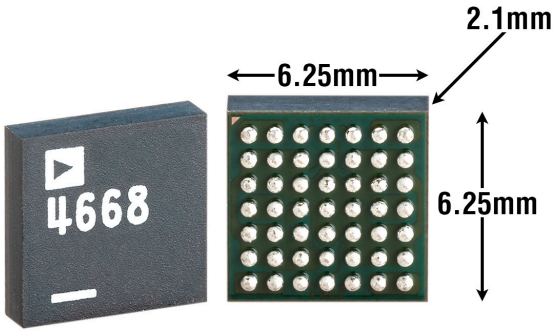
BGA 49 0917 REV Ø

REVISION HISTORY

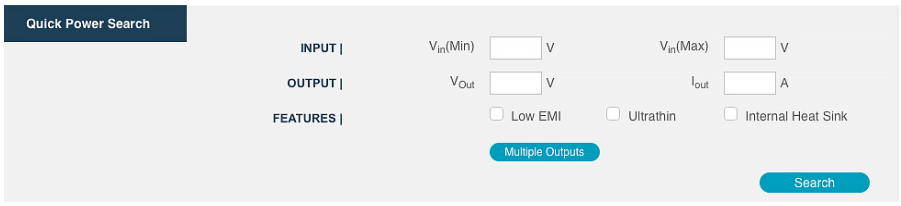
REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/20	Added ground symbol to Typical Application schematics.	1
		MODE/SYNC pin description: Added “Do not float this pin”.	5
		$INTV_{CC}$ pin description: Added “$INTV_{CC}$ only starts up if at least one of the RUN pins is high”.	5
		Added clarification on PGOOD in multi-channel applications.	10
		Edited Figure 17 and 18.	18
		Edited Figure 19.	18
B	08/21	Edited description of $\theta_{JCbottom}$ on Thermal Considerations and Output Current Derating.	12
C	06/22	Updated Part Marking in the Order Information table.	2
		Added ink marking statement to package photos.	22
D	2/24	Updated PGOOD Trip Level range (PCN 23_0160).	3
		Updated Electrical Characteristics, Note 4.	3
		Reorganized Pin Functions alphanumerically.	7
		Updated Table 1 Title.	7
		Minimum on-time corrected from 40ns to 60ns.	10
		Updated Table 8 Title.	16
		Layout Checklist/Example for parallel operation updated.	19

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4622	Ultrathin, Dual 2.5A or Single 5A Step-Down µModule Regulator	$3.6V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4622A	Higher V_{OUT} of LTM4622	$3.6V \le V_{IN} \le 20V$, $1.2V \le V_{OUT} \le 12V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4623	Ultrathin, Single 3A Step-Down µModule Regulator	$4V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4624	Single 4A Step-Down µModule Regulator	$4V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 5.01mm BGA
LTM4625	Single 5A Step-Down µModule Regulator	$4V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 5.01mm BGA
LTM4632	Ultrathin, Triple ±3A Step-Down µModule Regulator for DDR Memory	$3.6V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 2.5V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4643	Ultrathin, Quad 3A Step-Down µModule Regulator	$4V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 3.3V$, 9mm × 15mm × 1.82mm LGA, 9mm × 15mm × 2.42mm BGA
LTM4644	Quad 4A Step-Down µModule Regulator	$4V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, 9mm × 15mm × 5.01mm BGA