Evaluating the ADAU1861 Three ADCs, One DAC, Low Power Codec with Audio DSPs

EVALUATION KIT CONTENTS

- EVAL-ADAU1861EBZ evaluation board
- USB cable with Micro-USB plug

DOCUMENTS NEEDED

- ADAU1861 data sheet
- EVAL-ADAU1861EBZ user guide

SOFTWARE NEEDED

- Lark Studio GUI tool

GENERAL DESCRIPTION

This user guide details the design and setup of the EVAL-ADAU1861EBZ evaluation board. The EVAL-ADAU1861EBZ provides all the analog and digital inputs and outputs on the ADAU1861. The ADAU1861 core is controlled by Analog Devices, Inc., Lark Studio graphical user interface (GUI) software, which interfaces with the EVAL-ADAU1861EBZ by a USB connection.

The EVAL-ADAU1861EBZ can be powered by the USB bus or by a single 12 V supply. Any of these supplies are regulated to the voltages required on the EVAL-ADAU1861EBZ.

The printed circuit board (PCB) of the EVAL-ADAU1861EBZ is a 4-layer design, with a ground plane and a power plane on the inner layers. The EVAL-ADAU1861EBZ contains connectors for external microphones and speakers. The main clock of ADAU1861 can be provided externally or by the on-board 24.576 MHz oscillator or crystal.

The EVAL-ADAU1861EBZ contains a microphone array, aim for beamforming. A 16-channel, high performance, 192 kHz, 24-bit digital-to-analog converter (DAC) is used as the analog output for audio tuning. For compatibility with 3.3 V inputs and outputs, all digital audio interfaces can be transferred to 3.3 V inputs and outputs from 1.8 V with a level shifter.

For full details on the ADAU1861, see the ADAU1861 data sheet, which must be consulted with this user guide when using the EVAL-ADAU1861EBZ evaluation board.

EVAL-ADAU1861EBZ BOARD PHOTOGRAPH

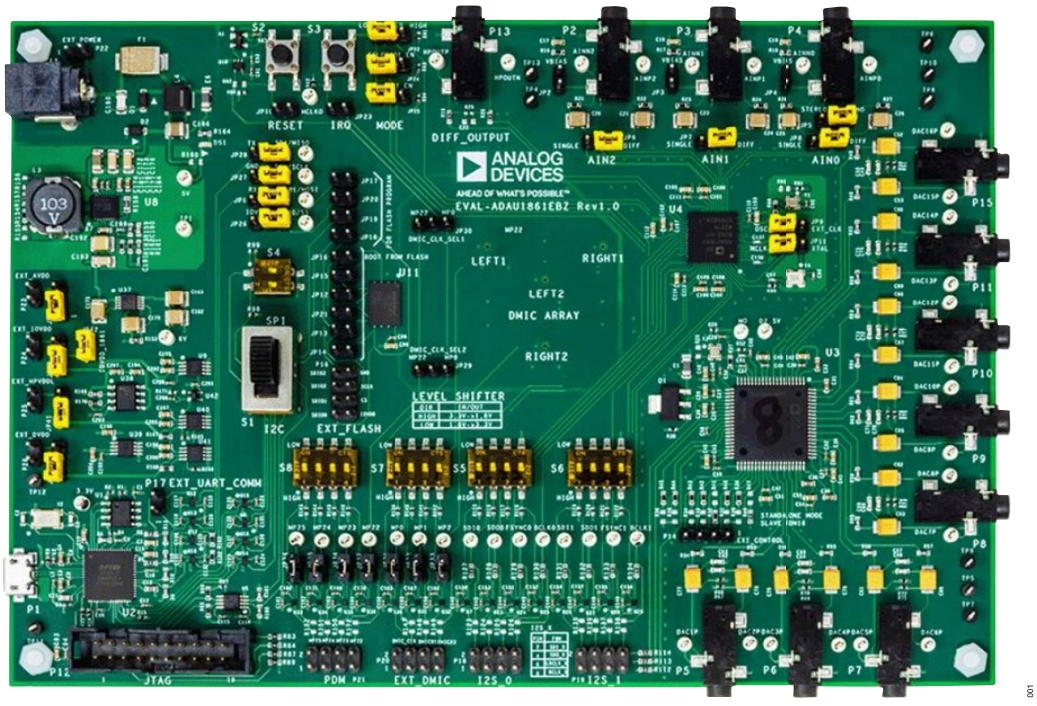

Figure 1. EVAL-ADAU1861EBZ Board Photograph

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REVISION HISTORY

1/2023—Revision 0: Initial Version

EVAL-ADAU1861EBZ BLOCK DIAGRAM

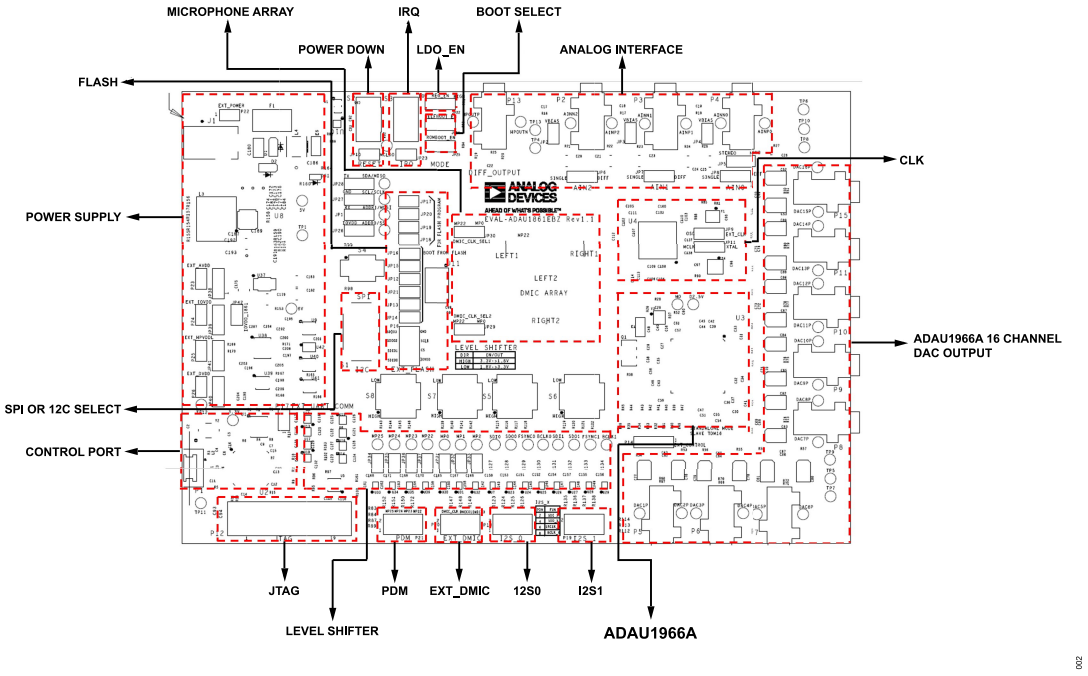

Figure 2. EVAL-ADAU1861EBZ Block Diagram

SETTING UP THE EVAL-ADAU1861EBZ EVALUATION BOARD

INSTALLING THE LARK STUDIO SOFTWARE

Take the following steps to download and install the latest version of the Lark Studio GUI tool:

1. Go to the ADAU1861 web page and download the latest version of the Lark Studio GUI tool found within the **Software & Systems Requirements** section.
2. Download the latest version of the Lark Studio zip file and run the **lark_studio** executable file within. Follow the prompts, including accepting the license agreement, to install the software.

INSTALLING THE USB DRIVERS

If the USB interface is not recognized by the **Lark Studio** GUI tool software and the PC, go to the Future Technology Devices International (FTDI) Limited chip official web page and download the relevant drivers.

DEFAULT SWITCH AND JUMPER SETTINGS

Table 1 shows the default switch and jumper settings.

Table 1. Default Switch and Jumper Settings

Jumper and Switch Connections	Option Selected
Pin 2 to Pin 3 of JP5	The P4 interface works in mono mode with ADC0
Pin 1 to Pin 2 of JP6	ADC2 differential mode
Pin 1 to Pin 2 of JP7	ADC1 differential mode
Pin 1 to Pin 2 of JP8	ADC0 differential mode
Pin 1 to Pin 2 of JP9 and Pin 1 to Pin 2 of JP11	Use JP9 and JP11 as the main clock (24.576 MHz oscillator) source paths
Pin 1 to Pin 2 of JP22	REG_EN disabled and DVDD supplied with on-board LDO
Pin 1 to Pin 2 of JP24	SELFBOOT disabled
Pin 1 to Pin 2 of JP25	ROM_BOOT_MODE disabled
Pin 1 to Pin 2 of JP38 and Pin 2 to Pin 3 of JP39	AVDD and IOVDD supplied by the 1.8 V on-board low-dropout (LDO) regulator (JP38 and JP39)
Pin 2 to Pin 3 of JP40	DVDD supplied by the 0.9 V on-board LDO regulator
Pin 2 to Pin 3 of JP41	HPVDDL supplied by the 1.3 V on-board LDO regulator
JP42 connected	IOVDD_1861 supplied with an IOVDD on-board LDO regulator
Pin 1 to Pin 2 of JP1, Pin 1 to Pin 2 of JP26, Pin 1 to Pin 2 of JP27, Pin 1 to Pin 2 of JP28	I^2C and SPI communication
S1 Up (SPI)	SPI communication
Pin 1 of S4 to GND and Pin 2 of S4 to GND	Set I^2C address
Pin 1 of S5 to GND and Pin 2 of S5 to GND, Pin 3 of S5 to GND and Pin 4 of S5 to GND	I2S0 port, 1.8 V to 3.3 V
Pin 1 of S6 to GND and Pin 2 of S6 to GND, Pin 3 of S6 to GND and Pin 4 of S6 to GND	I2S1 port, 1.8 V to 3.3 V
Pin 1 of S7 to GND and Pin 2 of S7 to GND, Pin 3 of S7 to GND and Pin 4 of S7 to GND	DMIC port, 1.8 V to 3.3 V
Pin 1 of S8 to GND and Pin 2 of S8 to GND, Pin 3 of S8 to GND and Pin 4 of S8 to GND	PDM port, 1.8 V to 3.3 V

SETTING UP COMMUNICATION IN SOFTWARE

POWERING UP THE EVAL-ADAU1861EBZ EVALUATION BOARD

To power up the EVAL-ADAU1861EBZ evaluation board, connect the ribbon cable to P1 of the EVAL-ADAU1861EBZ.

CONNECTING THE AUDIO CABLES

Three channels of the microphone inputs support both differential and single-end modes. The headphone output is differential and is dc-coupled. The digital audio signal can be I^2S or time division multiplexing (TDM) mode through the serial audio interface.

CREATING A BASIC SIGNAL FLOW

To create a basic signal flow in LARK Studio, follow these steps:

1. Download and install Lark Studio from www.analog.com/ADAU1861.
2. Double click the **Lark Studio** shortcut on the PC desktop.
3. Go to the **Project** and select **New Project** from the **dropdown** menu, or select **Create a New Project** in the **Welcome** section to create a new project, as shown in Figure 3. The **New Project** window shows the **Project Type:** options.
4. Select the **Lark** option for the ADAU1861 and then **OK**.
5. Edit the file name and save the file to a user-specified location.
6. Click **Target Connection** in the left navigation panel, and configure the **Connection settings** panel that opens on the right to set up the connection. If the USB connects, **Target Connected** displays (see Figure 4).

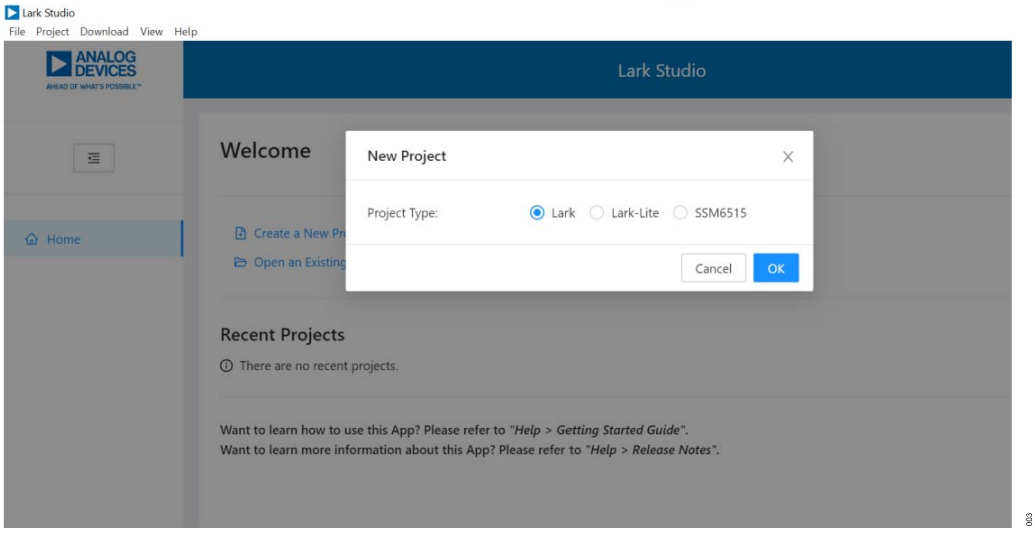

Figure 3. Create a New Project

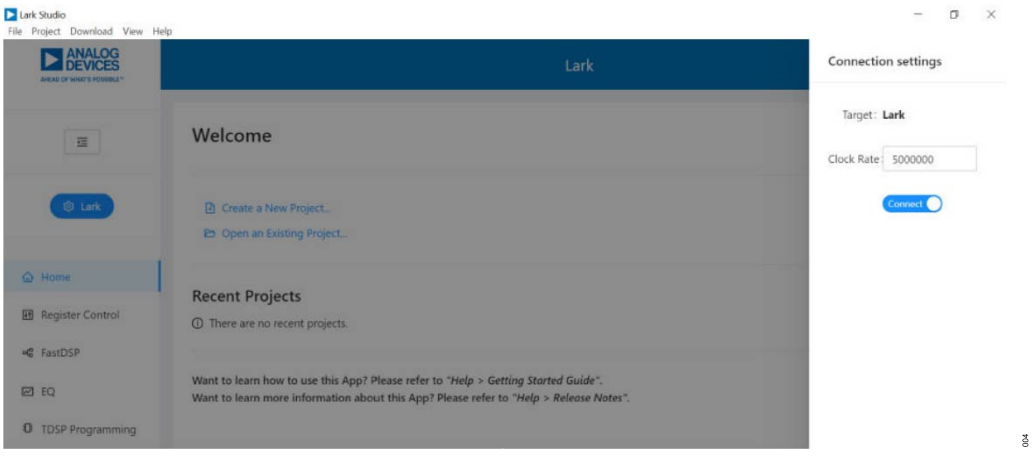

Figure 4. Connect with EVAL-ADAU1861EBZ

SETTING UP COMMUNICATION IN SOFTWARE

Configure the **Register Control**, **FastDSP**, and **EQ** settings on the left navigation panel. **Lark Register Control** has multiple tabs that control different sections of the ADAU1861. Figure 5 shows the **Power** tab, which allows the user to power up or power down various blocks within the ADAU1861. When a block is powered up, that block can be configured.

The **Clock** tab allows the phase-locked loop (PLL) to be used or bypassed. By register default, the PLL is disabled to save power. To generate a 24.576 MHz main clock, enable or disable the PLL according to the provided clock source. On the EVAL-ADAU1861EBZ evaluation board, a 24.576 MHz oscillator and a crystal with same frequency are supplied. To configure an application, take the following steps:

1. Select **Hibernate1**, **BLOCKS_ON**, and **CM_BST_ON** in the **CHIP_PWR** block in the **Power** tab, and then click **Write** (see Figure 5).
2. With the default 24.576 MHz oscillator on board, within the **Clock** tab, select **MCLK_FREQ_24P576** within the **MCLK_FREQ_INDEX** dropdown menu and select **PLL_FM_BP** within the **PLL_FM_BYPASS** dropdown menu, and then click **Write**.
3. Configure the other blocks.

When a register value is changed, click the related **Write** button in the block to update a single register, or click the **Write this Page** button below the tabs to update multiple registers. It is best practice to click **Write All** after all register changes to avoid a configuration error.

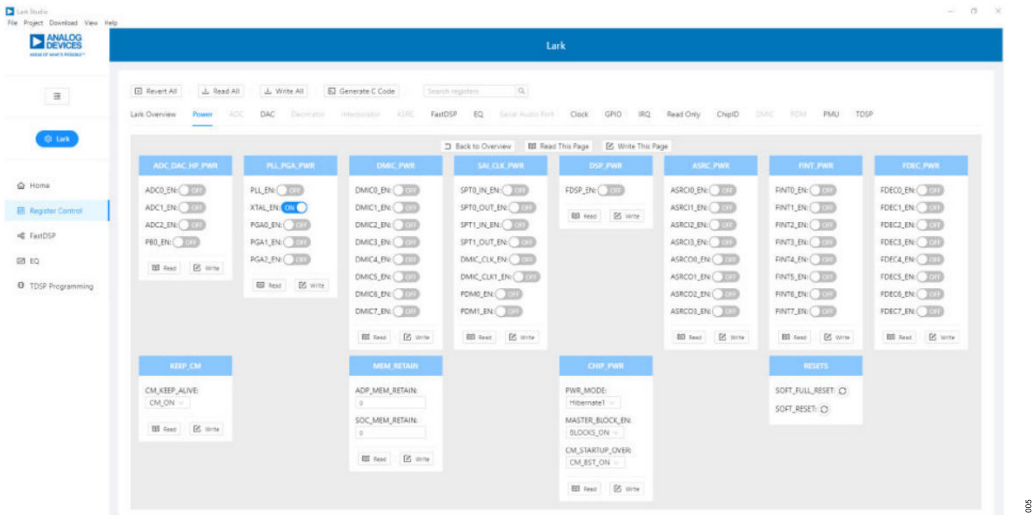

Figure 5. Register Configurations

SETTING UP COMMUNICATION IN SOFTWARE

If FastDSP is required in the project, a schematic must be created with the desired path for the ADAU1861 as follows:

1. Click **FastDSP** in the left navigation panel.
2. In the left pane of the **Lark FastDSP Schematic** window, click an arrow to expand a folder.
3. Select and drag an icon into the schematic window, for example, the **ADC** icon within the **IO** folder (see Figure 6). In this example, AIN1 and ASRCI0 are being routed to FastDSP **Output 0** and **Output 1** separately.
4. To download the correct parameter generated from the schematic, set **fs** to be the same as the FastDSP source, **FDSP_RATE_SOURCE**, which is set in the **FastDSP** tab in the **Lark Register Control** window.
5. Click **Download to Target** to write the parameter and command to the FastDSP memory. After the download finishes, FastDSP is enabled and runs automatically.

If an equalizer is required in the project, a configuration of the filters must be set for the ADAU1861 as follows:

1. Select **EQ** in the navigation panel.
2. Select the filter numbers and relative filter parameters.
3. Set **fs**the same as the equalizer source, **EQ_ROUTE**, which is set in the **EQ** tab in the **Lark RegisterControl** window.
4. Click **Download to Target** to write the parameter and command to the equalizer memory. After the download finishes, the equalizer is enabled and runs automatically.

If Tensilica HiFi 3z DSP (TDSP) is used, a hex file for the TDSP program code can be uploaded by using Lark Studio as follows:

1. Select **TDSP Programming** in the navigation panel.
2. Select the hex file to upload.
3. Click **TDSP Program**.
4. After uploading is finished, type in the **Reset Address** for the program, and then click **TDSP Reset**. The TDSP then runs automatically with the uploaded program.

For full details on the operation of Lark Studio, click **Getting Start Guide** within the **Help** menu of the Lark Studio GUI.

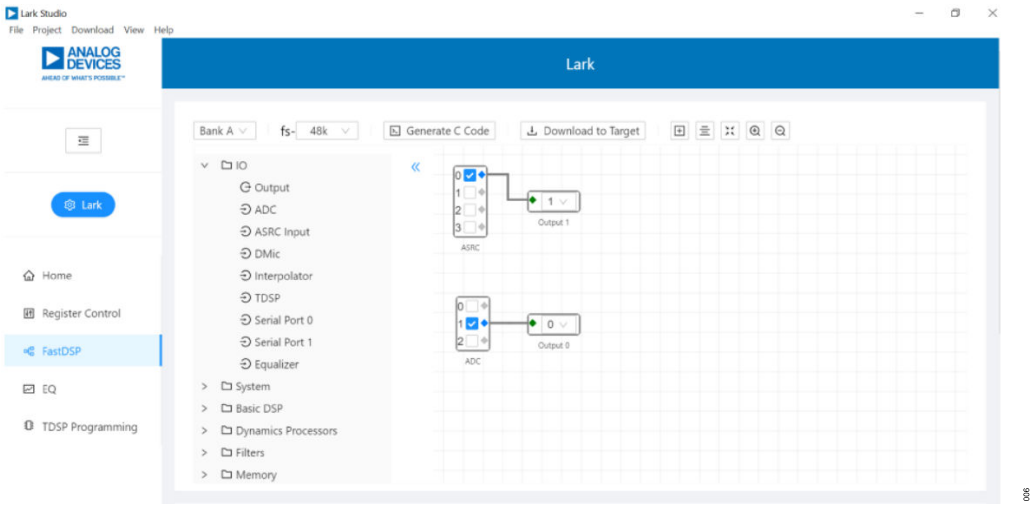

Figure 6. FastDSP Schematic Configuration

USING THE EVALUATION BOARD

POWER SUPPLY

The three ways to supply power to the EVAL-ADAU1861EBZ include the following:

1. By connecting a 5 V USB cable to P1 for control port communication
2. By connecting a 12 V DC power cable to J1
3. By connecting a 12 V DC power to P22

The FTDI 4232 is powered by an on-board LDO regulator with a 3.3 V output.

In addition, the following are other power-conversion circuits on the EVAL-ADAU1861EBZ:

- A buck or boost DC-DC converter (LTC3115EDHD-1#PBF) with a 7 V output.
- An LDO regulator circuit (LT3042IMSE#TRPBF) that provides a bias (6 V) for the external audio sources input circuit.
- An LDO regulator (U38, ADP7105ARDZ) with a 5 V output that provides power sources for other 5 V input circuits.
- An LDO regulator (U39, ADP1715ARMZ-3.3-R7) with a 3.3 V output that provides power sources for level-shift, pull-up, U2, U3, Y3, and reset circuits.

Table 2. Power-Supply Jumper Setting

	On-Board LDO Regulator and Internal LDO Regulator		External	
Power Source	**Jumper Settings**	**Power-Supply Voltage (V)**	**Jumper Settings**	**Port**
AVDD	Jump JP38 to below the AVDD pin	1.8	Jump JP38 to the UP pin	P23
IOVDD	Jump JP39 to below the IOVDD pin, and add a jumper on JP42	1.8	Jump JP39 to the UP pin and add a jumper on JP42	P24
HPVDD_L	Jump JP41 to below the HPVDD_L pin	1.3	Jump JP41 to the UP pin	P25
DVDD	Jump JP22 to low and then jump JP40 to below the DVDD pin on the on-board LDO regulator Jump JP22 high and then remove the JP40 jumper on the ADAU1861 internal LDO regulator	0.9	Jump JP22 low and then jump JP40 to the UP pin	P26

USING THE EVALUATION BOARD

CONTROL PORT

The EVAL-ADAU1861EBZ is configured to SPI mode by default. It also supports I2C and UART communications. Detailed connection and jumpers please refer to Table 3.

Table 3. Control Port Jumper and Switch (S1) Settings

Communication Port	Switch S4 Address Setting	Jumper Settings	Switch S1 Settings
SPI	Not applicable	Jump JP28, JP27, JP1, and JP26 to the right side (SDA/MISO_B, SCL/SCLK_B, ADDR1/MOSI_B, ADDR0/SS_B)	Up (SPI)
I^2C	S4, default 0x64 (00), 0x65 (01), 0x66 (10), 0x67 (11)	Jump JP28, JP27, JP1, and JP26 to the right side (SDA/MISO_B, SCL/SCLK_B, ADDR1/MOSI_B, ADDR0/SS_B)	Down (I^2C)
UART	Not applicable	Jump JP28, JP27, JP1, JP26 to the left side (TX, GND, RXI, IOVDD)	Not applicable

USING THE EVALUATION BOARD

CODEC SYSTEM

Clock Option

The EVAL-ADAU1861EBZ has three options for providing a main clock to the ADAU1861. The default option is to use the on-board 24.576 MHz oscillator. The second option is to provide an external MCLK signal directly to the XTALI pin of the codec from JP9 and JP11. The third option is to use the on-board crystal 24.576 MHz. Refer to Table 4 to check the MCLK settings.

Table 4. MCLK Jumper Settings

Clock Source	Jumper Settings	External Port
Oscillator	Pin 1 to Pin 2 of JP9, Pin 1 to Pin 2 of JP11, jump JP9 to the left (OSC), and jump JP11 to the left (MCLK)	Not applicable
Crystal	Float JP9 and Pin 2 to Pin 3 of JP11, and jump JP11 to the right (XTALI_MCLKIN)	Not applicable
External MCLK	Pin 2 to Pin 3 of JP9, Pin 1 to Pin 2 of JP11, jump JP9 to the right (EXT_MCLK), and jump JP11 to the left (MCLK)	JP9, EXT_MCLK pin

Boot-Up Options

Two boot-up options are available for the EVAL-ADAU1861EBZ. Use JP24 to select the boot-up options, which are self boot enabled or disabled. When self boot is enabled, the Tensilica HiFi 3z DSP core of the ADAU1861 loads the program from flash through QSPI™ with two ROM boot modes that can be selected by JP25.

Power-Down

The EVAL-ADAU1861EBZ can power down all of the analog and digital circuits of the codec by pressing the S2 button.

AUDIO INPUTS AND OUTPUTS

The EVAL-ADAU1861EBZ has multiple audio input and output options, including digital and analog, including three analog inputs, one analog output, eight digital microphone channels, a 2-channel pulse-density modulation (PDM) output, and two serial audio interface ports.

In addition, for audio tuning, the ADAU1966A also supports a 16-channel digital-to-analog converter. With its default settings, the ADAU1966A works in standalone mode after power on with a 12.288 MHz oscillator clock input. To save power consumption, the ADAU1966A works in subordinate mode, 256 × the sampling frequency (f_S), and a TDM 16 with digital audio input from the ADAU1861 serial audio port, I2S0. To improve performance of the ADAU1966A output, main mode of the ADAU1966A is suggested when audio tuning (see Table 5 for additional information).

Table 5. ADAU1966A Configurations

Mode	Resistor Installed	Resistor Uninstalled
Program	R30	R39
Standalone	R39	R30
Main	R34	R43
Subordinate	R43	R34

To program the ADAU1966A, P14 can be used as the control port with I^2C or SPI.

Analog Inputs

The three analog inputs (P2, P3, and P4) can be configured as microphone or line inputs. All three inputs are set to differential or single-ended through JP8, JP9, and JP10. Each analog input can work with an optional programmable-gain amplifier (PGA). JP5 can be used to choose mono (only ADC0) or stereo input mode (ADC0 and ADC1).

Refer to Table 6 for the hardware configuration of the analog input signals. Note that the control register must be changed simultaneously.

Table 6. ADC Mode Jumper Settings

ADC No.	Mode	Jumper Settings
ADC0	Differential	Jump JP8 to DIFF
	Single-ended	Jump JP8 to SINGLE
ADC1	Differential ends	Jump JP7 to DIFF
	Single-ended	Jump JP7 to SINGLE
ADC2	Differential ends	Jump JP6to DIFF
	Single-ended	Jump JP6 to SINGLE

Analog Output

The analog output (P13) can be set as a line output driver or as a headphone driver. In line output mode, the typical load is 10 kΩ. In headphone output mode, the typical loads are 16 Ω to 32 Ω. In addition, the ADAU1966A chip also supports 16 DAC single-channel analog outputs. Refer to Table 7 for detailed information.

Table 7. DAC Output Interfaces and Signal

Chip Number	Function	Pin Number and Px Value
ADAU1966A (Single-Ended)	DAC1P	Pin 3 of P5
	DAC2P	Pin 2 of P5
	DAC3P	Pin 3 of P6
	DAC4P	Pin 2 of P6
	DAC5P	Pin 3 of P7
	DAC6P	Pin 2 of P7
	DAC7P	Pin 3 of P8
	DAC8P	Pin 2 of P8
	DAC9P	Pin 3 of P9
	DAC10P	Pin 2 of P9
	DAC11P	Pin 3 of P10
	DAC12P	Pin 2 of P10
	DAC13P	Pin 3 of P11

USING THE EVALUATION BOARD

Table 7. DAC Output Interfaces and Signal (Continued)

Chip Number	Function	Pin Number and Px Value
	DAC14P	Pin 2 of P11
	DAC15P	Pin 3 of P15
	DAC16P	Pin 2 of P15
ADAU1861 (Differential)	HPOUTP	Pin 2 of P13
	HPOUTN	Pin 3 of P13

Digital Microphone Inputs

One default external digital microphone (DMIC) interfaces on the EVAL-ADAU1861EBZ, P20. Note that Pin 1, Pin 3, Pin 5, and Pin 7 of P44 are GND. Meanwhile, the external DMIC interface can be transferred to 0.3 V using a level shifter (S7) by jumping JP31, JP32, and JP38.

In addition, there is a DMIC array on board that is used to beam form. DMIC_CLK_MP0 and JTAG TCK_MP22 can be chosen as the DMIC clock input through JP30 and JP29.

Table 8. DMIC Interface

Function	Pin Number and Px Value
DMIC_CLK_MP0	Pin 2 of P20
DMIC_CLK_MP0	Pin 4 of P20
DMIC01_MP1	Pin 6 of P20
DMIC01_MP2	Pin 8 of P20

PDM Outputs

The PDM output is P21, and its recommended setting is to use the MP22 to MP25 pins as PDM outputs. Based on the level-shifter switch, the power supply of the interface is 1.8 V or 3.3 V. In addition, note that, Pin 1, Pin 3, Pin 5, and Pin 7 of P21 are GND. If the P20, JP34, and JP37 jumpers are floating jumpers, the default interface is JTAG.

SERIAL AUDIO INTERFACE

Serial audio signals in I^2S, left-justified, right-justified, and TDM formats are available by the serial audio interface headers (P18 and P19) to connect an external I^2S- or TDM-compatible device. Based on the level-shifter switch, the power supply of the interface is 1.8 V or 3.3 V, and Pin 1, Pin 3, Pin 5, and Pin 7 of P18 and Pin 1, Pin 3, Pin 5, and Pin 7 of P19 are all grounded.

Noticed that the serial audio port (I2S0) is connected to the ADAU1966A by 0 Ω resistor R112, and the R113 and R114 resistors are for audio tuning.

Table 9. Serial Audio Interface

Function	Pin Number and Px Value
I2S0 Data In	Pin 2 of P18
I2S0 Data Out	Pin 4 of P18
I2S0 Frame Clock	Pin 6 of P18
I2S0 Bit Clock	Pin 8 of P18
I2S1 Data In	Pin 2 of P19
I2S1 Data Out	Pin 4 of P19
I2S1 Frame Clock	Pin 6 of P19
I2S1 Bit Clock	Pin 8 of P19

OTHER INTERFACES

Other interfaces include the following:

- JTAG
- UART
- Flash
- Multipurpose pin

The JTAG interface is P12. Use the mIDAS-Link emulator to communicate with the Tensilica HiFi 3z DSP core.

The UART interface is P17.

An on-board flash W25Q128JWEIQ -128 M bits interface is available. Use JP12 to JP16 and JP21 to communicate with this flash from the ADAU1861 by QSPI. In addition, use JP17 to JP20 to communicate with this flash from the SPI. P16 is also included to connect an external flash, if required.

Note that all multipurpose pins (MP0 to MP25) are used to configure a variety of other functions, such as PDM, general-purpose input and output (GPIO), DMIC, and so on.

HARDWARE DESCRIPTION

JUMPERS

Table 10 lists the connector and jack descriptions.

Table 10. Connector and Jack Description

Reference Designator	Functional Name	Description
P1	USB interface	USB +5 V power and communication with GUI.
P2	Analog Input 2	Default differential-input, 3.5 mm jack.
P3	Analog Input 1	Default differential-input, 3.5 mm jack.
P4	Analog Input 0	Default differential-input, 3.5 mm jack.
P5	Analog output	DAC1 and DAC2 single-output, 3.5 mm jack.
P6	Analog output	DAC3 and DAC4 single-output, 3.5 mm jack.
P7	Analog output	DAC5 and DAC6 single-output, 3.5 mm jack.
P8	Analog output	DAC7 and DAC8 single-output, 3.5 mm jack.
P9	Analog output	DAC9 and DAC10 single-output, 3.5 mm jack.
P10	Analog output	DAC11 and DAC12 single-output, 3.5 mm jack.
P11	Analog output	DAC13 and DAC14 single-output, 3.5 mm jack.
P12	JTAG Interface	Joint Test Action Group (JTAG) communication.
P13	Analog output	Default differential-output, 3.5 mm jack.
P14	External control interface	External communication with ADAU1966A.
P15	Analog output	DAC15 and DAC16 single-output, 3.5 mm jack.
P16	External flash interface	Header that connects the external flash to the ADAU1861. When using the external flash, connect the JP22 pull-up to AVDD. Note that the default is to pull-down to GND on the board.
P17	UART interface	UART communication with level shift.
P18	Serial Audio Port 0	Input and output header for serial-audio signals.
P19	Serial Audio Port 1	Input and output header for serial-audio signals.
P20	Internal and external DMIC select	Used to select between the external DMIC source or the on-board DMIC. Note that the default is floating on the board. When using the external DMIC arrays, connect the external DMIC with this interface. When using the level shifter, connect JP31, JP32, and JP33. Note that the default is by floating.
P21	PDM output interface	Header that allows PDM interface devices to be connected to the EVAL-ADAU1861EBZ.
P22	EXT_12V	Used to connect the external 12 V supply to the EVAL-ADAU1861EBZ.
P23	EXT_AVDD	Used to connect the external AVDD (1.8 V) supply to the EVAL-ADAU1861EBZ. When using the external AVDD, connect JP38 to EXT_AVDD.
P24	EXT_IOVDD	Used to connect the external IOVDD (1.8 V) supply to the EVAL-ADAU1861EBZ. When using the external AVDD, connect JP39 to EXT_IOVDD.
P25	EXT_HPVDDL	Used to connect the external HPVDDL (1.3 V) supply to the EVAL-ADAU1861EBZ. When using the external AVDD, connect JP41 to EXT_HPVDDL.
P26	EXT_DVDD	Used to connect the external DVDD (0.9 V) supply to the EVAL-ADAU1861EBZZ. When using the external AVDD, connect JP40 to EXT_DVDD.
JP1 and JP26 to JP28	Communication Interface	By default, I^2C or SPI is used to communicate with the ADAU1861 by using the S1 switch. These jumpers must connect Pin 2 and Pin 3 if choose to use the UART.
JP2	Audio source bias select for ADC2	Provides the bias selection for the external audio sources. Note that the default is by floating.
JP3	Audio source bias select for ADC1	Provides the bias selection for the external audio sources. Note that the default is by floating.
JP4	Audio source bias select for ADC0	Provides the bias selection for the external audio sources. Note that the default is by floating.
JP5	STEREO or MONO sound selection	Used to choose between stereo and mono.
JP6	ADC2 input option	Selects single-ended input or differential input (AINP2 connects to DIFF by default).
JP7	ADC1 input option	Selects single-ended input or differential input (AINP1 connects to DIFF by default).
JP8	ADC0 input option	Selects single-ended input or differential input (AINP0 connects to DIFF by default).
JP9	CLK option	Selects EXT_CLK or Y1 output, default Y1 output.

HARDWARE DESCRIPTION

Table 10. Connector and Jack Description (Continued)

Reference Designator	Functional Name	Description
JP10	RESET option	The FT4232HQ-REEL sends the reset signal to the ADAU1861BCSZ and the ADAU1966A. Note that the default is floating if the jumper is connected. Use S2 to reset the ADAU1861BCSZ and the ADAU1966A.
JP11	XTALI/MCLKIN option	Used to select the signal from JP9 or the on-board crystal as the XTALI/MCLKIN.
JP12	QSPIM_CS_MP12 pin jumper	Used to connect the CS_N pin on the on-board flash to the MP12 pin on the ADAU1861.
JP13	QSPIM_CLK_MP11 pin jumper	Used to connect the CLK pin on the on-board flash to the MP11 pin on the ADAU1861.
JP14	QSPIM_SDIO0_MP13 pin jumper	Used to connect the DI/IO0 pin on the on-board flash to the MP13 pin on the ADAU1861.
JP15	QSPIM_SDIO1_MP14 pin jumper	Used to connect the DO/IO1 pin on the on-board flash to the MP14 pin on the ADAU1861.
JP16	QSPIM_SDIO2_MP15 pin jumper	Used to connect the WP_N/IO2 pin on the on-board flash to the MP15 pin on the ADAU1861.
JP17 to JP20	Communication interface	Used with the I^2C or SPI for the ADAD1861 and flash chip (W25Q128JWEIQ) communication.
JP21	QSPIM_SDIO3_MP16 pin jumper	Used to connect the HOLD_N/RESET_N/IO3 pin on the on-board flash to the MP15 pin on the ADAU1861.
JP22	REG_EN jumper	Used to select AVDD or GND to REG_EN.
JP23	IRQ jumper	Sends an IRQ signal to the ADAU1861 chip when S3 is pushed down to GND.
JP24	SELFBOOT jumper	Used to select IOVDD or GND to SELFBOOT.
JP25	ROMBOOT jumper	Used to select IOVDD or GND to ROM_BOOT_MODE.
JP29/JP30	DMIC CLK option	Used to select DMIC_CLK_MP0 or TCK_MP22 to CLK for the DMIC array.
JP31 to JP33	DMIC level shift jumper	DMIC level-shift jumper. Note that the default is floating.
JP34 to JP37	PDM level shift jumper	PDM level-shift jumper. Note that the default is floating.
JP38	1.8V_LDO/EXT_AVDD	Used to select between the external source or the 1.8 V on-board LDO regulator for the AVDD.
JP39	1.8V_LDO/EXT_IOVDD	Used to select between the external source or the 1.8 V on-board LDO regulator for the IOVDD.
JP40	0.9V_LDO/EXT_DVDD	Used to select between the external source or the 0.9 V on-board LDO regulator for the DVDD.
JP41	1.3V_LDO/EXT_HPVDDL	Used to select between the external source or the 1.3 V on-board LDO regulator for the HPVDDL.
JP42	IOVDD jumper	Used to connect between JP39 and ADAU1861 IOVDD.

EVALUATION BOARD SCHEMATICS

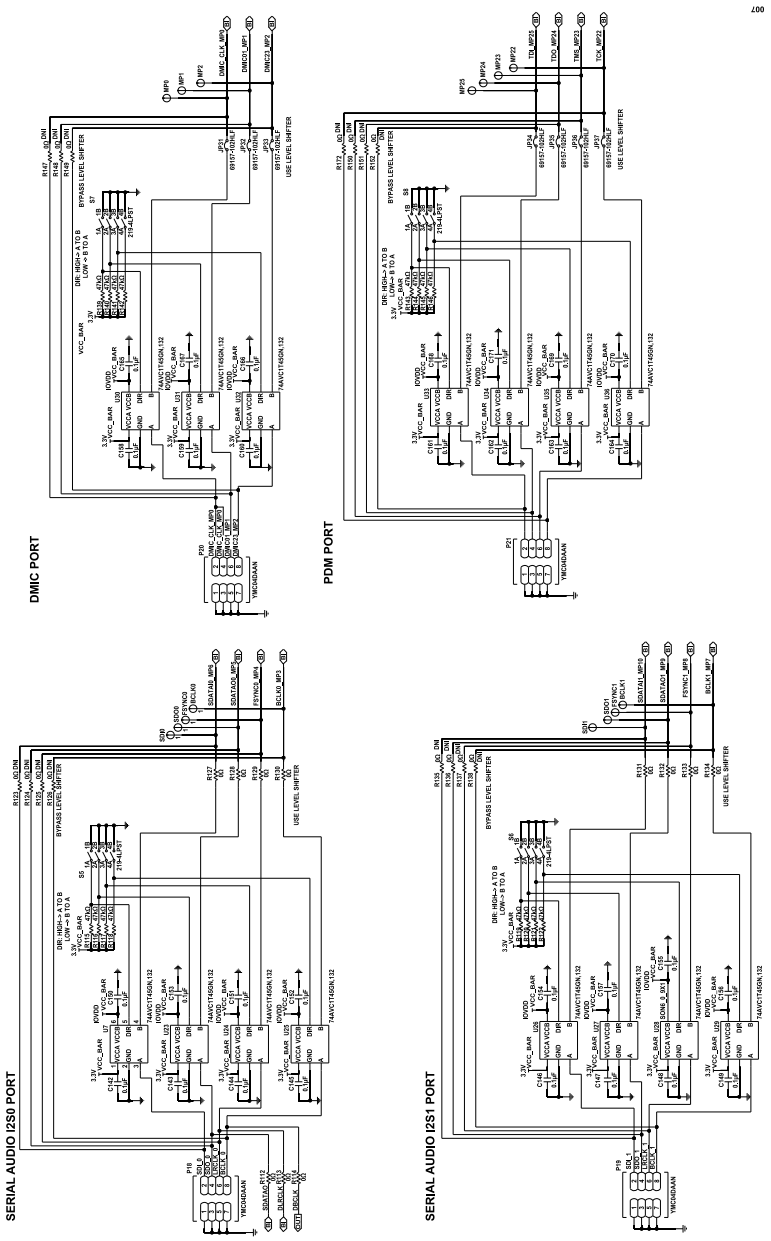

Figure 7. EVAL-ADAU1861EBZ Schematic, Page 1

EVALUATION BOARD SCHEMATICS

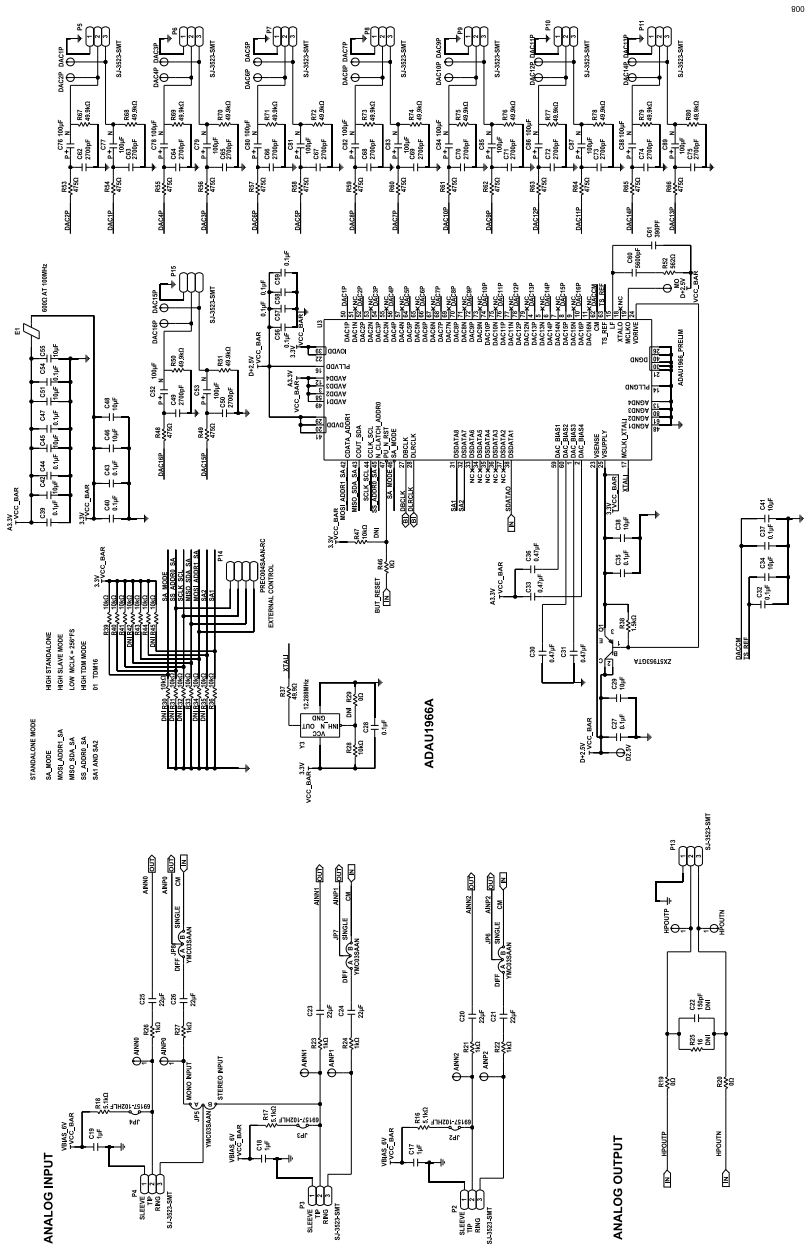

Figure 8. EVAL-ADAU1861EBZ Schematic, Page 2

EVALUATION BOARD SCHEMATICS

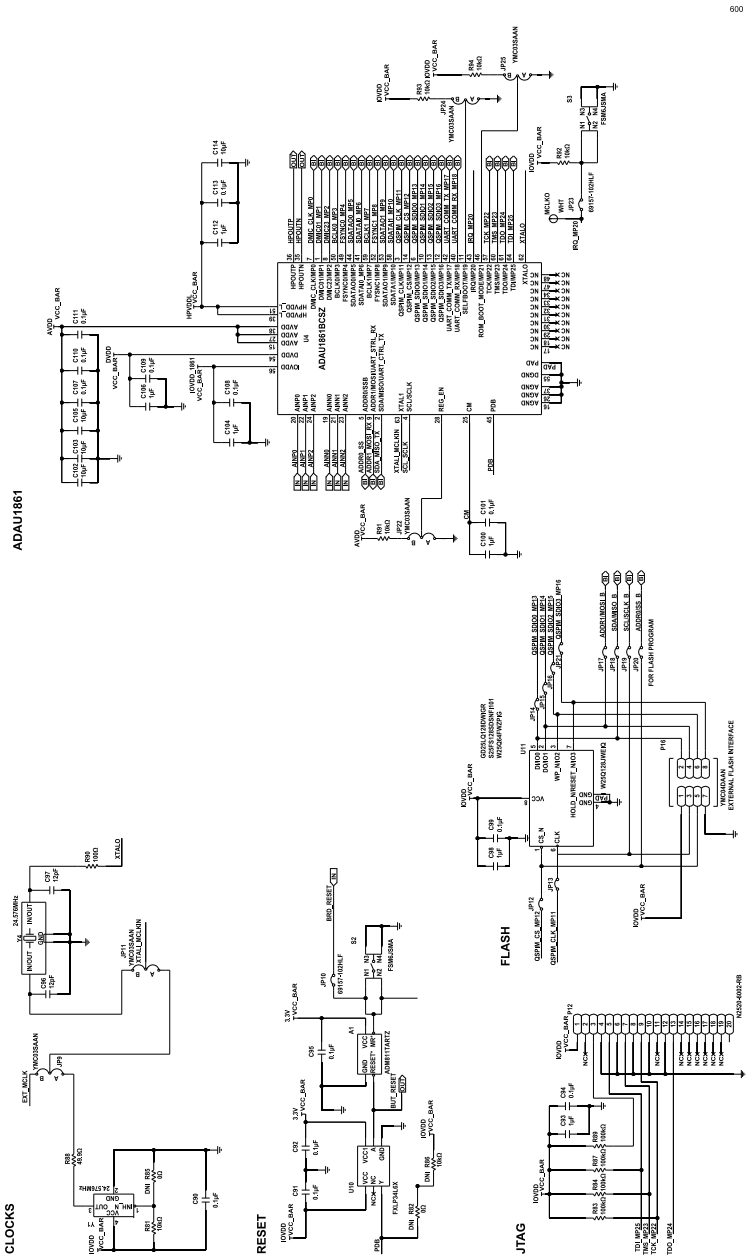

Figure 9. EVAL-ADAU1861EBZ Schematic, Page 3

EVALUATION BOARD SCHEMATICS

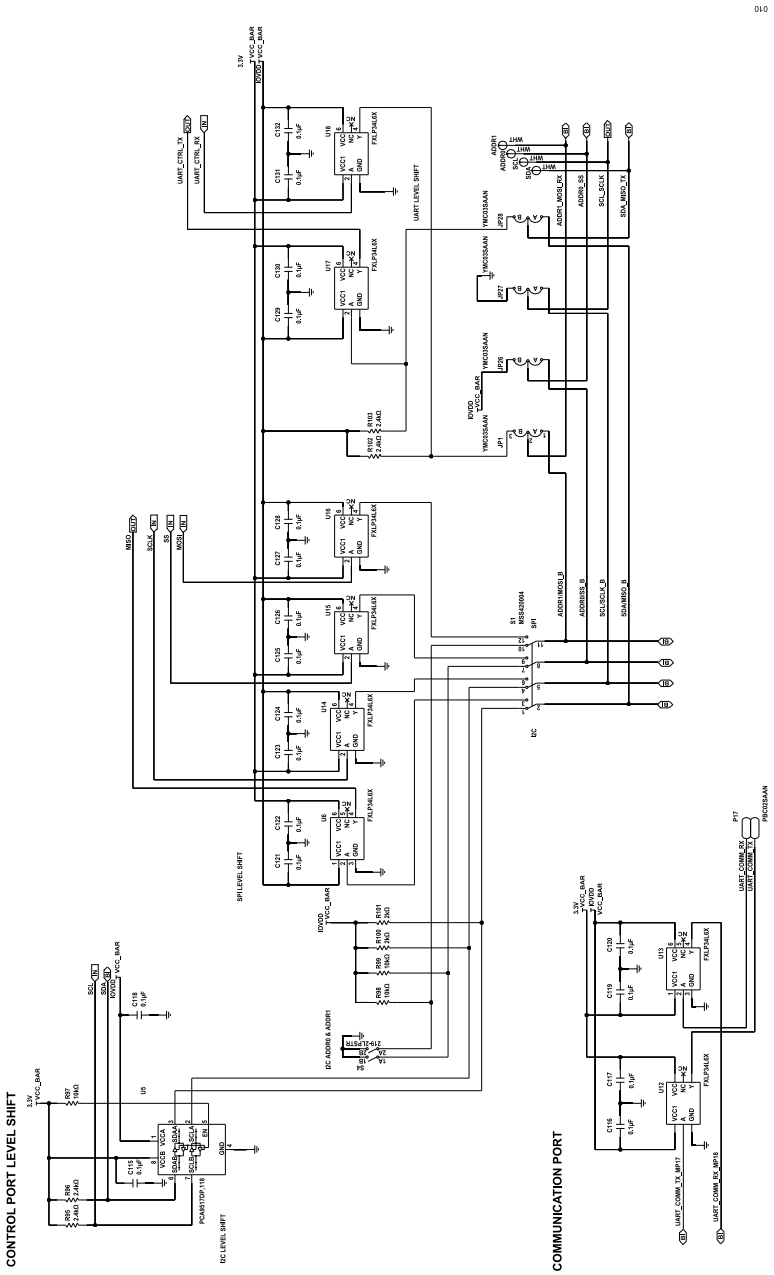

Figure 10. EVAL-ADAU1861EBZ Schematic, Page 4

EVALUATION BOARD SCHEMATICS

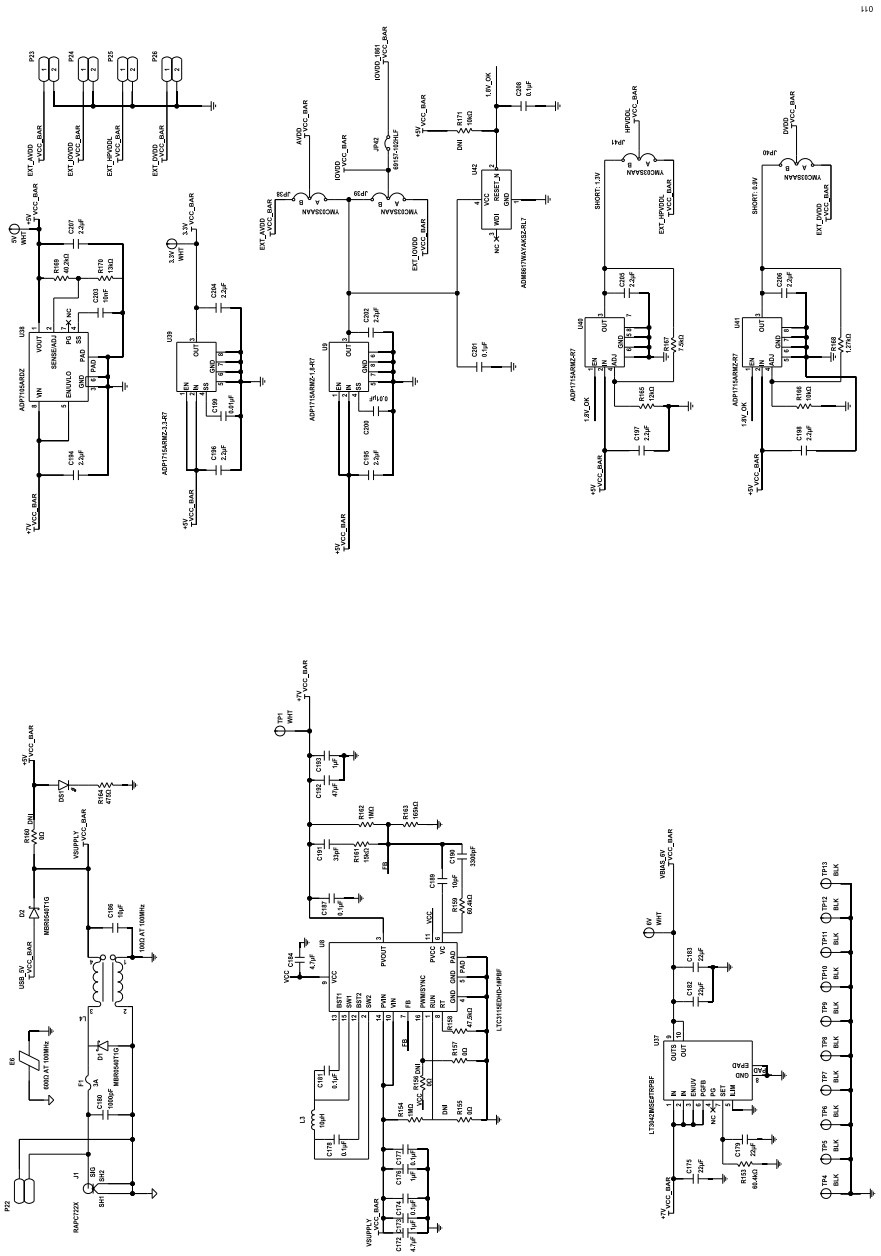

Figure 11. EVAL-ADAU1861EBZ Schematic, Page 5

EVALUATION BOARD SCHEMATICS

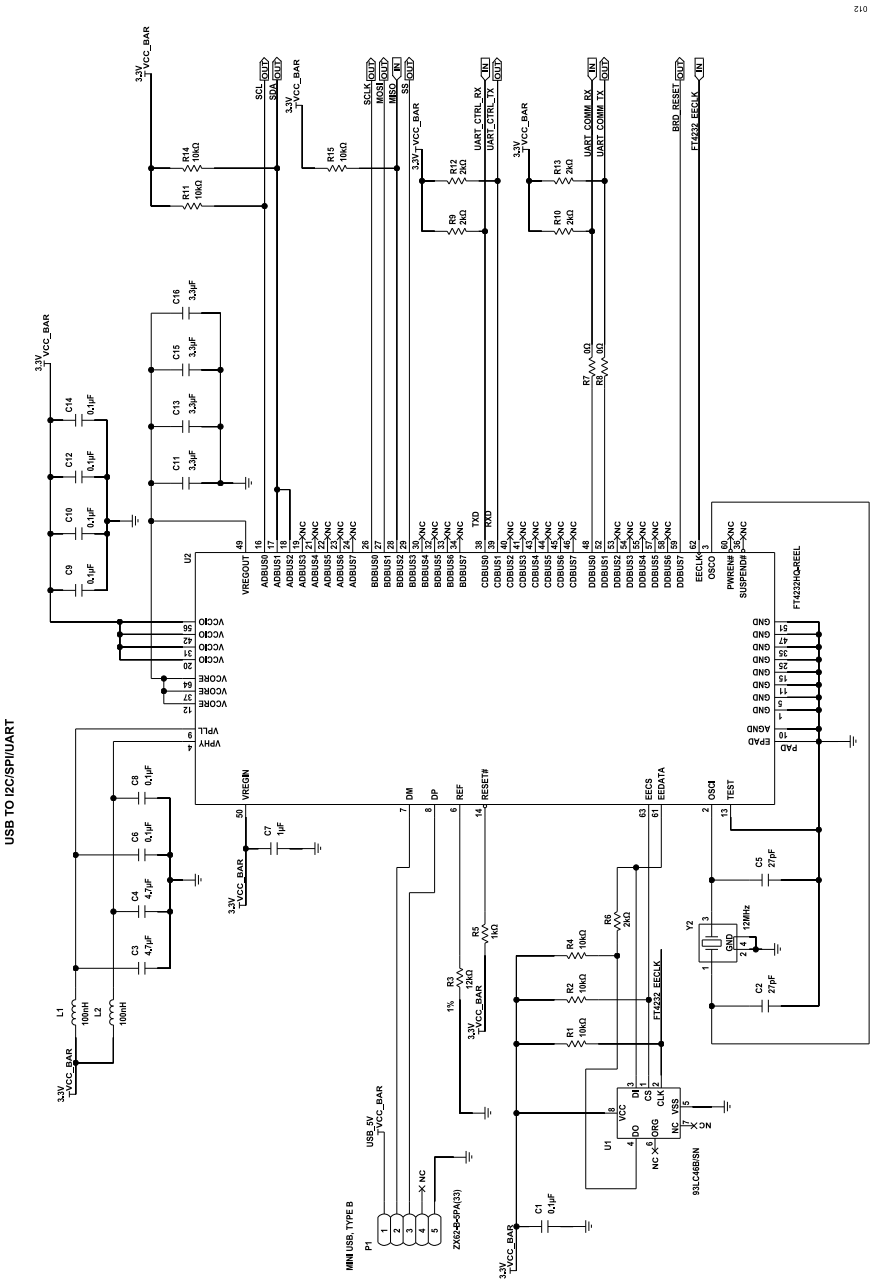

Figure 12. EVAL-ADAU1861EBZ Schematic, Page 6

EVALUATION BOARD SCHEMATICS

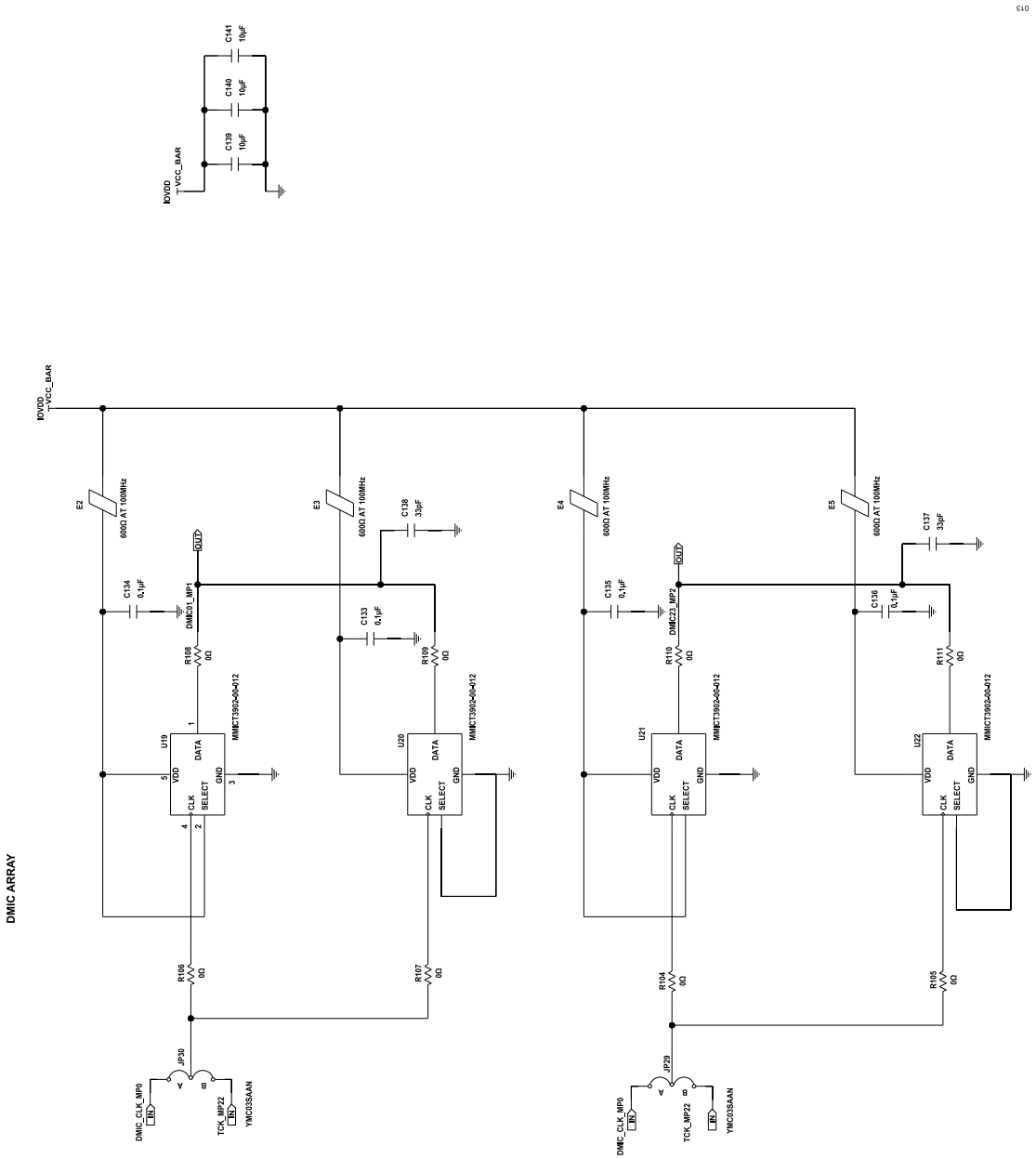

Figure 13. EVAL-ADAU1861EBZ Schematic, Page 7

ORDERING INFORMATION

BILL OF MATERIALS

Table 11. Bill of Materials

Qty	Components	Description	Manufacturer	Manufacturer Number
50	3.3V, 5V, 6V, ADDR0, ADDR1, AINN0, AINN1, AINN2, AINP0, AINP1, AINP2, BCLK0, BCLK1, D2.5V, DAC1P to DAC16P, FSYNC0, FSYNC1, HPOUTN, HPOUTP, MCLKO, MO, MP0, MP1, MP2, MP22, MP23, MP24, MP25, SCL, SDA, SDI0, SDI1, SDO0, SDO1, TP1	White test point, connector PCB	Keystone Electronics	5002
1	A1	Microprocessors supervisory circuit in 4-Lead SOT-143, log	Analog Devices, Inc.	ADM811TARTZ-REEL7
91	C1, C6, C8, C9, C10, C12, C14, C27, C28, C32, C35, C37, C39, C40, C43, C44, C47, C54, C56 to C59, C90 to C92, C94, C95, C99, C101, C107 to C111, C113, C115 to C136, C142 to C171, C178, C181, C201, C208	0.1 µF ceramic capacitors, 16 V, 10%, X7R, 0402, AEC-Q200	Murata	GCM155R71C104KA55D
10	C7, C17 to C19, C93, C98, C100, C104, C106, C112	1 µF ceramic capacitors, 16 V, 10%, X7R, 0603, AEC-Q200	Murata	GCM188R71C105KA64D
17	C29, C34, C38, C41, C42, C45, C46, C48, C51, C55, C102, C103, C105, C114, C139 to C141	10 µF ceramic capacitors, 10 V, 20%, X5R, 0603, AEC-Q200	Taiyo Yuden	GRM188R61A106ME69D
4	C11, C13, C15, C16	Not recommended for new designs (NRND), 3.3 µF ceramic capacitors, 16 V, 20%, X6S, 0603, low equivalent series resistance (ESR)	TDK	C1608X6S1C335M080AC
2	C137, C138	33 pF ceramic capacitors, 16 V, 5%, X7R, 0402, AEC-Q200	KEMET	C0402C330J4RACAUTO
1	C172	4.7 µF ceramic capacitor, 50 V, 10%, X7R, 1206	Murata	GRM31CR71H475KA12L
3	C173, C176, C193	1 µF ceramic capacitors, 50 V, 10%, X7R, 1206	AVX	12065C105KAT2A
3	C174, C177, C187	0.1 µF ceramic capacitors, 50 V, 10%, X7R, 0603, AEC-Q200, Low ESR	TDK	CGA3E2X7R1H104K080AA
10	C20, C21, C23 to C26, C175, C179, C182, C183	22 µF ceramic capacitors, 16 V, 10%, X7R, 1210	Murata	GRM32ER71C226KEA8L
1	C180	1000 pF ceramic capacitors, 50 V, 5%, C0G, 1206	AVX	12065A102JAT2A
3	C3, C4, C184	4.7 µF ceramic capacitors, 16 V, 10%, X6S, 0603	Murata	GRM188C81C475KE11D
1	C186	10 µF ceramic capacitor, 50 V, –20% to +80%, Y5V, 1210	AVX Corporation	GCM32EC71H106KA03L
1	C189	10 pF ceramic capacitor, 50 V, 0.5 pF, C0G, 0402	TDK	CGA2B2C0G1H100D050BA
1	C190	3300 pF ceramic capacitor, 50 V, 5%, C0G, 0603, AEC-Q200, Low ESR	TDK	CGA3E2C0G1H332J080AA
1	C191	33 pF ceramic capacitor, 50 V, 5%, C0G, 0402, AEC-Q200, Low ESR	TDK	CGA2B2C0G1H330J050BA
1	C192	47 µF ceramic capacitors, 10 V, 10%, X7R, 1210	Murata	GRM32ER71A476KE15L
10	C194 to C198, C202, C204 to C207	2.2 µF ceramic capacitors, 10 V, 10%, X7R, 0603	Murata	GRM188R71A225KE15D
2	C199, C200	0.01 µF ceramic capacitors, 25 V, 10%, X7R, 0402, AEC-Q200	Murata	GCM155R71E103KA37D
2	C2, C5	27 pF ceramic capacitors, 50 V, 5%, C0G, 0603	PHYCOMP (Yageo)	CC0603JRNP09BN270
1	C203	10 nF ceramic capacitor, 16 V, 5%, X7R, 0402	AVX Corporation	0402YC103JAT2A
4	C30, C31, C33, C36	NRND, 04.7 µF ceramic capacitors, 6.3 V, 10%, X5R, 0603	Murata	GRM188R60J474KA01D
16	C49, C50, C62 to C75	2700 pF ceramic capacitors, 50 V, 5%, C0G, 0603	Murata	GRM1885C1H272JA01D

ORDERING INFORMATION

Table 11. Bill of Materials (Continued)

Qty	Components	Description	Manufacturer	Manufacturer Number
16	C52, C53, C76 to C89	100 µF tantalum capacitors, 6.3 V, 10%, 3528-20	AVX Corporation	TAJB107K006RNJ
1	C60	5600 pF ceramic capacitor, 25 V, 10%, X7R, 0402	AVX Corporation	04023C562KAT4A
1	C61	390 pF ceramic capacitor, 50 V, 5%, C0G, 0402, AEC-Q200	Murata	GCM1555C1H391JA16D
2	C96, C97	12 pF ceramic capacitors, 50 V, 5%, C0G, 0402	Murata	GJM1555C1H120JB01D
2	D1, D2	Diodes, Schottky, rectifier, surface-mount device (SMD)	ONSEMI	MBR0540T1G
1	DS1	Light-emitting diode (LED), SMD, 0603, green	LUMEX	SML-LX0603GW-TR
2	E1, E6	Inductors, chip ferrite bead, 0.90 Ω DC resistance maximum, 0.2 A	Murata	BLM31AJ601SH1L
4	E2,E3,E4,E5	Inductor, ferrite bead, 0.52 Ω DCR, 0.3 A	TDK	MMZ1005S601CTD25
1	F1	Fuse reset polyswitch	TE Connectivity Ltd	SMD300F-2
1	J1	Connector PCB, Powerjack mini, 0.08 inches, right angle	Switchcraft	RAPC722X
19	JP1, JP5 to JP9, JP11, JP22, JP24 to JP30, JP38 to JP41	Connector PCB, high temperature, 3-position male headers, unshrouded, single-row, single-throw, 2.54 mm pitch, 3.05 mm solder tail	Sullins	YMC03SAAN/PRPC003SAAN-RC
23	JP2 to JP4, JP10, JP12 to JP21, JP23, JP31 to JP37, JP42	Connector PCB, BERG jumpers, ST male two position, 1X, M000385	Amphenol FCI	69157-102HLF/PREC001DAAN-RC
2	L1, L2	Inductors, RF ceramic chip	Johanson Technology, Inc.	L-07CR10JV6T
1	L3	Inductor, surface-mount technology (SMT) power	Coilcraft	MSS1048-103MLB
1	L4	Inductor, common-mode chock for large current, 0.013 Ω DCR, 6 A	Murata	DLW5BTM101SQ2L
1	P1	Connector PCB, Micro-USB 2.0 right angle, 0.65 mm pitch	Hirose	ZX62-B-5PA(33)
12	P2 to P11, P13, P15	Connector PCB, 3.5 mm, stereo mode, audio jack stereo	CUI	SJ-3523-SMT
1	P12	Connector PCB, low profile header, dual row, 2.54 mm pitch	3M	N2520-6002-RB
1	P14	Connector PCB, header male, ST, 2.54 mm pitch, 3.05 mm solder tail	Sullins	PREC004SAAN-RC
5	P16, P18 to P21	Connector PCB, 8-position male headers, double row ST, 2.54 mm pitch, 3.05 mm solder tail, 5.84 mm post height	Sullins	YMC04DAAN/PR20204VBDN
6	P17, P22 to P26	Connector PCB, 2-position male headers, unshrouded single row ST, 2.54 mm pitch, 3.05 mm solder tail	Sullins	PBC02SAAN/PREC001DAAN-RC
1	Q1	PNP transistor medium power	Diodes Inc.	ZX5T953GTA
18	R1, R2, R4, R11, R14, R15, R28, R81, R91 to R94, R97 to R99, R166	10 kΩ SMD resistors, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1002X
7	R6, R9, R10, R12, R13, R100, R101	2 kΩ SMD resistors, 1%, 1/10 W, 0603	Yageo	RC0603FR-072KL
4	R95, R96, R102, R103	2.4 kΩ SMD resistors, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF2401V
25	R7, R8, R19, R20, R46, R104 to R114, R127 to R134, R156	0 kΩ SMD resistors, jumper, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEY0R00V
16	R115 to R122, R139 to R146	47 kΩ SMD resistors, 0.5%, 1/16 W, 0402, AEC-Q200 high reliability	Panasonic	ERA-2AED473X/AT0402FRE0747KL
2	R153, R159	60.4 kΩ SMD resistors, 1%, 1/10 W, 0603	Yageo	RC0603FR-0760K4L
2	R154, R162	1 MΩ SMD resistors,, 1% 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1004V
1	R158	47.5 kΩ SMD resistor, 1%, 1/8 W, 0805, AEC-Q200	Panasonic	ERJ-6ENF4752V
3	R16 to R18	5.1 kΩ SMD resistors, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF5101V
1	R161	15 kΩ SMD resistor, 1%, 1/10 W, 0603	Yageo	RC0603FR-0715KL
1	R163	165 kΩ SMD resistor, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1653V

ORDERING INFORMATION

Table 11. Bill of Materials (Continued)

Qty	Components	Description	Manufacturer	Manufacturer Number
17	R48, R49, R53 to R66, R164	475 Ω SMD resistors, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4750V/ RC0603FR-07475RL
2	R3, R165	12 kΩ SMD resistors, 1%, 1/16 W, 0402	Yageo	RC0402FR-0712KL/ RC0402DR-0712KL
1	R167	7.5 kΩ SMD resistor, 0.1%, 0.15 W, 0603, AEC-Q200, sulfur resistant	Vishay	PAT0603E7501BST1/ RT0603DRE077K5L
1	R168	1.27 kΩ SMD resistor, 1%, 1/10 W, 060,3 AEC-Q200	Panasonic	ERJ-3EKF1271V
1	R169	40.25 kΩ SMD resistor, 1%, 1/10 W, 0603, AEC-Q200	Vishay	CRCW060340K2FKEA/ AC0603FR-1340K2L
1	R170	13 kΩ SMD resistor, 1%, 1/10 W, 0603	Yageo	RC0603FR-0713KL
6	R21 to R24, R26, R27	1 kΩ SMD resistors, 1% 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1001V
7	R32, R39, R40, R42 to R45	10 kΩ SMD resistors, 1% 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1002V
2	R37, R88	49.95 kΩ SMD resistors, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF49R9V
1	R38	1.5 kΩ SMD resistor, 1%, 1/10 W 0402, AEC-Q200	Panasonic	ERJ-2RKF1501X
1	R5	1 kΩ SMD resistor, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1001X
16	R50, R51, R67 to R80	49.9 kΩ SMD resistors, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF4992X
1	R52	562 Ω SMD resistor, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF5620X
4	R83, R84, R87, R89	100 kΩ SMD resistors, 1%, 1/10 W, 0603	Bourns	CR0603-FX-1003ELF
1	R90	100 Ω SMD resistor 5%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GEJ101X
1	S1	Switch, slide, 4PDT	TE Connectivity Ltd	MSS420004
2	S2, S3	Switches, tactile, 6 mm GULLWING SMD	TE Connectivity Ltd	FSM6JSMA
1	S4	Switch, SPST, slide, 2-position	CTS Electronic Components	219-2LPSTR
4	S5 to S8	Switches, 4-postion slide dual in-line package (DIP)	CTS Electronic Components	219-4LPST
10	TP4 to TP13	Connector PCB, black test points	Keystone Electronics	5001
1	U1	IC, CMOS 1K microwave serial EEPROM	Microchip Technology	93LC46B/SN
1	U11	IC, low-power 1.8 V, 128 MBIT, SPI/quad, serial, nonvolatile storage flash	WINBOND	W25Q128JWEIQ
9	U6, U10, U12 to U18	IC, 1-bit unidirectional translators	ONSEMI	FXLP34L6X
4	U19 to U22	IC, bottom port, PDM, low power, multimode microphone with high acoustic overload point mode	TDK	MMICT3902-00-012
1	U2	IC, quad, high-speed, USB to multipurpose UART, multiprotocol synchronous serial engine	FTDI	FT4232HQ-REEL
15	U7, U23 to U36	IC, transistor-to-transistor logic (TTL) translator 1-channel bidirectional	NEXPERIA	74AVC1T45GN,132
1	U3	IC, 16-channel, high performance, 192 kHz, 24-bit DAC	Analog Devices	ADAU1966AWBSTZ
1	U37	IC, 20 V, 200 mA, ultra-low noise, ultra-high power-supply rejection ratio (PSRR) RF linear regulator	Analog Devices	LT3042IMSE#TRPBF
1	U38	IC, 20 V, 500 mA, low noise LDO regulator with soft-start	Analog Devices	ADP7105ARDZ
1	U39	IC, 500 mA, low dropout, CMOS, linear regulator with soft-start	Analog Devices	ADP1715ARMZ-3.3-R7
1	U4	IC, three analog-to-digital converters (ADCs), one DAC, lowe power codec with audio digital-signal processors (DSPs)	Analog Devices	ADAU1861BCSZ-RL
2	U40, U41	IC, 500 mA, low-dropout, CMOS, linear regulator with soft-start	Analog Devices	ADP1715ARMZ-R7
1	U42	IC, low voltage supervisory circuit with watchdog in 4-Lead SC70	Analog Devices	ADM8616WCYAKSZ-RL7
1	U5	IC-CMOS I^2C bus repeater	NXP Semiconductors	PCA9517DP,118

ORDERING INFORMATION

Table 11. Bill of Materials (Continued)

Qty	Components	Description	Manufacturer	Manufacturer Number
1	U8	IC, 40 V, 2 A synchronous buck-boost DC-DC converter	Analog Devices	LTC3115EDHD-1#PBF
1	U9	IC, 500 mA, low-dropout, CMOS, linear regulator with soft-start	Analog Devices	ADP1715ARMZ-1.8-R7
1	Y1	Oscillator, crystal, CMOS, 24.576 MHz, 30 ppm, 15 pF, 1.8 V, 2.5 V, or 3.3 V	Kyocera	KC2520Z24.5760C15XXK
1	Y2	IC, crystal ceramic, 10 pF load capacitance,	Abracon Corporation	ABM3B-12.000MHZ-10-1-U-T
1	Y4	IC, crystal quartz, 12 pF, 500 Ω	ECS, Inc.	ECS-245.7-12-33Q-JES-TR
1	Y3	Oscillator, crystal, CMOS, 12.288 MHz, 30 ppm, 15 pF, 1.8 V, 2.5 V, or 3.3 V	Kyocera	MC2520Z12.2880C19XSH

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).