Industrial SPoE PD Controller

FEATURES

- **IEEE 802.3cg Compliant**
- **Wide Input Voltage Range: 2.3V to 60V**
- **Supports Serial Communication Classification Protocol (SCCP)**
- **Wakeup Signature**
- **Integrated 3.5V Standby Regulator**
- **150µA Maximum Current During Classification**
- Drives Low-Side Bridge MOSFETs for Polarity Correction
- Charge Pump Enhances External N-Channel MOSFET
- Pin Programmable Class Configuration
- Available in 12-Pin MSOP and DFN 4mm × 3mm Packages

APPLICATIONS

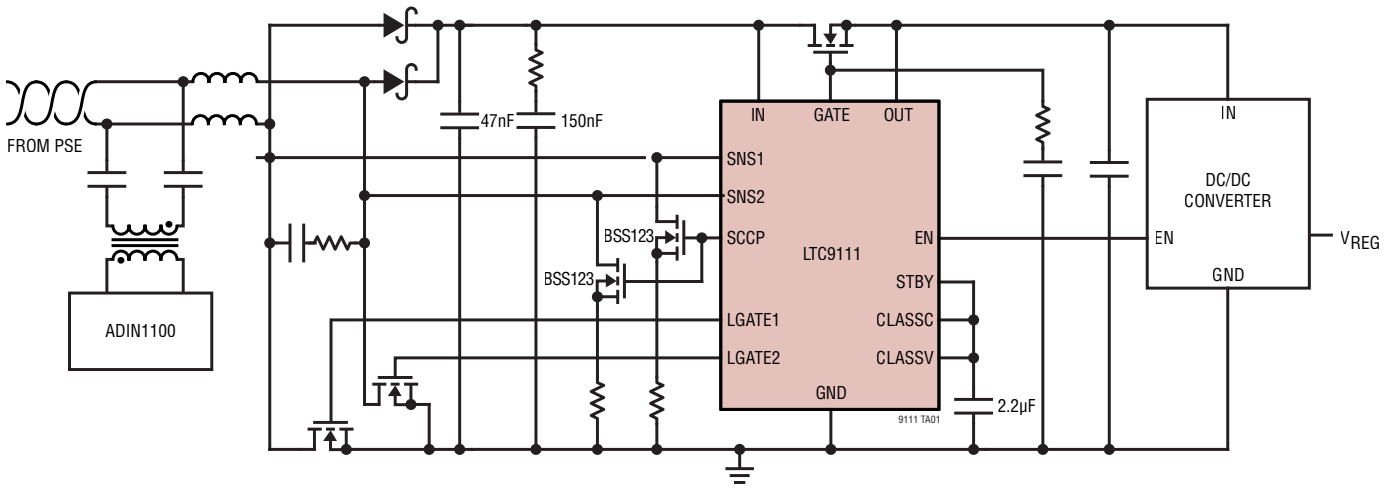
- Building Automation
- Factory Automation
- Security Systems
- Traffic Control Systems

DESCRIPTION

The LTC®9111 is an IEEE 802.3cg compliant Single-Pair Power over Ethernet (SPoE) Powered Device (PD) controller. A wide 2.3V to 60V operating range capability with polarity correction make the LTC9111 particularly well suited for classification-based systems in building and factory automation.

SCCP-based classification ensures full operating voltage is applied by the Power Sourcing Equipment (PSE) only when a valid PD is connected. The LTC9111 drives two external N-channel MOSFET switches during classification with micropower operation to minimize reservoir capacitor requirements. An external N-channel MOSFET switch isolates the output capacitance from the connector during classification and inrush. A voltage supervisor enables the external MOSFET when the PD input voltage exceeds the ON voltage threshold for the configured class and after a mandated delay. The EN output asserts after the controlled GATE pin ramp-up. The MOSFET is disabled if the input voltage drops below the OFF voltage threshold for the configured class. The LTC9111 drives a pair of external low-side N-channel MOSFETs with a low start-up voltage of 1.6V for polarity correction with reduced power losses.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3, 4)

Supply Voltage
- IN ..... –2V to 100V

Input Voltages
- SNS1, SNS2 ..... –5V to 100V
- CLASSC, CLASSV, SCCP ..... –0.3V to 5.5V

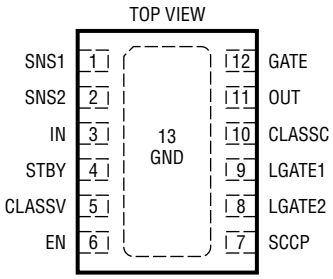
Output Voltages
- LGATE1, LGATE2 ..... –0.3V to 8V
- OUT ..... –2V to 100V
- GATE to OUT ..... –0.3V to 10V

Output Voltages
- GATE ..... –0.3V to 100V
- EN ..... –0.3V to 5.5V
- STBY ..... –0.3V to 5.5V

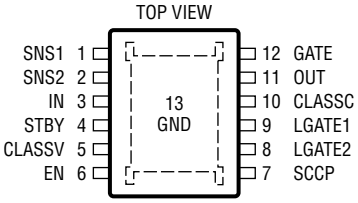
Operating Junction Temperature Range
- LTC9111R ..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DE/EU PACKAGE
12-PIN (4mm × 3mm) PLASTIC DFN
θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-PIN (4mm × 3mm) PLASTIC MSOP
θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC9111RDE#PBF	LTC9111RDE#TRPBF	9111	12-Pin (4mm × 3mm) Plastic DFN	–40°C to 150°C
LTC9111RMSE#PBF	LTC9111RMSE#TRPBF	9111	12-Pin Plastic MSOP with Exposed Pad	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN, SNS1, SNS2, OUT							
V_{IN}	Input Supply Operating Range	Normal Operating Range	●	2.3		60	V
I_{IN}	Input Supply Current	V_{IN} = 3.3V, CLASSIFICATION State V_{IN} = 60V, MDI_POWER2 State	● ●		75 500	150 1000	µA µA
I_{PD_PWR1}	Input Supply Current During Inrush	V_{IN} < V_{ON}, MDI_POWER1 State	●			700	µA
I_{WAKEUP_PD}	Wakeup Signature Current	2.3V < V_{IN} < 3.575V	●	1.3	1.55	1.8	mA
V_{SIG_ENABLE}	DISCONNECT State Exit Threshold Voltage	ΔV_{SNS} Falling Edge	●	3.9	4	4.1	V
$V_{SIG\_DISABLE}$	MDI_PWR1 State Entry Threshold Voltage	ΔV_{SNS} Rising Edge	●	6.7	6.8	6.9	V
V_{ON}	Gate On Threshold Voltage	V_{IN} Rising Edge, V_{SNS1} = V_{IN}, V_{SNS2} = 0V CLASS 10/11/12: V_{CLASSV} = 0V CLASS 13/14/15: V_{CLASSV} = V_{STBY}	 ● ●	 17 44.8	 17.5 46	 18 47.2	 V V
V_{OFF}	Gate Off Threshold Voltage	V_{IN} Falling Edge, V_{SNS1} = V_{IN}, V_{SNS2} = 0V CLASS 10/11/12: V_{CLASSV} = 0V CLASS 13/14/15: V_{CLASSV} = V_{STBY}	 ● ●	 11.5 29	 12 30	 12.5 31	 V V
V_{OV}	Overvoltage Threshold for Classes 10 through 12	V_{IN} Rising Edge	●	37	38.5	40	V
I_{SNS1}	SNS1 Input Current	V_{SNS1} = 60V	●			200	µA
I_{SNS2}	SNS2 Input Current	V_{SNS2} = 60V	●			200	µA
I_{OUT_SLEEP}	OUT Pull-Down Current, Sleep	V_{OUT} = V_{IN} = 6V	●	8	16		µA
I_{OUT_ON}	OUT Leakage Current, Gate ON	V_{OUT} = V_{IN} = 60V	●			±10	µA
V_{EN_ASSERT}	Gate Drive Voltage Required to Assert EN	(V_{GATE} to V_{IN}) Rising Edge	●	6.5		8.2	V
GATE							
ΔV_{GATE}	Gate Drive	ΔV_{GATE} = V_{GATE} to V_{OUT}, I_{LGATE} = –1µA, V_{IN} > 5.75V, MDI_POWER2 State	●	10		12.5	V
$I_{GATE(UP)}$	GATE Pull-Up Current	GATE ON, V_{GATE} = 1V, V_{OUT} = 0V, MDI_POWER2 State	●	–6.5	–10	–14	µA
$I_{GATE(DOWN)}$	GATE Pull-Down Current	GATE OFF, V_{GATE} = V_{OUT} + 5V, 4.4V < V_{IN} to V_{OUT} < 60V	●	3.5		7.5	mA
t_{POWER_DLY}	GATE ON Assertion Delay	ΔV_{SNS} > V_{ON} (Note 4)	●	80	100	120	ms
STBY Regulator							
V_{STBY}	STBY Regulator Output Voltage	V_{IN} > 4V, I_{STBY} < 1.5mA	●	3.4	3.5	3.6	V
V_{STBY_DV}	STBY Regulator Dropout Voltage	I_{STBY} = –0.1mA I_{STBY} = –1.5mA	● ●			40 250	mV mV
I_{STBY_LIM}	STBY Regulator Current Limit	V_{STBY} = 0V	●	2			mA
LGATE1, LGATE2							
V_{LGATE}	Open-Circuit Low-Side Gate Drive Voltage	V_{STBY} = 3.5V, $I_{LGATE1/2}$ = –1µA	●	5		8	V
I_{LGATE}	Start-Up Gate Pull-Up	V_{IN} = 1.6V, $V_{LGATE1/2}$ = 3V V_{IN} = 3.1V, $V_{LGATE1/2}$ = 3V	● ●	–1.5 –20	–5 –60		µA µA
V_{GATE_HI}	Low-Side Gate Voltage Threshold to Enable Wakeup Signature		●	2.9			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Output EN							
V_{OH}	High Output Voltage	I_{SINK} = 0, –0.1µA	●	3.2		3.6	V
V_{OL}	Low Output Voltage	I_{SOURCE} = 0.1mA	●	0		0.25	V
Digital Input CLASSV							
V_{IH}	High Level Input Voltage		●	2			V
V_{IL}	Low Level Input Voltage		●			0.7	V
Ternary Input CLASSC							
V_{IH}	Input High Threshold Voltage		●	V_{STBY} – 0.5			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
$I_{IH, IL}$	High, Low Input Current		●			±100	µA
SCCP							
t_{RSTL}	Minimum Valid PSE Reset Pulse	2.4V < V_{STBY} < 3.6V (Note 4)	●	5		8	ms
t_{PDH}	Presence Detect High	2.4V < V_{STBY} < 3.6V (Note 4)	●	0.78	0.98	1.18	ms
t_{PDL}	Presence Detect Low	2.4V < V_{STBY} < 3.6V (Note 4)	●	3.14	3.92	4.7	ms
t_{R0L}	Read 0 Low	2.4V < V_{STBY} < 3.6V (Note 4)	●	1.96	2.45	2.94	ms
$t_{SCCP\_WATCHDOG}$	SCCP Watchdog Timer	2.4V < V_{STBY} < 3.6V (Note 4)	●	1320	1650	1970	ms
V_{TH}	SCCP Logic High	2.4V < V_{STBY} < 3.6V, ($V_{SNS1/2}$ to V_{GND})	●		2.05	2.9	V
V_{TL}	SCCP Logic Low	2.4V < V_{STBY} < 3.6V, ($V_{SNS1/2}$ to V_{GND})	●	1.2	1.95		V
I_{SCCP_UP}	SCCP FET Driver Pull-Up Current	V_{STBY} = 3.5V, V_{SCCP} = 2V	●	–150	–225		µA
I_{SCCP_DN}	SCCP FET Driver Pull-Down Current	V_{STBY} = 3.5V, V_{SCCP} = 1V	●	150	285		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

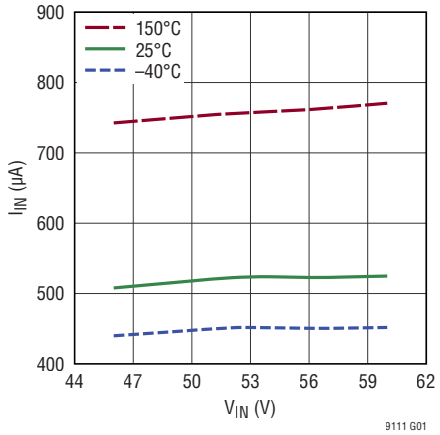
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits V_{GATE} to a minimum of 10V above V_{OUT}. Driving this pin voltages beyond this clamp may damage the device.

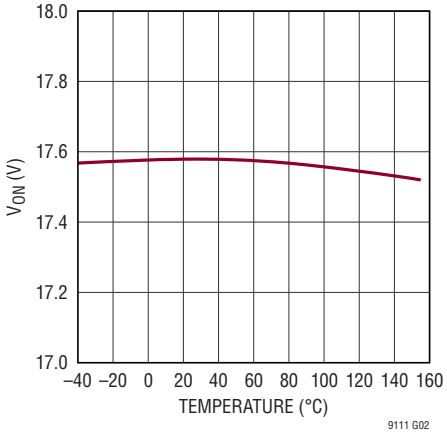
Note 4: These specifications are guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

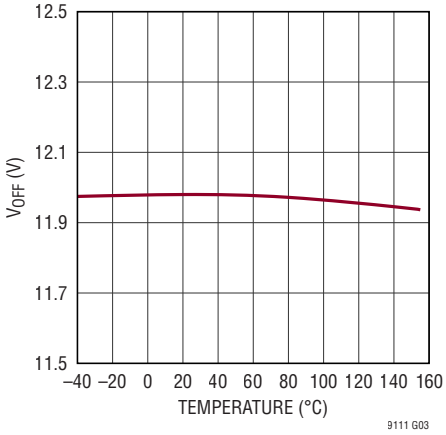
I_{IN} vs V_{IN}



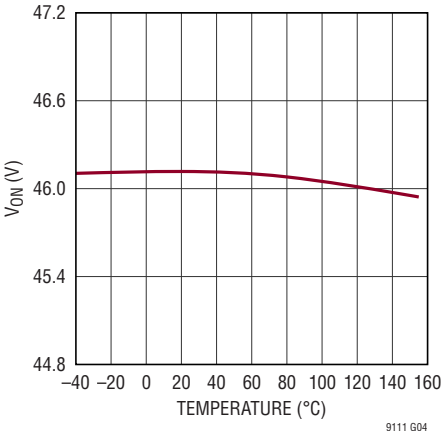
V_{ON} (Class 10 through 12) vs Temperature



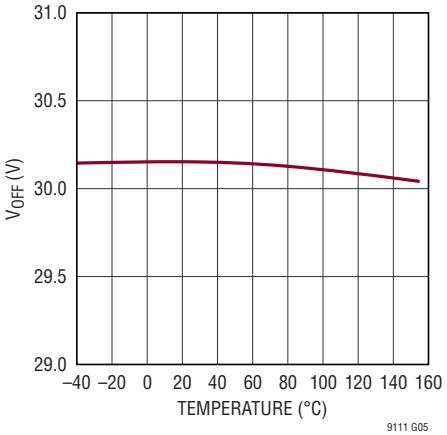
V_{OFF} (Class 10 through 12) vs Temperature



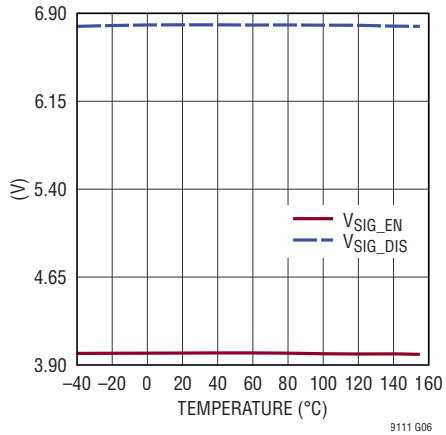
V_{ON} (Class 13 through 15) vs Temperature



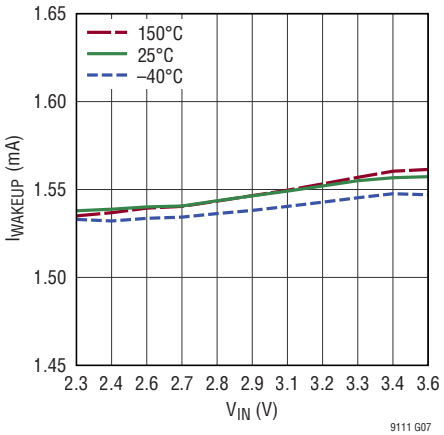
V_{OFF} (Class 13 through 15) vs Temperature



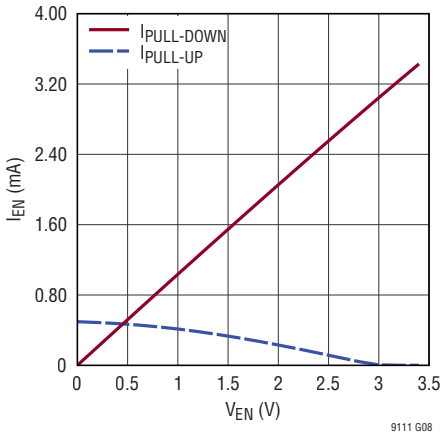
V_{SIG_EN} and V_{SIG_DIS} vs Temperature



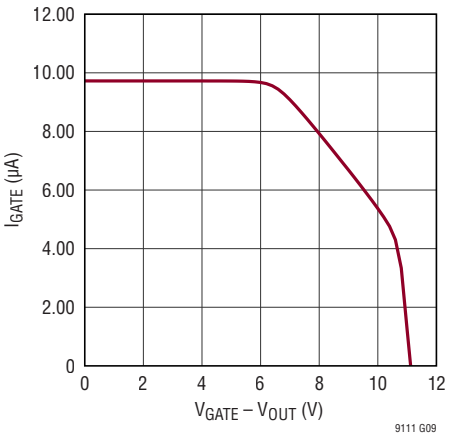
I_{WAKEUP} vs V_{IN}



V_{EN} vs I_{EN}



I_{GATE} Pull-Up



PIN FUNCTIONS (DFN, MSOP)

SNS1 (Pin 1): PD Power Interface Sense Input 1. Connect to MDI/PI connector pin 1 through the coupling network. See Applications Information for more details.

SNS2 (Pin 2): PD Power Interface Sense Input 2. Connect to MDI/PI connector pin 2 through the coupling network. See Applications Information for more details.

IN (Pin 3): Controller Supply Voltage.

STBY (Pin 4): 3.5V Low-Dropout (LDO) Regulator Output. Bypass with a 2.2µF ceramic capacitor close to the pin.

CLASSV (Pin 5): Binary PD Class Voltage Configuration Input. Tie to GND for 24V Classes (Class 10 through 12). Tie to STBY for 55V Classes (Class 13 through 15).

EN (Pin 6): Digital Enable Output. Asserts high when the port is powered on and the external hot swap MOSFET is enhanced. Connect to enable input of the PD application DC/DC converter(s).

SCCP (Pin 7): SCCP Pull-Down Gate Drive. Connect to gate of external pull-down N-channel MOSFETs for transmitting a logic 0 during classification. See Applications Information for more details.

LGATE2 (Pin 8): Low-Side Active Bridge Gate Drive 2. Connect to gate of low-side pass MOSFET connected to MDI/PI connector pin 2.

LGATE1 (Pin 9): Low-side Active Bridge Gate Drive 1. Connect to gate of low-side pass MOSFET connected to MDI/PI connector pin 1.

CLASSC (Pin 10): Ternary PD Class Current Configuration Input. Together with CLASSV pin, CLASSC pin can be tied HIGH, LOW or left unconnected to configure the LTC9111 as PD Class 10 through 15 as defined by IEEE 802.3cg. See Class Configuration section for more information.

OUT (Pin 11): PD Supply Voltage Output. For inrush control, connect to source of external N-channel MOSFET.

GATE (Pin 12): Gate Drive External N-Channel MOSFET. Capacitance to GND determines inrush time.

GND(Pin 13): Exposed Pad and Device Ground. Must be soldered to PCB ground.

OPERATION

PRODUCT OVERVIEW

The LTC9111 is the world's first IEEE 802.3cg compliant PD controller. It presents a valid wakeup signature to the PSE in order to request power. It also supports the Serial Communication Classification Protocol (SCCP) to communicates the configured voltage and current levels to the PSE during classification. The LTC9111 monitors the port voltage to control inrush and enable/disable the application appropriately and safely. The LTC9111 is designed to implement a Type E PD, compliant with a 10Base-T1L PHY. The LTC9111 does not support the optional feature of cable resistance measurement.

LTC9111 implements the necessary circuitry to implement an IEEE 802.3cg compliant PD design. The application circuit of the LTC9111 uses external MOSFETs to minimize power loss, optimize system cost, and improve fault tolerance.

The IEEE 802.3cg mandated polarity insensitivity requirement is addressed using low-side rectifying MOSFETs. External diodes are required for high-side polarity correction and back-feed prevention. The LTC9111 monitors the unrectified voltage for classification and state navigation. Input polarity is sensed and rectified automatically. The LTC9111 drives a pair of external MOSFETs when transmitting a logic low during classification, regardless of the input polarity. An external high-side MOSFET is used to isolate the load circuitry and capacitance from the PD Power Interface (PI); this allows system designers to overcome restrictions imposed by the standard.

TECHNOLOGY OVERVIEW

Power over Data Lines, or PoDL, is a standard protocol for sending DC power over two-wire copper Ethernet data cables. PoDL is similar in concept to traditional Power over Ethernet (PoE) but differs significantly in definition and implementation. The differences stem mainly from the unique power coupling techniques used in a two-wire powering circuit, as opposed to PoE's four and eight wire, pair-oriented powering techniques. PoDL enables the simultaneous transmission of power and data over a single conductor pair, e.g., balanced twisted pair or coaxial cable. Figure 1 illustrates one possible PoDL circuit architecture.

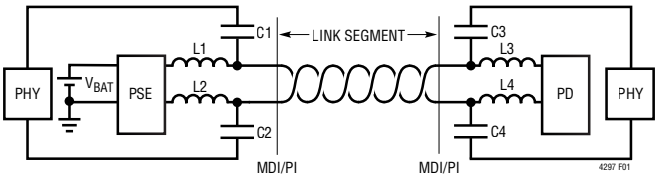


Figure 1. Basic PoDL Circuit Architecture

IEEE 802.3bu (PoDL) was ratified in 2016. Multiple complementary data standards are already ratified or are in development, ranging from 10Mbps to 10Gbps and higher. IEEE 802.3bu defines protocols for detecting, classifying, powering, disconnecting, and standby power operation. In 2019, the IEEE extended the PoDL standard (802.3cg) to accommodate long reach protocol 10Base-T1L, with cable lengths of up to 1km.

The Ethernet Alliance adopted a family of standard Power over Ethernet acronyms to differentiate the types and generations of PoE. As such, Single-Pair Power over Ethernet is referred to as SPoE and is a common name for 802.3cg technology. PoDL refers to Clause 104 in 802.3 standard.

The IEEE standard also defines PoDL terminology. A device that provides power to the network is known as power sourcing equipment, or PSE. A device that draws power from the network is known as a powered device, or PD.

PoDL BASICS

Common xBase-T1 Ethernet data connections consist of a single pair of wires, AC coupled at each end to avoid ground loops. Unlike PoE systems that transmit power common mode to the data, PoDL systems duplex power and data over a single pair of cables. IEEE 802.3cg defines the classification-based power delivery protocol for the PSE and PD. The classification protocol is defined to ensure PSE and PD class compatibility and to avoid applying power into a short circuits, open circuits, or incompatible Ethernet equipment.

Upon connection to a PD, a PSE performs detection/classification before applying full operating voltage to the PD. During classification, the PSE communicates with the PD to request information such as the PD Class, the PD Type, and cable resistance measurement support. Based on cable resistance and available power, a PSE and PD negotiate allocation of power to the PD. If the PSE determines

OPERATION

that the connected PD is compatible, it proceeds to apply full operating voltage to the PD. In order to stay fully powered, the PD is required to present a valid Maintain Full Voltage Signature (MFVS). If the PD is disconnected or goes to sleep, the PSE detects the absence of MFVS and removes full operating voltage. The PSE also removes full operating voltage in the event of a fault.

After removing the full operating voltage, the PSE provides a very low power standby voltage (3.3V). The PD can request wakeup in this condition by presenting a wakeup current signature to the PSE. Thereafter, the PSE may begin the sequence again to re-establish full operating voltage.

PORT STATE MACHINE SEQUENCE

The LTC9111 implements a voltage-driven PD state machine as defined by the IEEE 802.3cg standard. Figure 2 illustrates the time-domain sequence of powering up after the initial application of power.

In a compliant PoDL system, the PSE will initially apply voltage in the range of V_{SLEEP} (typical 3.3V). When power is first applied to the LTC9111, it enters the WAKEUP state. In the WAKEUP state, the LTC9111 alerts the PSE to its presence with a wakeup signature, I_{WAKEUP_PD} (typically 1.55mA).

An IEEE 802.3cg compliant PSE and PD perform the classification step using the Serial Communication Classification Protocol (see Power Class and SCCP) and the PSE evaluates if the PD is compatible. If it is, the PSE proceeds to ramp the port voltage.

The LTC9111 monitors the port voltage as it ramps. Once the port voltage crosses a threshold of V_{ON}, and after a mandated delay of t_{PWRDLY}, the LTC9111 enters the MDI_POWER2 state. The LTC9111 ramps up the GATE pin, turning on the external MOSFET and inrushing the application capacitance. After inrush, the EN pin is pulled high to enable the PD application.

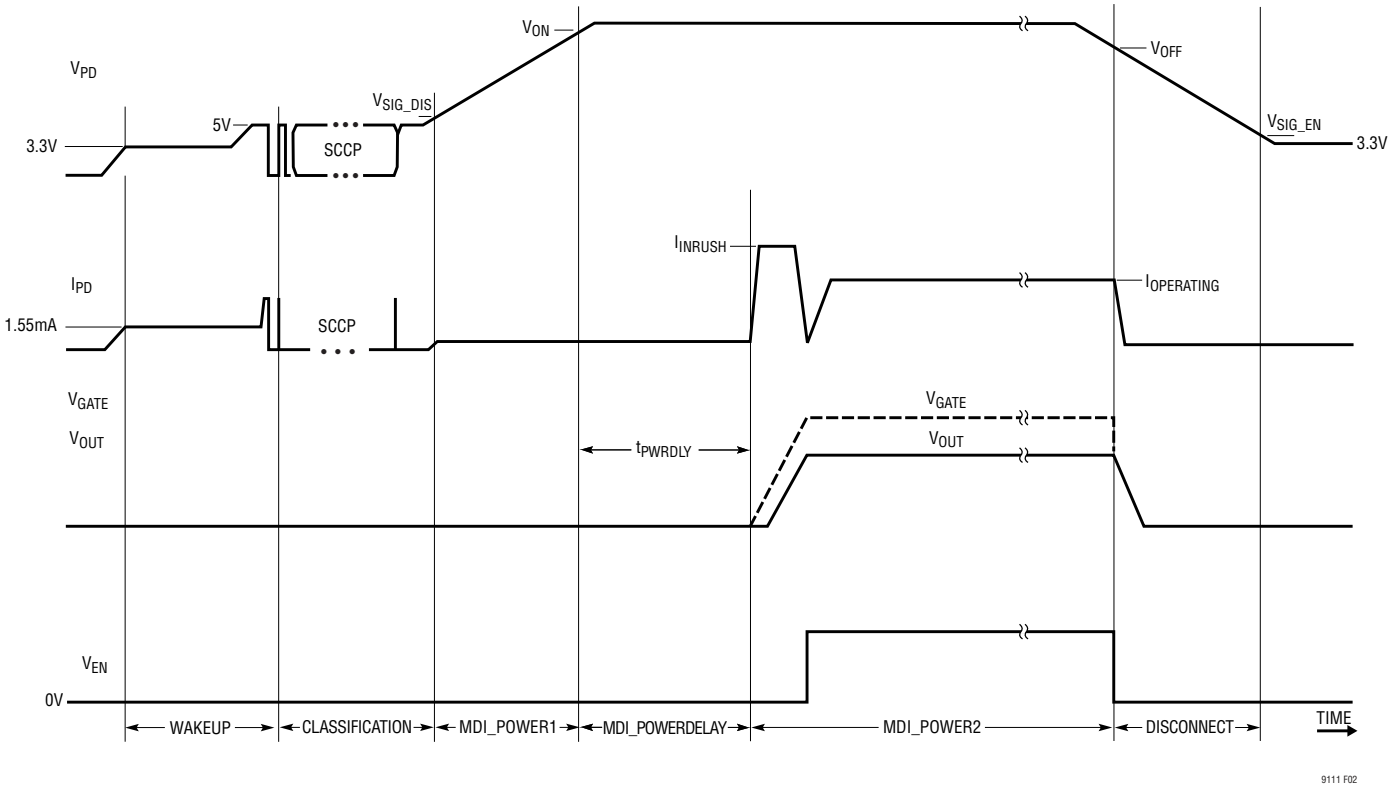


Figure 2. LTC9111 State Machine Sequence (Not to Scale)

OPERATION

Subsequently, the PSE removes full operating voltage if power becomes unavailable or if MFVS is not detected by the PSE. As the port voltage drops below V_{OFF}, the LTC9111 enters the DISCONNECT state and the application is disabled by de-asserting the EN pin. Once the PSE has discharged the port voltage to the range of V_{SLEEP}, the LTC9111 enters the WAKEUP state. Thereafter, the same sequence may be repeated to return the port to its full operating voltage. Figure 3 provides a simplified state diagram. In the following sections, each state is described in more detail.

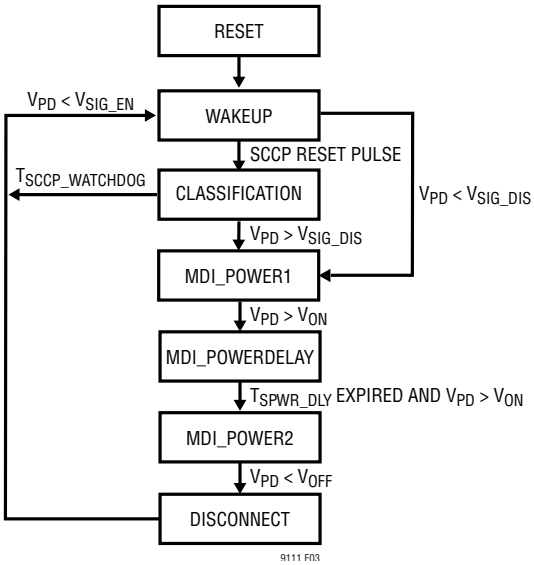


Figure 3. Simplified PD State Machine

RESET

Upon initial application of voltage, the LTC9111 begins in the RESET state. The LTC9111 ramps its internal supply and turns on one of the external low-side polarity correction MOSFETs, according to the input polarity sensed at the SNS1 and SNS2 pins. Once the low-side polarity-correcting MOSFET has been enhanced, the LTC9111 proceeds to the WAKEUP state.

WAKEUP

In the WAKEUP state, the LTC9111 presents the wakeup signature in the form of a pull-down current, I_{WAKEUP_PD} (typically 1.55mA). The wakeup signature alerts the PSE to the presence of a PD. The PSE responds by sourcing a detection probe current. Since the LTC9111 supports classification, it does not present a constant-voltage physical detection signature. A compliant PSE limits the port voltage to around 5V in the absence of a PD detection signature. After a mandated delay (maximum 3.11ms), the PSE proceeds to classification. The PSE initiates classification by sending a reset pulse. The LTC9111 detects the reset pulse and advances to the CLASSIFICATION state.

CLASSIFICATION

During classification, the LTC9111 responds to PSE commands as defined by SCCP. The protocol is explained in detail below (see Power Class and SCCP section). The PSE, in its assigned time slot, pulls down on the cable to transmit a logic low or pulls up on the cable (typically 5V to 5.5V) to transmit a logic high. The LTC9111, in its assigned time slot, pulls down on the cable to transmit a logic low or releases the cable to transmit a logic high.

The LTC9111 monitors the voltage at the SNS1 and SNS2 pins for serial data input and drives external MOSFETs using the SCCP pin to pull-down the cable voltage when transmitting a logic low.

Power cannot be delivered over the cable during pull-down time slots. During these periods, the LTC9111 maintains its state and continues operating by drawing current from the capacitor on the STBY pin. The voltage at the IN pin may collapse transiently during transmission of a logic low, depending on the leakage of the rectifying diodes and other factors. As such, the internal path from IN to STBY is designed to block reverse current during these periods and thus prevent the voltage on the STBY pin reservoir capacitor from collapsing.

After a successful classification, the PSE starts a controlled ramp of the port voltage. The LTC9111 transitions to the MDI_POWER1 state when the voltage exceeds V_{SIG_DIS}.

The LTC9111 maintains a watchdog timer, $T_{SCCP\_WATCHDOG}$ in the CLASSIFICATION state. If a fault occurs during classification or the PSE does not apply power upon completion of SCCP, the LTC9111 will return to the WAKEUP state after $T_{SCCP\_WATCHDOG}$.

OPERATION

MDI_POWER1

In the MDI_POWER1 state, the wakeup signature circuitry and SCCP pull-down are disabled. The LTC9111 current draw is reduced to I_{PD_PWR1}, allowing the PSE pull-up current to charge the cable and port capacitance. When the LTC9111 senses that its input voltage has risen above V_{ON}, it advances to the MDI_POWERDELAY state.

When in MDI_POWER1 state, if the input voltage drops below V_{SIG_ENABLE} due to a fault, the LTC9111 re-enters the WAKEUP state.

MDI_POWERDELAY

With the port voltage greater than V_{ON}, the PSE has nearly finished ramping the port to the full operating voltage. When the LTC9111 enters the MDI_POWERDELAY state, it starts a timer t_{PWRDLY} (> 80ms). This delay ensures the PSE finishes ramping the port voltage before the application is enabled, thereby preventing oscillatory behavior caused by the cable and coupling network impedance. After the timer expires, the LTC9111 enters the MDI_POWER2 state.

MDI_POWER2

When the LTC9111 enters the MDI_POWER2 state, the PSE is ready to provide the full rated class power. The external high-side MOSFET is enabled via a current source on the GATE pin (see External Component Selection section). An internal comparator monitors the GATE pin, and when the GATE pin voltage exceeds the IN pin voltage by V_{EN_ASSERT} (6.5V min), the LTC9111 asserts the logic-level EN pin. The EN pin can be used to enable the DC/DC converter or application circuitry connected to the OUT pin.

The LTC9111 remains in the MDI_POWER2 state until the port voltage drops below V_{OFF}. If the port voltage drops below V_{OFF}, the LTC9111 enters the DISCONNECT state. The port voltage may drop due to physical disconnection from the PSE or because the PSE initiated power removal.

DISCONNECT

When the LTC9111 enters the DISCONNECT state, the external high-side MOSFET is turned off and the EN pin is de-asserted. A compliant PSE will discharge the port voltage to the range of V_{SLEEP} (typically 3.3V). As the port voltage drops below V_{SIG_ENABLE}, the LTC9111 again enters the WAKEUP state.

Thereafter, the PSE may re-perform classification of the LTC9111 before applying full operating voltage to the LTC9111. A PSE may also maintain the port at the ~3.3V sleep voltage or disable the port entirely and discharge the voltage to 0V, in which case the LTC9111 will return to the RESET state.

POWER CLASS AND SCCP

Power Class is a key concept in the Power over Data Line (PoDL) standard. Class defines both the PSE output voltage range and the maximum power being sourced or drawn in the system. PoDL defines 16 Classes (0 through 15). Class 0 through 9 are defined by IEEE 802.3bu for automotive systems. Class 10 through 15 are defined by IEEE 802.3cg for discoverable systems used in building and factory automation. Classes 10 through 12 correspond to a 24V nominal PSE output voltage, as demanded by many industrial, factory automation, legacy building automation and wet locations. Each of the three 24V classes represents a different cabling definition and accompanying maximum power transfer. Classes 13 through 15 provide a 54V nominal PSE output voltage, to maximize power transfer without exceeding Safety Extra Low Voltage (SELV). Table 1 summarizes the IEEE 802.3cg PSE and PD Class pairs.

In addition to their Power Class, PoDL PSEs and PDs are identified with a Type based on their PHY compatibility. The LTC9111 is designed for PDs compatible with 10Base-T1L PHYs, which is defined as Type E.

Table 1. PSE and PD Valid Class Pairs

PSE CLASS	MAX PD POWER (W)	PD VOLTAGE (MIN) (V)	PD VOLTAGE (MAX) (V)	I_{MAX} (mA)	COMPATIBLE PD CLASS(ES)
10	1.23	14	30	92	10
11	3.2	14	30	240	10, 11
12	8.4	14	30	632	10, 11, 12
13	7.7	35	58	231	13
14	20	35	58	600	13, 14
15	52	35	58	1579	13, 14, 15

OPERATION

CLASS CONFIGURATION

The LTC9111 uses the CLASSC ternary pin and the CLASSV binary pin to configure the Power Class. The class configuration setting determines the V_{ON} and V_{OFF} thresholds for state machine navigation and is reported to the PSE during classification. The CLASSC and CLASSV pin configurations corresponding to each class are shown in Table 2.

Table 2. LTC9111 Class Configuration

PD CLASS	CLASSV	CLASSC
10	GND	GND
11	GND	FLOAT
12	GND	STBY
13	STBY	GND
14	STBY	FLOAT
15	STBY	STBY

SCCP INITIALIZATION

Every SCCP bit communication begins with a reset pulse, issued by the PSE, followed by a presence pulse response from the PD (see Figure 4). The PSE begins the reset pulse by pulling the port voltage below V_{TL} for time t_{RSTL} and then pulling up to V_{PUP}. The PD detects the reset pulse and waits for time t_{PDH} before pulling down for time t_{PDL}. This is called the PD presence pulse. The PSE samples to identify a presence pulse at time t_{MSP} starting from the end of reset pulse. Once the PSE has confirmed the presence of the PD, it continues with either a write or a read operation.

SCCP WRITE SLOT

The PSE begins a write operation by pulling down the port voltage to V_{TL} (see Figure 5). When writing a 0, the PSE pulls down for time t_{W0L}. When writing a 1, the PSE pulls down for time t_{W1L}. The PD detects the falling edge and samples the port voltage after t_{SSW} to determine the bit polarity.

SCCP READ SLOT

The PSE begins a read operation by pulling below V_{TL} for t_{W1L} (see Figure 6). If sending a 0 to the PSE, the PD detects the pull-down by the PSE and pulls down immediately for t_{R0L}. If sending a 1 to the PSE, the PD does not pull-down the port and allows the PSE to pull-up after t_{W1L}. The PSE samples the port voltage after t_{MSR}, measured from from PSE pull-down, in order to determine the bit.

PACKET SUPPORT

The LTC9111 supports and responds to the SCRATCHPAD_READ command from the PSE; this includes the PD Class (as configured with the CLASSC and CLASSV pins) and the PD Type (E).

MAINTAIN FULL VOLTAGE SIGNATURE (MFVS)

While a port is powered on, a compliant PSE monitors the port for the presence of a minimum load, called MFVS. If MFVS is not detected, PSE will remove the power to the PD. Specifically, a powered PD must draw a minimum of 11mA, for at least 10ms, every 300ms in order to stay powered on. The LTC9111 has a low operating current and will not meet the criteria for MFVS on its own. For PD applications in which the quiescent load may be less than the MFVS threshold, an appropriate minimum load may need to be added e.g., on the OUT pin.

A compliant PSE may recognize currents as low as 2.5mA as a valid MFVS. Thus, for the PD application to ensure removal of power (e.g., because it has been locally disabled), the PD must reduce its quiescent current below 2.5mA.

EXTERNAL COMPONENT SELECTION

STBY Bias Supply

An internal linear regulator produces a nominal 3.5V supply at the STBY pin. It is used to power internal control circuitry. Bypass the STBY pin with a capacitance of 2.2µF placed near the pin. In case of a ceramic chip capacitor, the effective capacitance with a bias of 3.5V should be > 1.8µF. An 0805 or larger capacitor is recommended.

OPERATION

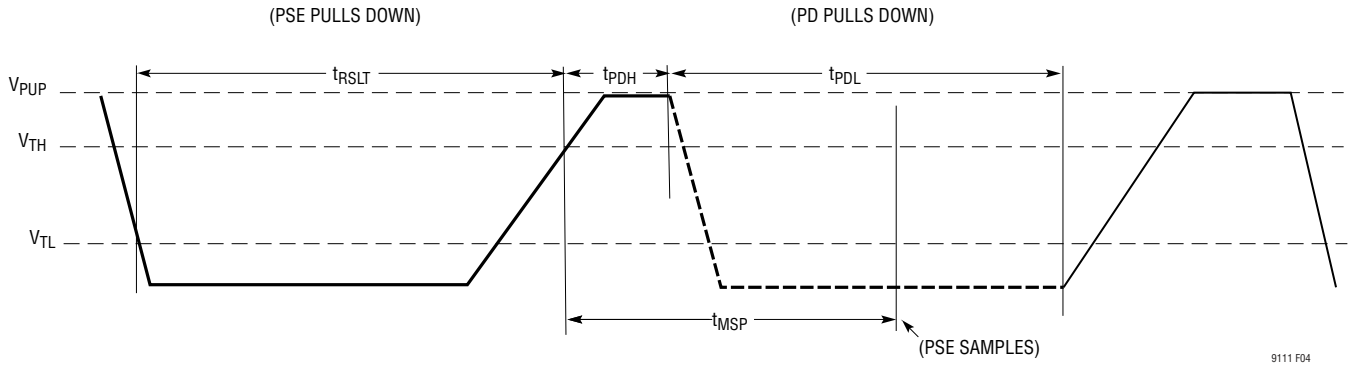


Figure 4. SCCP Initialization

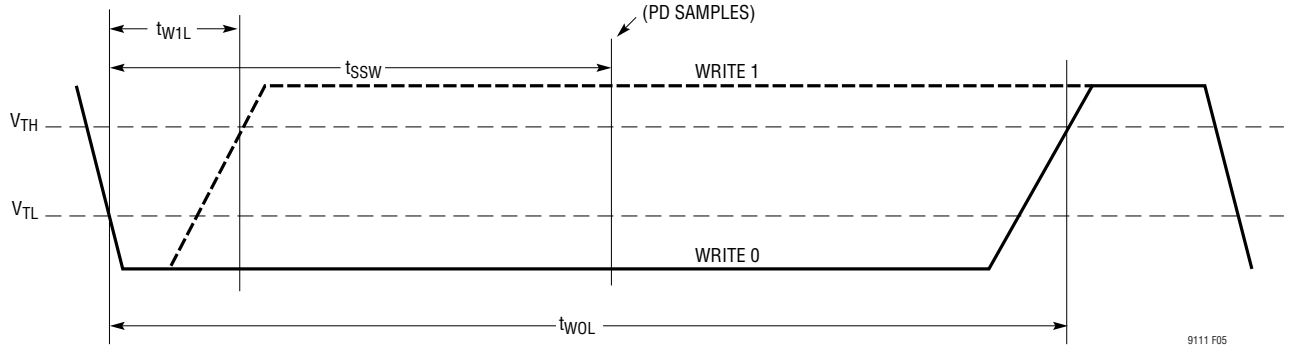


Figure 5. SCCP Write Slot

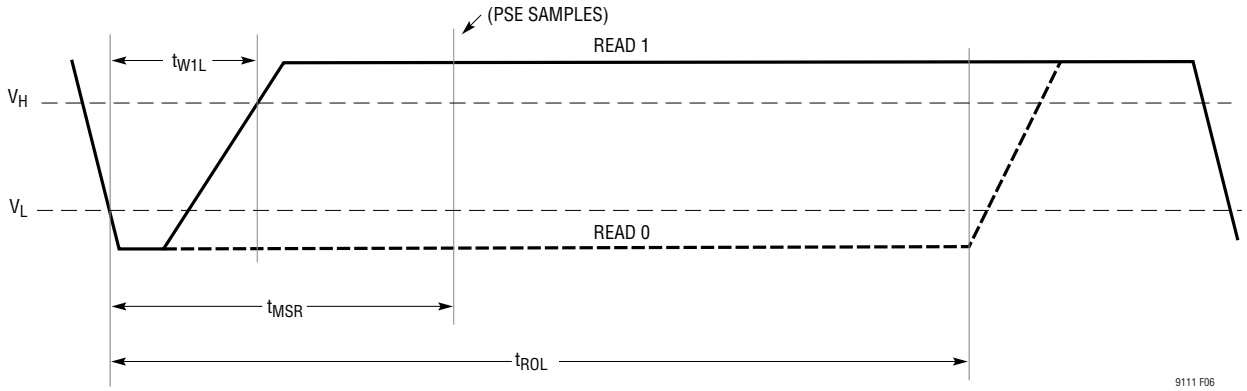


Figure 6. SCCP Read Slot

APPLICATIONS INFORMATION

Note that, during classification, the STBY pin capacitor serves as a charge reservoir to keep the chip operational when either the PSE or PD are pulling the port voltage low to signal a logical zero. Any external load on the STBY pin during classification may discharge the capacitor and cause brownout. There should be no external load on the STBY pin during classification.

External MOSFET Switch and Inrush Control

The GATE and OUT pins allow the LTC9111 to drive an external MOSFET (M1, Figure 7) as an inrush controller and load switch. An internal charge pump allows the GATE pin to be driven above the input voltage to enhance an external N-channel MOSFET. The gate driver turns on the external MOSFET upon entering the MDI_POWER2 state by sourcing I_{GATE_UP} into the GATE pin. A capacitor C_{GATE}, installed between the GATE pin and the GND pin, will produce a linear ramp at OUT and determine the inrush current based on the total bulk capacitance C_{BULK}. Use Equation 1 to ensure that the inrush current does not exceed the maximum PD current for the corresponding class.

$$C_{GATE} >> 2 \bullet C_{BULK} \bullet (I_{GATEUP}\ MAX/I_{CLASS}\ MAX) \quad (1)$$

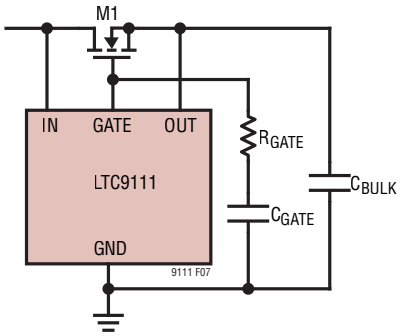


Figure 7. Inrush Control

During inrush, there can be significant transient power dissipation in the external MOSFET; SOA capability must be considered in selecting the pass device.

Any load present at the OUT pin before inrush is complete will also contribute to the total PD current observed at the connector; this may necessitate slower inrush (i.e., larger C_{GATE}). The EN logic output can be used to ensure that application load does not contribute to the PD current until the external MOSFET switch is enhanced and inrush is complete. The EN pin does not go high until GATE exceeds IN by V_{EN_ASSERT}, at which point inrush is complete.

A resistor, R_{GATE}, in series with C_{GATE} is recommended for robustness. As an example, a fault which shorts the OUT pin to ground instantaneously while power is applied will pull the source of the external MOSFET to ground while C_{GATE} maintains high voltage at the GATE pin, causing stress on the gate of the external MOSFET. A resistor value of R_{GATE} = 10k will effectively decouple the gate of the MOSFET from the capacitor in such a scenario.

When the external MOSFET switch M1 is turned off (because the PD exited the MDI_POWER2 state), the GATE pin is pulled to the OUT pin with a pull-down current of IOUT_SLEEP. Once the MOSFET has been turned off (i.e., GATE = OUT) there is an internal pull-down trickle current, I_{OUT_SLEEP}, on the OUT pin which helps ensure that the GATE and OUT pins settle to ground.

PD INPUT CAPACITANCE/SNUBBER NETWORK

The LTC9111 requires a bypass capacitance between the IN pin and ground. In order to avoid forming a highly resonant LC tank with the coupling magnetics, a snubber network should be used as shown in Figure 8. L_{PODL} is the equivalent differential inductance of the power coupling network.

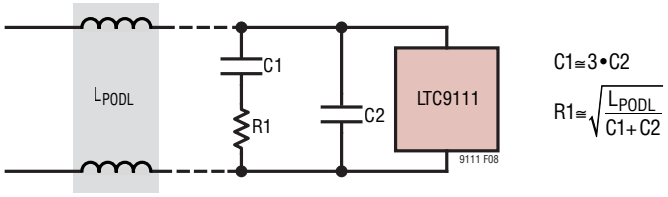


Figure 8. Snubber Network

IEEE 802.3cg specifies a maximum PD input capacitance of 400nF during classification. This ensures sufficient bandwidth for SCCP. Note that the PHY coupling capacitors and any additional snubber network on the cable side are also included in this budget.

A well damped snubber network with a total capacitance (C1 + C2) of at least 150nF will generally suffice. The voltage coefficient of the capacitor and operating voltage should be taken into consideration, as small package ceramic capacitors will generally provide only a fraction of

APPLICATIONS INFORMATION

their nominal capacitance when biased at higher voltages. If the effective capacitance is reduced under DC bias, the LC tank formed by the power coupling magnetics and the bypass capacitor will be resonant.

INPUT POLARITY CORRECTION

IEEE 802.3cg requires polarity insensitive PDs to facilitate fool-proof field installation with screw terminals. The LTC9111 drives external MOSFETs (M4/M5, Figure 9) for polarity correction on the low-side and relies on external Schottky diodes (D1/D2) to rectify the high-side voltage. Active low-side rectification minimizes power losses and also helps overcome circuit start-up challenges posed by the constraints of the standard.

When the port is first initialized, a compliant PoDL PSE will bias the port at a voltage of V_{SLEEP}, which may be as low as 3.1V. The voltage available to bias the PD controller is even lower, due to the drop ($V_{D(Schottky)}$) across the high-side rectifying diodes and the body diode of the low-side MOSFET. The LTC9111 is guaranteed to enhance the low-side rectifying MOSFET at startup, as long as the voltage between IN and GND is greater than 1.6V. Once the low-side rectifying MOSFET is on, the voltage at the input to the LTC9111 increases according to Equation 2.

$$V_{IN} = V_{SLEEP} - V_{D(Schottky)} - I_{(PORT)} \bullet R_{DS(ON)} \quad (2)$$

Since port currents are in the mA range while the port is in the WAKEUP and CLASSIFICATION states, the drop over the external MOSFET is expected to be very small. In order to ensure that the LTC9111 provides a valid wakeup signature, the voltage at the IN pin should be at least 2.3V in the WAKEUP state. The drop across a traditional silicon diode may be too high, especially at cold temperatures. For this reason, Schottky diodes are recommended for high-side rectification, even in cases where power dissipation is not critical. Since the full application current flows through the high-side Schottky diodes once the port is powered up, they must meet the current and power-dissipation requirements of the application.

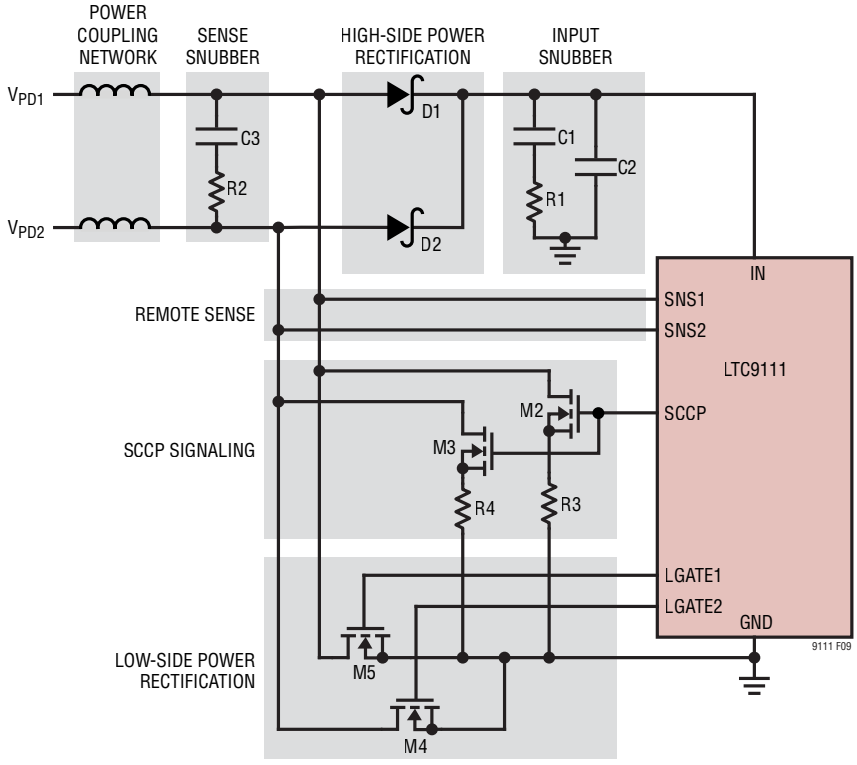


Figure 9. External Components for Power Rectification, Sensing, and SCCP

APPLICATIONS INFORMATION

The low-side polarity correcting MOSFETs should be sized appropriately for the current level of the application. The drive voltage at the LGATE1 and LGATE2 pins is compatible with modern standard-level power MOSFETs. These MOSFETs do not experience high voltage and high current simultaneously, so SOA performance is not critical.

REMOTE SENSE PINS

The SNS1 and SNS2 pins allow the LTC9111 to sense the port voltage outside the power rectifier for SCCP and accurate state machine voltage thresholds.

For most applications, the pins can be connected on the application side of the power coupling network. This prevents parasitic capacitance from corrupting the data signal and filters out excessive ringing that can be observed directly at the connector during classification. A small snubber between the SNS pins (C3/R2, Figure 9) prevents high-frequency ringing when the rectifying diodes are reverse biased during SCCP logic transitions.

SCCP PULL-DOWN MOSFET

The LTC9111 uses external MOSFETs (M2/M3, Figure 9) to pull-down the port voltage during classification in order to transmit a logic low. The use of two external MOSFETs allows successful classification regardless of input connector polarity configuration. The drive voltage at the SCCP pin is appropriate for low cost, logic-level discrete MOSFETs.

While inexpensive, commodity external MOSFETs such as the BSS123 will generally suffice for this purpose, some care may be needed to ensure that the IEEE 802.3cg standard requirements are met while protecting the components from overstress.

IEEE 802.3cg requires that a PD sink 30mA with a connector voltage of 0.8V while signaling a logic low. The SCCP pull-down must be connected in series with the power coupling network magnetics to prevent corruption of the data link by parasitic capacitances. As such, the voltage developed over the parasitic resistance of the coupling network must be included when calculating the effective pull-down strength.

Depending on the coupling network resistance and inductance, the peak transient current through the pull-down MOSFET may exceed the absolute maximum rating of some low-cost external MOSFETs. A resistor in series with the source of the SCCP pull-down can be used to reduce the peak current, provided it does not compromise the effective DC pull-down strength.

To meet the 0.8V/30mA requirement, the total SCCP pull-down path resistance needs to be less than 26.6Ω. This resistance includes the coupling network parasitic resistance, MOSFET $R_{DS(ON)}$, and any limiting resistors. Variations in the external MOSFET parameters should be accounted for when selecting an appropriate discrete MOSFET.

PD LOAD DYNAMICS

In order to protect PHY data integrity and avoid EMI issues, IEEE 802.3cg establishes specific limitations for input current dI/dt, input voltage dV/dt, and ripple voltage amplitude measured at the PI. The coupling network and PD capacitance form a filter between the application and the connector, so that AC dynamics in the application are attenuated at the connector. Additional filtering elements may be required in applications with large dynamic loads.

Filtering can be achieved with bulk capacitance at the hot swap output, a higher-order series filter network, or capacitance at the output of a step-down converter servicing the application load, as shown in Figure 10.

In addition to filtering high frequency noise generated by, for example, switching in the application circuitry, these elements play an important role in case of large transient load steps. Because of the large inductors in the power coupling network, the current provided by the PSE cannot change instantaneously. The application must have enough bulk capacitance to prevent the line voltage from browning out during a load step.

The optimal configuration of these filtering elements depends on the specific application—how much high-frequency noise it generates, and the magnitude and speed of the worst-case change in load during operation.

APPLICATIONS INFORMATION

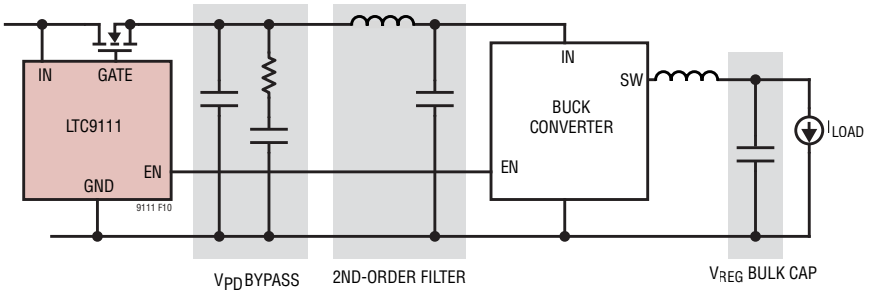


Figure 10. Filtering and Bypass for Dynamic Loads

AUXILIARY POWER

An auxiliary DC supply can be connected at the LTC9111 OUT pin or down-stream DC/DC converter output with a diode, bypassing the LTC9111 features. In this case, the auxiliary supply is responsible for inrush.

FAULT PROTECTION

PD Overload Condition

In the event of a PD current overload condition, it is anticipated that the PSE will limit the port current as mandated by IEEE 802.3cg, causing the voltage at the PD input to collapse. When the PD input voltage drops below the V_{OFF} threshold, the LTC9111 will disable the external MOSFET by pulling the GATE pin to the OUT pin and thus isolate the overload from the cable.

PD Input Short

If the inputs of the PD are shorted together after application of power, the high-side polarity correction diodes prevent the PD bulk capacitor from backfeeding through the coupling magnetics, thus protecting the LTC9111. A voltage clamp such as a TVS diode may be necessary to protect the PHY coupling capacitors and magnetics.

PD Load Dump

If the application produces a large load dump (e.g., the PD current is quickly reduced to zero from a large value), the input voltage to the LTC9111 may overshoot as the power coupling network inductors discharge. The LTC9111 provides a large transient voltage capability of 100V in order to accommodate such transients.

If other elements in the system do not have margin to cover such transients, additional application bulk capacitance can absorb the energy from the charged inductance, limiting the voltage stress experienced by the application circuitry.

PD Disconnect

If a compliant PD is disconnected from a PSE, the 802.3cg standard requires specific limits on the energy that can be back-fed at the connector. In the recommended application schematic, the high-side rectifier diodes isolate the PD bulk capacitance from the connector, guaranteeing compliance with this specification.

PD Connected to Voltage Source

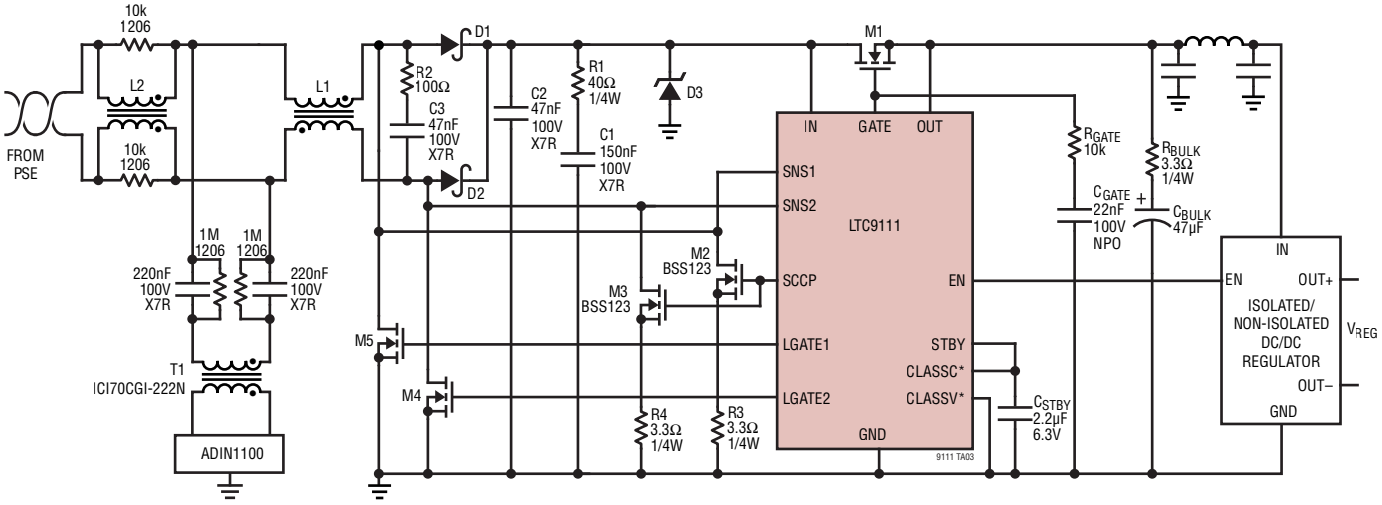
The LTC9111 is designed primarily for connection to an 802.3cg complaint, classifying PSE. When a PD is powered directly by an auxiliary power supply, the state will advance to the MDI_POWER2 state and enable the application, provided the supply voltage exceeds V_{ON} for the configured class. Note that the LTC9111 does not implement current limit or circuit breaker functionality.

OV Protection for 24V Classes

When the LTC9111 is configured for Class 10 through 12 (i.e., CLASSV pin is tied low), an overvoltage protection feature is enabled to protect downstream elements in the application from exposure to excessive voltage. When the input voltage exceeds V_{OV} (40V max), the gate of the external hot swap MOSFET will be turned off, regardless of the port state.

TYPICAL APPLICATION

Circuit for Classes 10 through 14



*CLASSC/CLASSV TO BE CONFIGURED AS STATED IN TABLE 3.

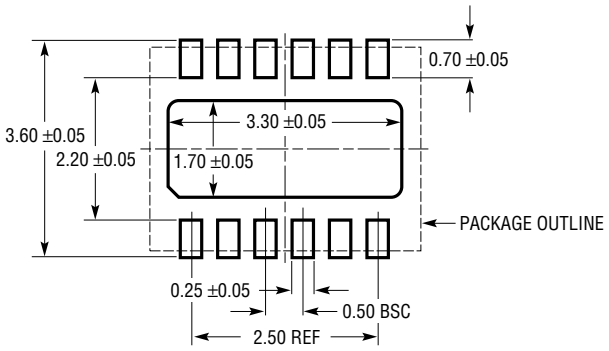
PARTS SUITABLE FOR ALL CLASSES
INPUT BRIDGE RECTIFIER HIGH SIDE DIODES (D1, D2): NEXPERIA, PMEG10020AELRX
INPUT BRIDGE RECTIFIER LOW SIDE FETS (M4, M5): NEXPERIA, BUK9M120-100EX OR
DUAL FET: NEXPERIA, BUK9K134-100EX
SCCP PULLDOWN FETS (M2, M3): ONSEMI, BSS123LT1G
INPUT TVS (D3): NEXPERIA, PTVS58VP1UTP
PD HOT SWAP FET (M1): NEXPERIA, PSMN075-100MSEX

Table 3. Recommendations for IEEE 802.3cg Classes

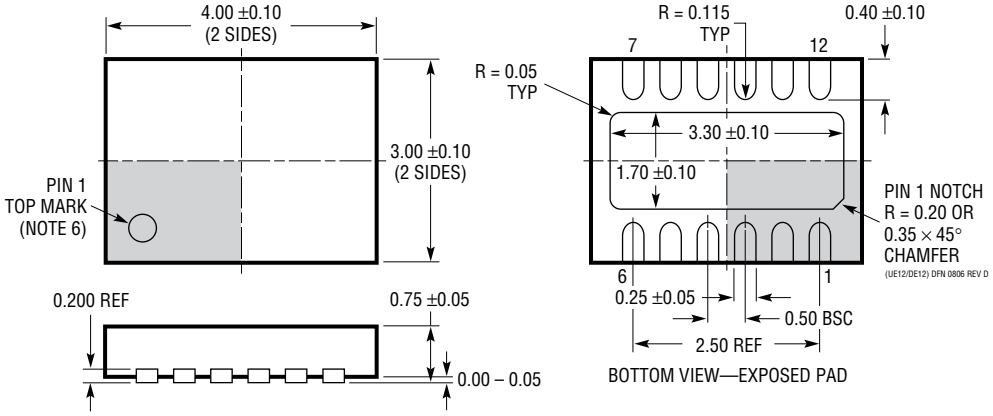
IEEE 802.3cg PSE CLASS	SPoE INDUCTOR (L1)	POWER + DATA CMC (L2)	OUTPUT BULK CAPACITOR (C_{BULK})	CLASSV	CLASSC
CLASS 10	MSD7342-683 PID75-650M	DR334A-474BE B82793C0474N215	47µF, 50V	GND	GND
CLASS 11					FLOAT
CLASS 12	MSD1048H-683 PID100-650M	SRF0905A-471Y RCM70CGI-471N			STBY
CLASS 13	MSD7342-683 PID75-650M	DR334A-474BE B82793C0474N215	47µF, 100V	STBY	GND
CLASS 14	MSD1048H-683 PID100-650M	SRF0905A-471Y RCM70CGI-471N			FLOAT

PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



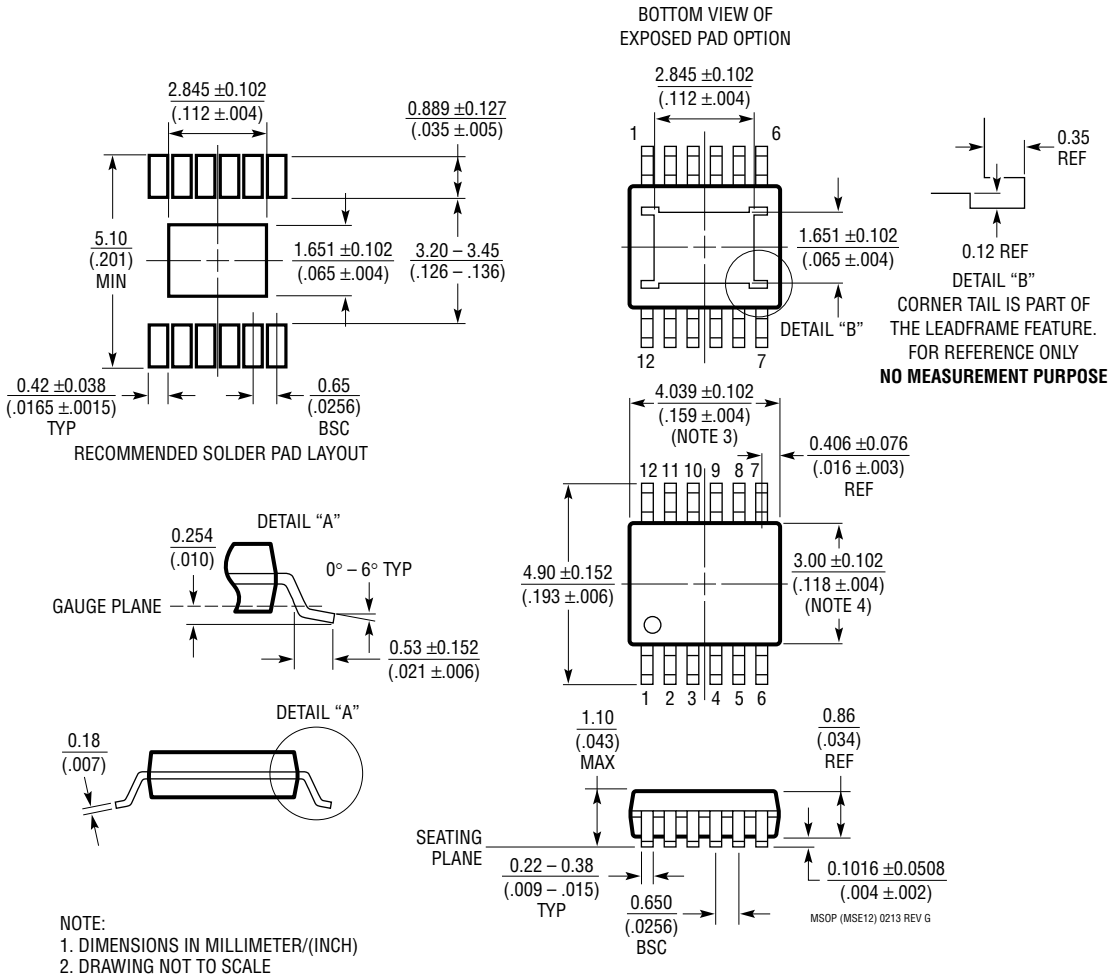
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION
   (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

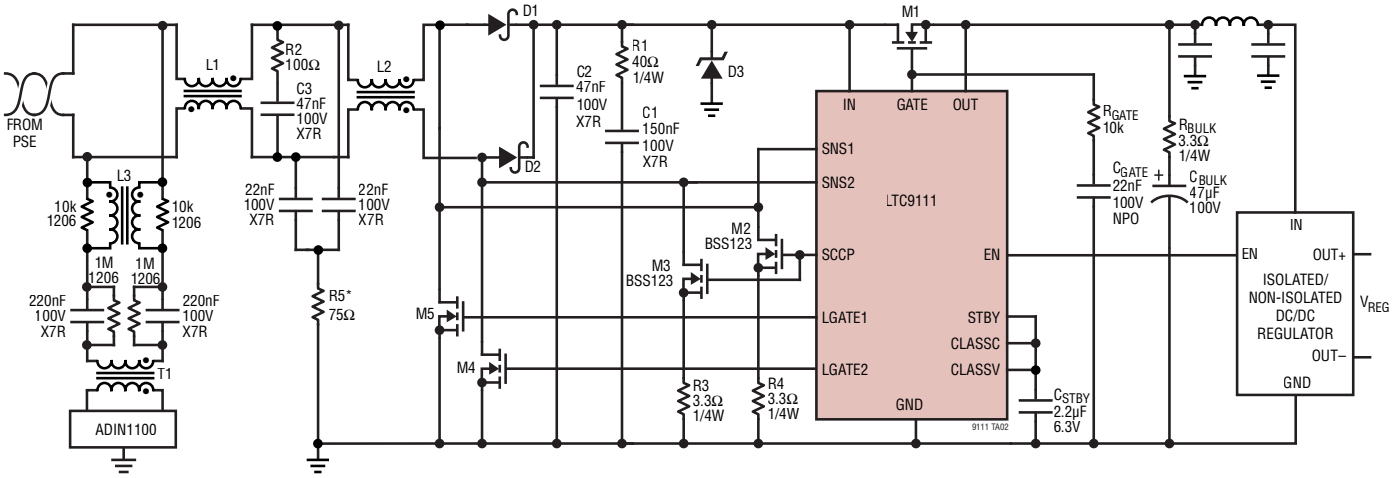
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

Circuit for Class 15: 55V, 52W



*R5 VALUE DEPENDS ON COMMON MODE IMPEDANCE OF CABLE.

SPoE DIFFERENTIAL INDUCTOR (L1):
TDK, PID120H-560M
COILCRAFT, MSD1278H-563

SPoE COMMON MODE CHOKE (L2):
BOURNS, SRF1306-600Y

DATA COMMON MODE CHOKE (L3):
BOURNS, DR334A-475ME
TDK, B82793C0475N265

DATA TRANSFORMER (T1):
TDK, ICI70CGI-222N

INPUT BRIDGE RECTIFIER HIGH SIDE DIODES (D1, D2):
NEXPERIA, PMEG10020AELRX

INPUT BRIDGE RECTIFIER LOW SIDE FETS (M4, M5):
NEXPERIA, BUK9M120-100EX
DUAL FET: NEXPERIA, BUK9K134-100EX

SCCP PULLDOWN FETS (M2, M3):
ONSEMI, BSS123LT1G

INPUT TVS (D3):
NEXPERIA, PTVS58VP1UTP

PD HOT SWAP FET (M1):
NEXPERIA, PSMN075-100MSEX

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4296-1	IEEE 802.3cg SPoE 5-port PSE Controller	Transformer Isolation, Fully Compliant IEEE 802.3bt Type 3 and Type 4; Supports IEEE 802.3af, IEEE 802.3at and IEEE 802.3bt PDs
ADIN1100	IEEE 802.3cg 10Base-T1L Ethernet PHY	Low Power, Single Port Transceiver; Compliant with IEEE 802.3cg-2019 Ethernet Standard for Long Reach SPE
ADIN2111	Low Complexity, 2-Port Ethernet Switch with Integrated 10Base-T1L PHYs	Low Power, Low Complexity, Two-Ethernet Ports Switch and One SPI Port
ADIN1110	Robust, Industrial, Low Power 10Base-T1L Ethernet MAC-PHY	Ultralow Power, Single Port Transceiver; Compliant with IEEE 802.3cg-2019 Ethernet Standard for Long Reach SPE
LT8301	42V_{IN} Micropower No-Opto Isolated Flyback Converter with 65V/1.2A Switch	Low I_Q Monolithic No-Opto Flyback 5-Lead TSOT-23
LT8303	100V_{IN} Micropower Isolated Flyback Converter with 150V/450mA Switch	Low I_Q Monolithic No-Opto Flyback, 5-Lead TSOT-23
LT8331	Low I_Q Boost/SEPIC/Flyback/Inverting Converter with 0.5A, 140V Switch	V_{IN} = 4.5V to 100V, $V_{OUT(MAX)}$ =140V, I_Q = 6µA (Burst Mode® Operation), MSOP-16(12)E Package
LT8309	Secondary-Side Synchronous Rectifier Driver	4.5V ≤ V_{CC} ≤ 40V, Fast Turn-On and Turn-Off, 5-Lead TSOT-23
LT8607	42V, 750mA, 93% Efficiency, 2.2MHz Synchronous Step-Down DC/DC Converter	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.778V, I_Q = 6µA, I_{SD} < 1µA, MSOP-10E Package
LT8619	60V, 1.2A Synchronous Monolithic Buck Regulator with 6µA Quiescent Current	V_{IN} = 3V to 60V, $V_{OUT(MIN)}$ = 3.3V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-16E Packages
LT8641	65V, 3.5A Synchronous Step-Down Silent Switcher® with 2.5µA Quiescent Current	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.81V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18