# Pseudo Differential Input, Quad, 4 MSPS Simultaneous Sampling, 16-Bit/14-Bit, SAR ADC

## FEATURES

- 16-bit and 14-bit ADC family
- Quad simultaneous sampling
- Pseudo differential analog inputs
- High throughput rate: 4 MSPS
- SNR: 86.7 dB (typical) at $V_{REF}$ = 3.3 V (AD7383-4)
- On-chip oversampling function
- SNR: 91 dB (typical) with OSR = 8×, RES = 1
- 2-bit resolution boost
- Out of range indicator ($\overline{ALERT}$)
- INL: 3.8 LSBs (maximum)
- High speed serial interface
- Temperature range: −40°C to +125°C
- 24-lead, 4 mm × 4 mm LFCSP

## APPLICATIONS

- Motor control position feedback
- Motor control current sense
- Data acquisition systems
- Erbium-doped fiber amplifier (EDFA) applications
- Inphase and quadrature demodulation

## PRODUCT HIGHLIGHTS

1. Quad simultaneous sampling and conversion.
2. Pin-compatible product family.
3. High 4 MSPS throughput rate.
4. Space-saving 4 mm × 4 mm LFCSP.
5. Integrated oversampling block to increase dynamic range, reduce noise, and reduce SCLK speed requirements.
6. Pseudo differential analog inputs.
7. Small sampling capacitor reduces amplifier drive burden.

## FUNCTIONAL BLOCK DIAGRAM

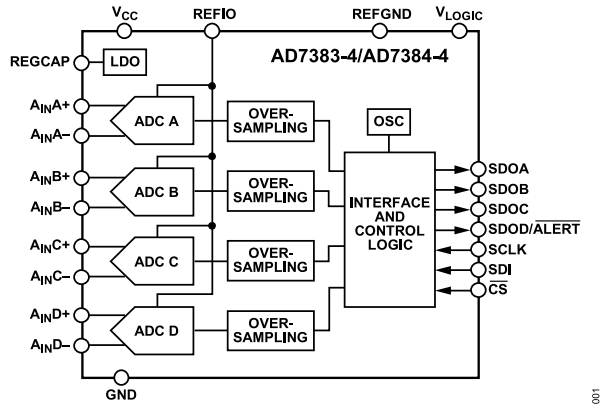


*Figure 1. Functional Block Diagram*

## GENERAL DESCRIPTION

The 16-bit AD7383-4 and 14-bit AD7384-4 are pin-compatible, quad, simultaneous sampling, high speed, successive approximation register (SAR), analog-to-digital converters (ADCs) operating from a 3.0 V to 3.3 V power supply with throughput rates up to 4 MSPS. The analog input type is a pseudo differential and is sampled and converted on the falling edge of $\overline{CS}$.

The AD7383-4/AD7384-4 have on-chip oversampling blocks to improve dynamic range and reduce noise at lower bandwidths. The oversampling boosts up to two bits of added resolution. A buffered internal 2.5 V reference is included. Alternatively, an external reference up to 3.3 V can be used.

The conversion process and data acquisition use standard control inputs allowing easy interfacing to microprocessors or digital signal processors (DSPs). The conversion result can clock out simultaneously via 4-wire mode for faster throughput or via 1-wire serial mode when slower throughput is allowed. The devices are compatible with 1.8 V, 2.5 V, and 3.3 V interfaces using the separate logic supply.

The AD7383-4/AD7384-4 are available in a 24-lead, 4 mm × 4 mm LFCSP and a temperature range of −40°C to +125°C.

*Table 1. Related Devices*

| No. of Channels | Input Type | 16 Bits | 14 Bits | 12 Bits |
|---|---|---|---|---|
| 4 | Differential | AD7380-4<br>AD7389-4 | AD7381-4 | |
| 2 | Differential | AD7380<br>AD4680<br>AD4681 | AD7381 | |
| | Single-ended | AD7386 | AD7387 | AD7388 |

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## REVISION HISTORY

**4/2023—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, reference voltage ($V_{REF}$) external = 2.5 V to 3.3 V, sampling frequency ($f_{SAMPLE}$) = 4 MSPS, $T_A$ = −40°C to +125°C, and no oversampling enabled, unless otherwise noted. SDOA, SDOB, SDOC, and SDOD are connected with a 100 Ω series resistor.

***Table 2. AD7383-4***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 16 | | | Bits |
| THROUGHPUT | | | | | |
| Conversion Rate | | | | 4 | MSPS |
| DC ACCURACY | | | | | |
| No Missing Codes | | 16 | | | Bits |
| Differential Nonlinearity (DNL) Error | | −0.9 | ±0.6 | +0.9 | LSB |
| Integral Nonlinearity (INL) Error | External reference | −3.8 | ±1.4 | +3.8 | LSB |
| | Internal reference | | ±1.7 | | |
| Gain Error | External reference = 3.3 V | −0.07 | ±0.02 | +0.07 | % FS[1] |
| | Internal reference = 2.5 V | | ±0.02 | | |
| Gain Error Drift | | −2 | ±0.3 | +2 | ppm/°C |
| Gain Error Match | | | ±0.03 | +0.08 | % FS[1] |
| Zero Error | External reference | −1.1 | ±0.05 | +1.1 | mV |
| | Internal reference | | ±0.15 | | |
| Zero Error Temperature Drift | | −5 | ±1 | +5 | µV/°C |
| Zero Error Match | | | ±0.2 | +1.2 | mV |
| AC ACCURACY | Input frequency ($f_{IN}$) = 1 kHz | | | | |
| Dynamic Range | $V_{REF}$ = 3.3 V (external) | | 87 | | dB |
| | Internal reference = 2.5 V | | 86 | | dB |
| Oversampled Dynamic Range | OSR = 4×, RES = 1 (decimal) | | 92.5 | | dB |
| Signal-to-Noise Ratio (SNR) | $V_{REF}$ = 3.3 V (external), $V_{CC}$ = 3.3 V | 82.9 | 86.7 | | dB |
| | Internal reference = 2.5 V | | 85.1 | | dB |
| | Rolling average OSR = 8×, RES = 1 (decimal), external reference | | 94.7 | | dB |
| | $f_{IN}$ = 100 kHz,$V_{REF}$ = 3.3 V (external) | | 85.5 | | dB |
| Spurious-Free Dynamic Range (SFDR) | | | 100 | | dB |
| Total Harmonic Distortion (THD) | $V_{REF}$ = 3.3 V (external) | | −98 | | dB |
| | $f_{IN}$ = 100 kHz | | −90 | | dB |
| Signal-to-Noise and Distortion (SINAD) | $V_{REF}$ = 3.3 V (external) | 83.3 | 86.4 | | dB |
| | Internal reference | | 84.6 | | dB |
| Channel to Channel Isolation | | | −110 | | dB |
| POWER SUPPLIES | | | | | |
| $V_{CC}$ Current ($I_{VCC}$) | Normal mode (operational) | | 39.3 | 43 | mA |
| Power Dissipation | | | | | |
| Total Power ($P_{TOTAL}$) | | | 169 | 186.6 | mW |
| $V_{CC}$ Power ($P_{VCC}$) | Normal mode (operational) | | 141.5 | 154.8 | mW |

[1] These specifications include full temperature range variation, but they do not include the error contribution from the external reference.

## SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, $V_{REF}$ = 2.5 V to 3.3 V, $f_{SAMPLE}$ = 4 MSPS, $T_A$ = −40°C to +125°C, and no oversampling enabled, unless otherwise noted. SDOA, SDOB, SDOC, and SDOD are connected with 100 Ω series resistor.

***Table 3. AD7384-4***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 14 | | | Bits |
| THROUGHPUT | | | | | |
| Conversion Rate | | | | 4 | MSPS |
| DC ACCURACY | | | | | |
| No Missing Codes | | 14 | | | Bits |
| DNL Error | | −0.9 | ±0.3 | +0.9 | LSB |
| INL Error | External reference = 3.3 V | −1.0 | ±0.35 | +1.0 | LSB |
| | Internal reference | | ±0.5 | | LSB |
| Gain Error | External reference = 3.3 V | −0.07 | ±0.02 | +0.07 | % FS[1] |
| | Internal reference | | ±0.01 | | |
| Gain Error Drift | | −2 | ±0.3 | +2 | ppm/°C |
| Gain Error Match | | | ±0.03 | +0.08 | % FS |
| Zero Error | External reference = 3.3 V | −1.1 | ±0.1 | +1.1 | mV |
| | Internal reference | | ±0.04 | | mV |
| Zero Error Temperature Drift | | −5 | ±1 | +5 | µV/°C |
| Zero Error Match | | | 0.2 | +1.2 | mV |
| AC ACCURACY | Input frequency ($f_{IN}$) = 1 kHz | | | | |
| Dynamic Range | $V_{REF}$ = 3.3 V | | 84 | | dB |
| | Internal reference = 2.5 V | | 83 | | dB |
| Oversampled Dynamic Range | OSR = 4×, RES = 1 (decimal) | | 90 | | dB |
| SNR | $V_{REF}$ = 3.3 V (external), $V_{CC}$ = 3.3 V | 81.5 | 83.5 | | dB |
| | Internal reference = 2.5 V | | 82.7 | | dB |
| | Rolling average OSR = 8×, RES = 1 (decimal), external reference | | 91.3 | | dB |
| | $f_{IN}$ = 100 kHz | | 82.8 | | dB |
| SFDR | | | 100 | | dB |
| THD | $V_{REF}$ = 3.3 V (external) | | −98 | | dB |
| | $f_{IN}$ = 100 kHz | | −90 | | dB |
| SINAD | $V_{REF}$ = 3.3 V (external) | 80.8 | 83.4 | | dB |
| | | | 82.4 | | dB |
| Channel to Channel Isolation | | | −110 | | dB |
| POWER SUPPLIES | | | | | |
| $I_{VCC}$ | Normal mode (operational) | | 39 | 43 | mA |
| Power Dissipation | | | | | |
| $P_{TOTAL}$ | | | 169 | 186.6 | mW |
| $P_{VCC}$ | Normal mode (operational) | | 141.5 | 154.8 | mW |

[1] These specifications include full temperature range variation, but they do not include the error contribution from the external reference.

## SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, external $V_{REF}$ = 2.5 V to 3.3 V, $T_A$ = −40°C to +125°C, and no oversampling enabled, unless otherwise noted. SDOA, SDOB, SDOC, and SDOD are connected with 100 Ω series resistor.

***Table 4. All Devices***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ANALOG INPUT | | | | | |
| Voltage Range | $A_{IN}x+ - A_{IN}x-$ | $-V_{REF}$ | | $+V_{REF}$ | V |
| Absolute Input Voltage | $A_{IN}x+$, $A_{IN}x-$ | −0.1 | | $V_{REF}$ + 0.1 | V |
| Common-Mode Input Range | $A_{IN}x+$, $A_{IN}x-$ | 0.2 | $V_{REF}$ × 0.5 | $V_{REF}$ − 0.2 | V |
| Analog Input Common-Mode Rejection Ratio (CMRR) | $f_{IN}$ = 500 kHz | | −76 | | dB |
| DC Leakage Current | | | 0.1 | 1 | µA |
| Input Capacitance | Track mode | | 18 | | pF |
| | Hold mode | | 5 | | pF |
| SAMPLING DYNAMICS | | | | | |
| Input Bandwidth | At −0.1 dB | | 6.6 | | MHz |
| | At −3 dB | | 26.8 | | MHz |
| Aperture Delay | | | 2 | | ns |
| Aperture Delay Match | | | 46.8 | 145 | ps |
| Aperture Jitter | | | 20 | | ps |
| REFERENCE INPUT AND OUTPUT ($V_{REF}$) | | | | | |
| Input Voltage Range | External reference | 2.49 | | 3.4 | V |
| Input Current | External reference | | 0.91 | 0.97 | mA |
| Output Voltage | −40°C to +125°C | 2.495 | 2.5 | 2.505 | V |
| Temperature Coefficient | | | 2 | 10 | ppm/°C |
| Noise | | | 7 | | µV RMS |
| DIGITAL INPUTS (SCLK, SDI, AND $\overline{CS}$) | | | | | |
| Logic Levels | | | | | |
| Input Voltage Low ($V_{IL}$) | $V_{LOGIC}$ < 2.3 V | | | 0.45 | V |
| | $V_{LOGIC}$ ≥ 2.3 V | | | 0.7 | V |
| Input Voltage High ($V_{IH}$) | $V_{LOGIC}$ < 2.3 V | $V_{LOGIC}$ − 0.45 | | | V |
| | $V_{LOGIC}$ ≥ 2.3 V | 0.8 × $V_{LOGIC}$ | | | V |
| Input Current Low ($I_{IL}$) | | −1 | | +1 | µA |
| Input Current High ($I_{IH}$) | | −1 | | +1 | µA |
| DIGITAL OUTPUTS (SDOA, SDOB, SDOC, AND SDOD/$\overline{ALERT}$) | | | | | |
| Output Coding | | Twos complement | | | Bits |
| Output Voltage Low ($V_{OL}$) | Current sink ($I_{SINK}$) = 300 µA | | | 0.4 | V |
| Output Voltage High ($V_{OH}$) | Current source ($I_{SOURCE}$) = −300 µA | $V_{LOGIC}$ − 0.3 | | | V |
| Floating State Leakage Current | | | | ±1 | µA |
| Floating State Output Capacitance | | | 10 | | pF |
| POWER SUPPLIES | | | | | |
| $V_{CC}$ | | | | | |
| | | 3.0 | 3.3 | 3.6 | V |
| | External reference = 3.3 V | 3.3 | | 3.6 | V |
| $V_{LOGIC}$ | | 1.65 | | 3.6 | V |
| $I_{VCC}$ | | | | | |
| Normal Mode (Static) | | | 2.6 | 3.2 | mA |
| Shutdown Mode | | | 104 | 200 | µA |
| $V_{LOGIC}$ Current ($I_{VLOGIC}$) | Analog inputs at positive full scale | | | | |

## SPECIFICATIONS

*Table 4. All Devices (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Normal Mode (Static) | | | 155 | 400 | nA |
| Normal Mode (Operational) | | | 7.6 | 8.9 | mA |
| Shutdown Mode | | | 155 | 400 | nA |
| Power Dissipation | | | | | |
| $P_{VCC}$ | | | | | |
| Normal Mode (Static) | | | 9.3 | 11.5 | mW |
| Shutdown Mode | | | 375 | 720 | µW |
| $V_{LOGIC}$ Power ($P_{VLOGIC}$) | Analog inputs at positive full scale | | | | |
| Normal Mode (Static) | | | 0.55 | 1.4 | µW |
| Normal Mode (Operational) | | | 27.3 | 31.8 | mW |
| Shutdown Mode | | | 0.55 | 1.4 | µW |

## TIMING SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, $V_{REF}$ = 2.5 V, and $T_A$ = −40°C to +125°C, unless otherwise noted. When referencing a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed, such as $\overline{ALERT}$. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

*Table 5. Timing Specifications*

| Parameter | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|
| $t_{CYC}$ | 250 | | | ns | Time between conversions |
| $t_{SCLKED}$ | 5 | | | ns | $\overline{CS}$ falling edge to first SCLK falling edge |
| $t_{SCLK}$ | 12.5 | | | ns | SCLK period |
| $t_{SCLKH}$ | 5.5 | | | ns | SCLK high time |
| $t_{SCLKL}$ | 5.5 | | | ns | SCLK low time |
| $t_{CSH}$ | 20 | | | ns | $\overline{CS}$ pulse width |
| $t_{QUIET}$ | 20 | | | ns | Interface quiet time prior to conversion |
| $t_{SDOEN}$ | | | 5.5 | ns | $\overline{CS}$ low to SDOA and SDOB enabled |
| $t_{SDOH}$ | 3 | | | ns | SCLK rising edge to SDOA and SDOB hold time |
| $t_{SDOS}$ | | | 5 | ns | SCLK rising edge to SDOA and SDOB setup time |
| $t_{SDOT}$ | | | 8 | ns | $\overline{CS}$ rising edge to SDOA and SDOB high impedance |
| $t_{SDIS}$ | 4 | | | ns | SDI setup time prior to SCLK falling edge |
| $t_{SDIH}$ | 4 | | | ns | SDI hold time after SCLK falling edge |
| $t_{SCLKCS}$ | 0 | | | ns | SCLK rising edge to $\overline{CS}$ rising edge |
| $t_{CONVERT}$ | | | 190 | ns | Conversion time |
| $t_{ACQUIRE}$ | 110 | | | ns | Acquire time |
| $t_{RESET}$ | | 250 | | ns | Valid time to start conversion after soft reset |
| | | 800 | | ns | Valid time to start conversion after hard reset |
| $t_{POWERUP}$ | | | | | Supply active to conversion |
| | | | 5 | ms | First conversion allowed |
| | | | 11 | ms | Settled to within 1% with internal reference |
| | | | 5 | | Settled to within 1% with external reference |
| $t_{REGWRITE}$ | | | 5 | ms | Supply active to register read write access allowed |
| $t_{STARTUP}$ | | | | | Exiting shutdown mode to conversion |
| | | | 10 | µs | Settled to within 1% with external reference |
| $t_{CONVERT0}$ | 6 | 8 | 10 | ns | Conversion time for first sample in OS normal mode |
| $t_{CONVERTx}$ | | | | | Conversion time for xth sample in OS normal mode, 4 MSPS, 16-bit devices |
| | $t_{CONVERT0}$ + (320 × (x − 1)) | | | ns | For AD7383-4 |
| | $t_{CONVERT0}$ + (250 × (x − 1)) | | | ns | For AD7384-4 |

## SPECIFICATIONS

*Table 5. Timing Specifications (Continued)*

| Parameter | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|
| $t_{ALERTS}$ | | | 220 | ns | Time from $\overline{CS}$ to $\overline{ALERT}$ indication |
| $t_{ALERTC}$ | | | 10 | ns | Time from $\overline{CS}$ to $\overline{ALERT}$ clear |
| $t_{ALERTS\_NOS}$ | | | 20 | ns | Time from internal conversion with exceeded threshold to $\overline{ALERT}$ indication |

## Timing Diagrams

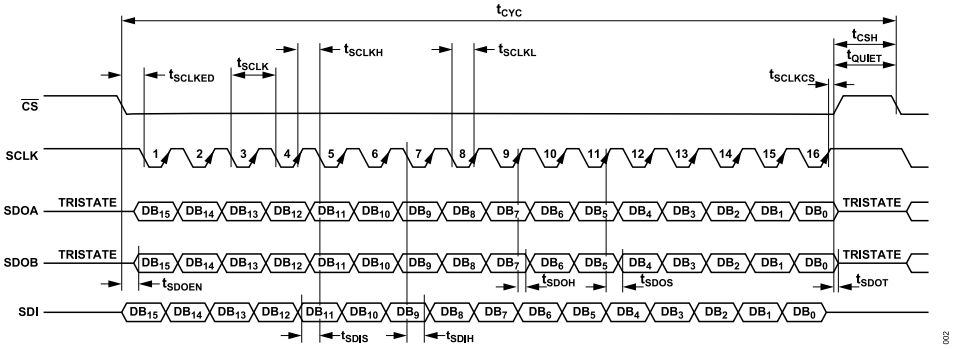


*Figure 2. Serial Interface Timing Diagram*

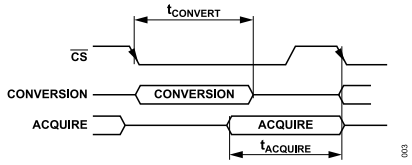


*Figure 3. Internal Conversion Acquire Timing*

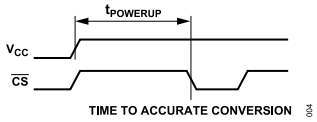


*Figure 4. Power-Up Time to Conversion*

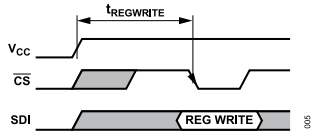


*Figure 5. Power-Up Time to Register Read Write Access*

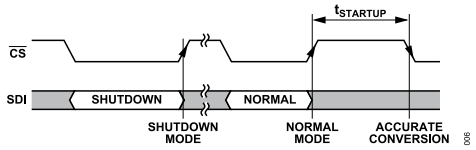


*Figure 6. Shutdown Mode to Normal Mode Timing*

## SPECIFICATIONS

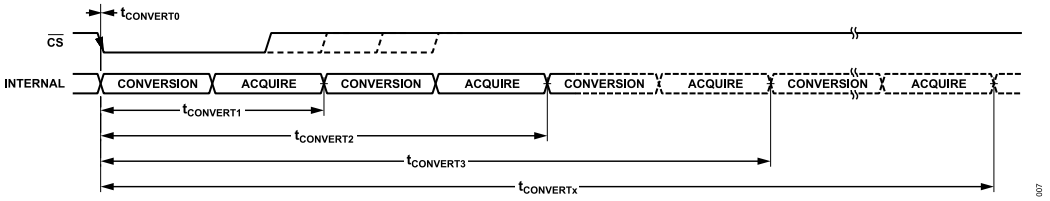


*Figure 7. Conversion Timing During OS Normal Mode*

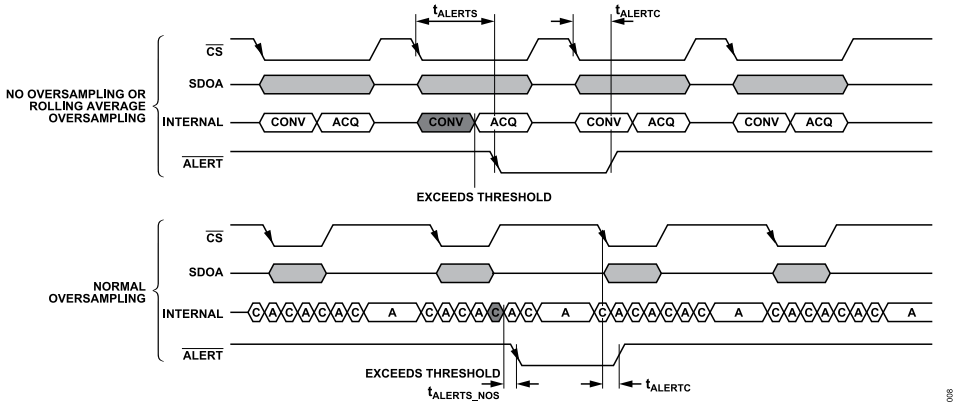


*Figure 8. $\overline{\text{ALERT}}$ Timing*

## ABSOLUTE MAXIMUM RATINGS

*Table 6. Absolute Maximum Ratings*

| Parameter | Rating |
|---|---|
| $V_{CC}$ to GND | −0.3 V to +4 V |
| $V_{LOGIC}$ to GND | −0.3 V to +4 V |
| Analog Input Voltage to GND | −0.3 V to $V_{REF}$ + 0.3 V or $V_{CC}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to $V_{LOGIC}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $V_{LOGIC}$ + 0.3 V |
| REFIO Input to GND | −0.3 V to $V_{CC}$ + 0.3 V |
| Input Current to Any Pin Except Supplies | ±10 mA |
| Temperature | |
| Operating Range | −40°C to +125°C |
| Storage Range | −65°C to +150°C |
| Maximum Junction | 150°C |
| Pb-Free Soldering Reflow | 260°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. $\theta_{JC}$ is the junction to case thermal resistance.

*Table 7. Thermal Resistance*

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| CP-24-25[1] | 48.4 | 0.43[1] | °C/W |

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESDS1.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charge device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

### ESD Ratings for AD7383-4 and AD7384-4

*Table 8. AD7383-4 and AD7384-4, 24-lead LFCSP*

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | ±4000 | 3A |
| FICDM | ±1250 | C3 |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

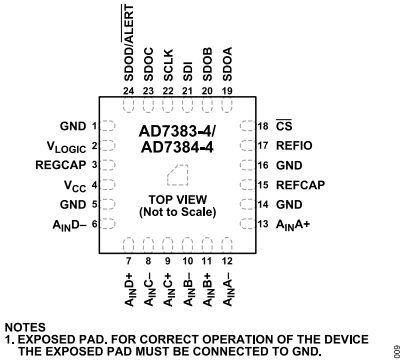


*Figure 9. Pin Configuration*

*Table 9. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 5, 14, 16 | GND | Ground Reference Point. GNDs are the ground reference points for all circuitry on the device. |
| 2 | $V_{LOGIC}$ | Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple $V_{LOGIC}$ to GND with a 1 µF capacitor. |
| 3 | REGCAP | Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple REGCAP to GND with a 1 µF capacitor. The voltage at REGCAP is 1.9 V typical. |
| 4 | $V_{CC}$ | Power Supply Input Voltage, 3.0 V to 3.6 V. Decouple $V_{CC}$ to GND using a 1µF capacitor. |
| 6, 7 | $A_{IN}D-$, $A_{IN}D+$ | Analog Inputs of ADC D. The $A_{IN}D-$ and $A_{IN}D+$ analog inputs form a pseudo differential pair. $A_{IN}D-$ is typically connected to $V_{REF}/2$, and the $A_{IN}D+$ voltage range is from 0 V to $V_{REF}$. |
| 8, 9 | $A_{IN}C-$, $A_{IN}C+$ | Analog Inputs of ADC C. The $A_{IN}C-$ and $A_{IN}C+$ analog inputs form a pseudo differential pair. $A_{IN}C-$ is typically connected to $V_{REF}/2$, and the $A_{IN}C+$ voltage range is from 0 V to $V_{REF}$. |
| 10, 11 | $A_{IN}B$-, $A_{IN}B+$ | Analog Inputs of ADC B. The $A_{IN}B-$ and $A_{IN}B+$ analog inputs form a pseudo differential pair. $A_{IN}B-$ is typically connected to $V_{REF}/2$, and the $A_{IN}B+$ voltage range is from 0 V to $V_{REF}$. |
| 12, 13 | $A_{IN}A-$, $A_{IN}A+$ | Analog Inputs of ADC A. The $A_{IN}A-$ and $A_{IN}A+$ analog inputs form a pseudo differential pair. $A_{IN}A-$ is typically connected to $V_{REF}/2$, and the $A_{IN}A+$ voltage range is from 0 V to $V_{REF}$. |
| 15 | REFCAP | Decoupling Capacitor Pin for Band Gap Reference. Decouple REFCAP to GND with a 0.1 µF capacitor. The voltage at REFCAP is 2.5 V typical. |
| 17 | REFIO | Reference Input and Output. The on-chip reference of 2.5 V is available as an output on REFIO for external use if the device is configured accordingly. Alternatively, an external reference of 2.5 V to 3.3 V can be input to REFIO. Set the REFSEL bit in the CONFIGURATION1 register to 1 when using the external reference and apply the REFSEL bit after $V_{CC}$ and $V_{LOGIC}$. Decoupling is required on REFIO for both the internal and external reference options. Apply a 1 µF capacitor from REFIO to GND. |
| 18 | $\overline{CS}$ | Chip Select Input. Active low, logic input $\overline{CS}$ provides the dual function of initiating conversions on the AD7383-4 and the AD7384-4 and framing the serial data transfer. |
| 19 | SDOA | Serial Data Output A. SDOA functions as a serial data output pin to access the conversion results and register contents. |
| 20 | SDOB | Serial Data Output B. SDOB functions as a serial data output pin to access the conversion results. |
| 21 | SDI | Serial Data Input. SDI provides the data written to the on-chip control registers. |
| 22 | SCLK | Serial Clock Input. SCLK is for data transfers to and from the ADC. |
| 23 | SDOC | Serial Data Output C. SDOC functions as a serial data output pin to access the conversion results and register contents. |
| 24 | SDOD/$\overline{ALERT}$ | Serial Data Output D/Alert Indication Output. SDOD/$\overline{ALERT}$ can operate as a serial data output pin or alert indication output.<br>SDOD functions as a serial data output pin to access the conversion results.<br>$\overline{ALERT}$ operates as an alert pin going low to indicate that a conversion result has exceeded a configured threshold. |
| Not applicable | EPAD | Exposed Pad. For correct operation of the device, the exposed pad must be connected to GND. |

## TYPICAL PERFORMANCE CHARACTERISTICS

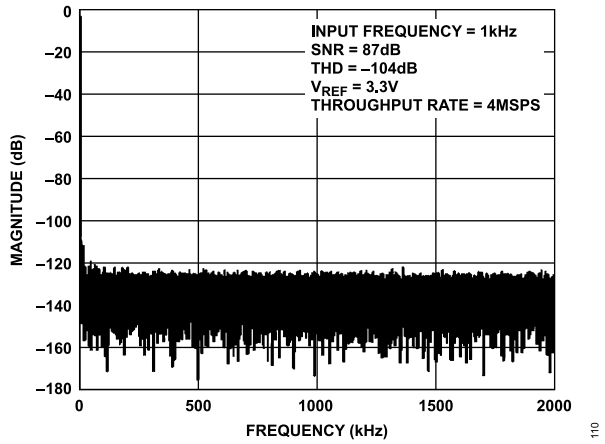


Figure 10. Fast Fourier Transform (FFT), External Reference Voltage = 3.3 V

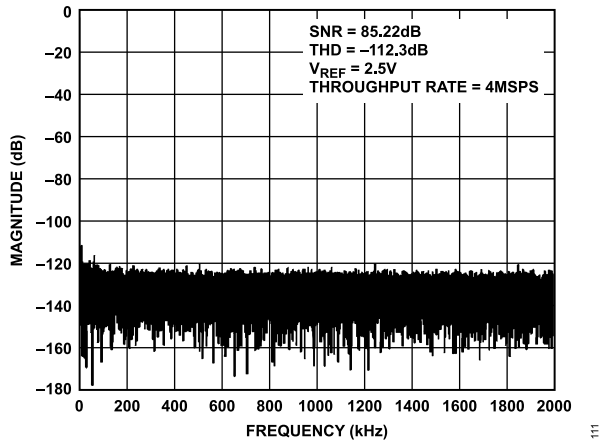


Figure 11. FFT, Internal Reference Voltage = 2.5 V

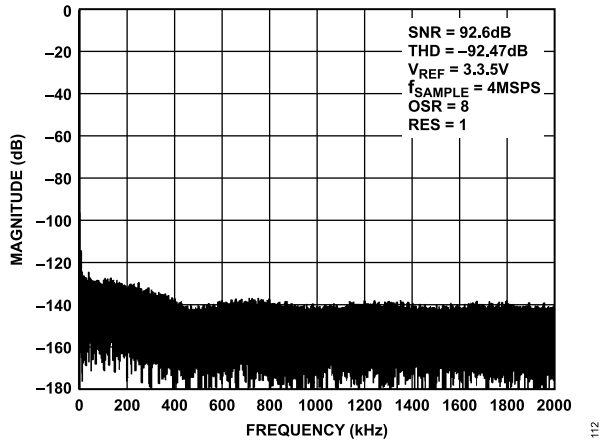


Figure 12. FFT, 4 MSPS Throughput Rate with Oversampling

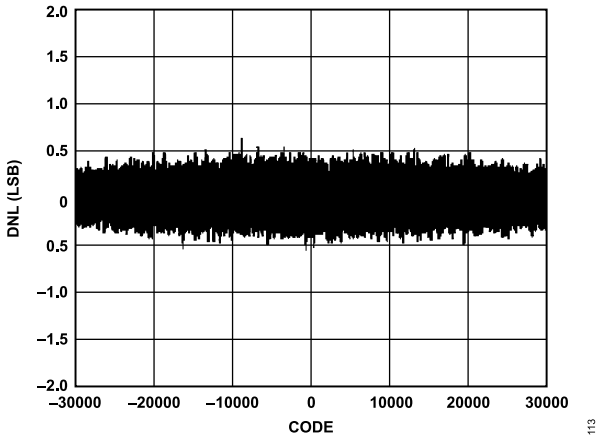


Figure 13. DNL

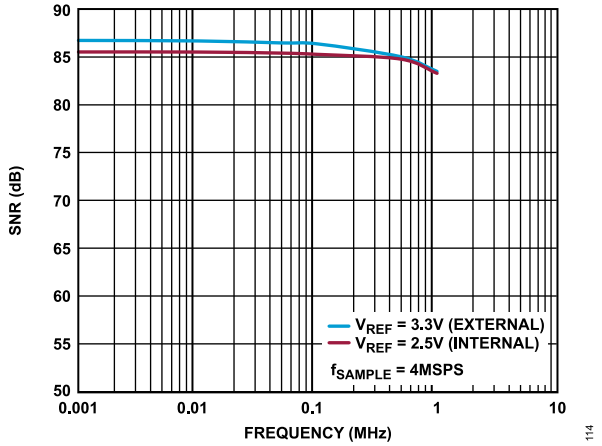


Figure 14. AD7383-4 SNR vs. Input Frequency

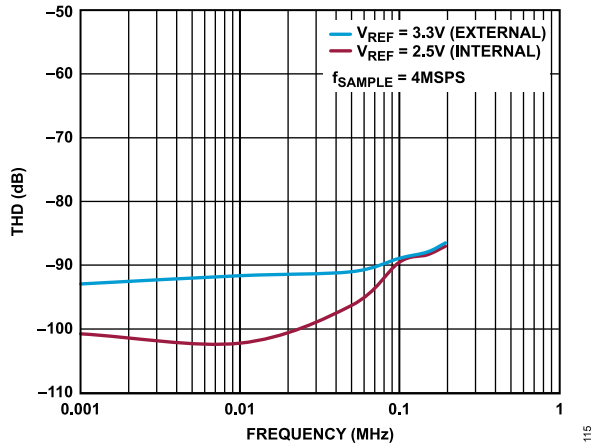


Figure 15. AD7383-4 THD vs. Input Frequency

## TYPICAL PERFORMANCE CHARACTERISTICS

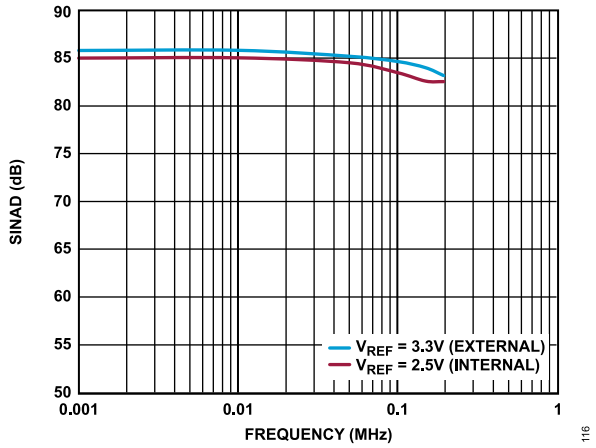


*Figure 16. SINAD vs. Input Frequency*

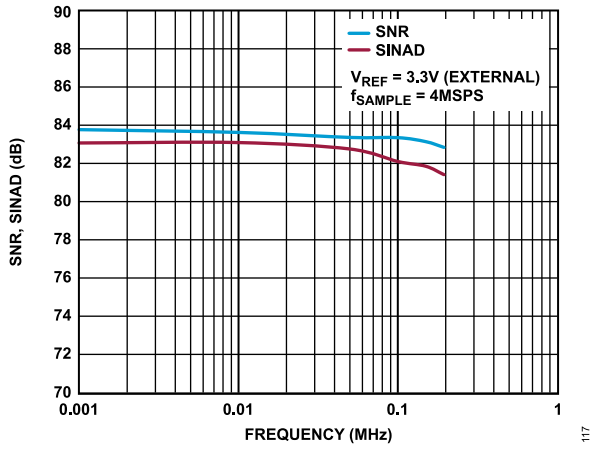


*Figure 17. AD7384-4 SINAD, SNR vs. Input Frequency*

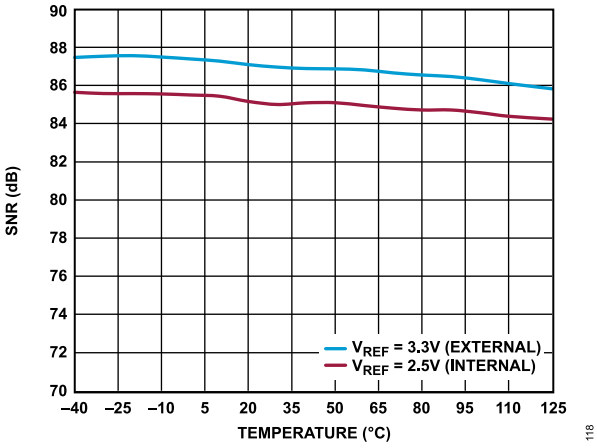


*Figure 18. SNR vs. Temperature*

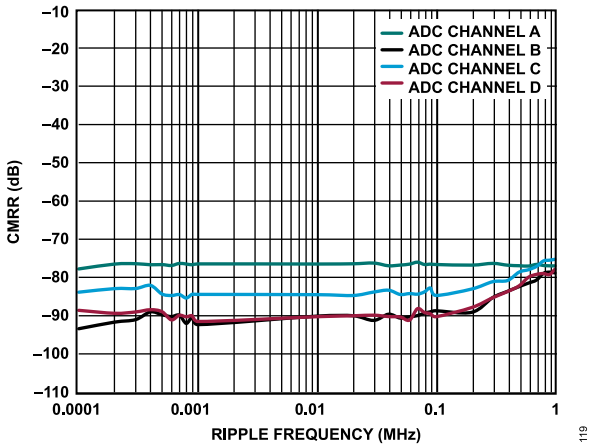


*Figure 19. CMRR vs. Ripple Frequency*

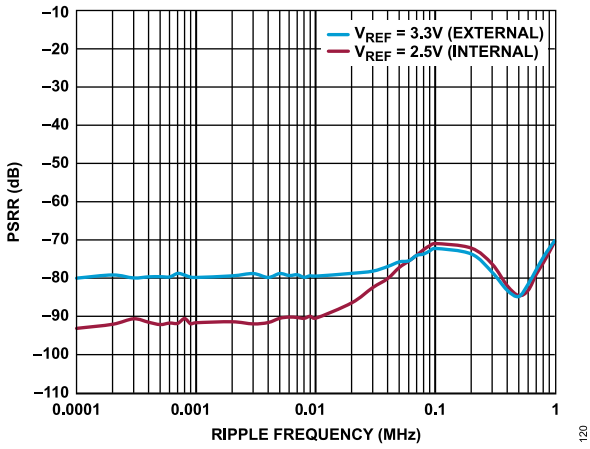


*Figure 20. PSRR vs. Ripple Frequency*

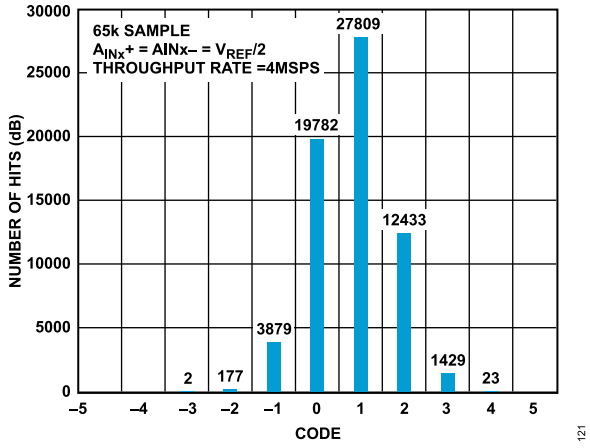


*Figure 21. Histogram*

## TYPICAL PERFORMANCE CHARACTERISTICS

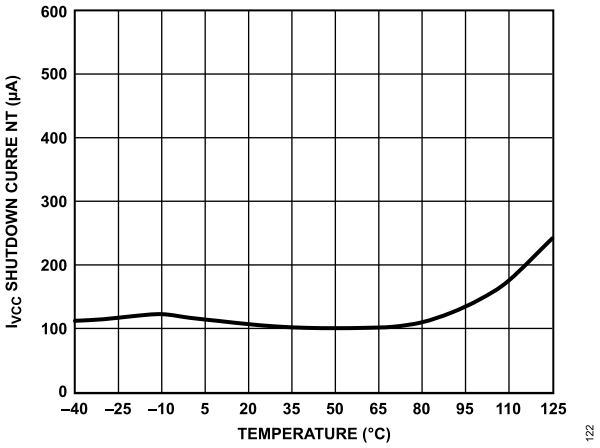


*Figure 22. Rolling Average Oversampling*

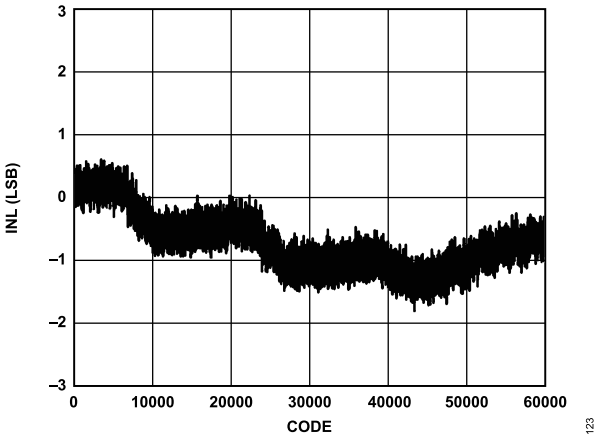


*Figure 23. INL*

## TERMINOLOGY

### Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

### Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

### Gain Error

The first transition (from 100 … 000 to 100 …001) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

### Gain Error Drift

The gain error change due to a temperature change of 1°C.

### Gain Error Matching

Gain error matching is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

### Zero Error

Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

### Zero Error Temperature Drift

Zero error temperature drift is the zero error change due to a temperature change of 1°C.

### Zero Error Match

Zero error match is the difference in zero error between the input channels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the RMS amplitude of the input signal and the peak spurious signal.

### Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonic components to the RMS value of a full-scale input signal and is expressed in decibels.

### Signal-to-Noise and Distortion (SINAD) Ratio

SINAD is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

### Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of $A_{INx}+$ and $A_{INx}-$ of f. CMRR is expressed in decibels.

$$CMRR = 10log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:

$P_{ADC\_IN}$ is the common-mode power at the f applied to the $A_{INx}+$ and $A_{INx}-$ inputs.

$P_{ADC\_OUT}$ is the power at the f in the ADC output.

### Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

### Aperture Jitter

Aperture jitter is the variation in aperture delay.

## THEORY OF OPERATION

### CIRCUIT INFORMATION

The AD7383-4/AD7384-4 are high speed, quad, pseudo differential, 16-bit and 14-bit (respectively), SAR ADCs. The devices operate from a 3.0 V to 3.6 V power supply and feature throughput rates up to 4 MSPS.

The AD7383-4/AD7384-4 contain four successive approximation ADCs and serial peripheral interfaces (SPIs) with four separate data output pins. The devices are housed in a 24-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the devices via the SPI. The SPI can operate with two, four, or one serial output(s). The AD7383-4/AD7384-4 have an on-chip 2.5 V internal reference ($V_{REF}$). If an external reference voltage is required, and the values range from 2.5 V to 3.3 V, set the REFSEL bit in the CONFIGURATION1 register to 1. If the internal reference is used elsewhere in the system, buffer the reference output. The pseudo differential analog input range for the AD7383-4/AD7384-4 is the common-mode voltage ($V_{CM}$) ± $V_{REF}$/2.

The AD7383-4/AD7384-4 feature on-chip oversampling blocks to improve performance. Normal averaging and rolling average oversampling modes are available. Power-down options to allow power saving between conversions are available. Configuration of the devices is implemented via the standard SPI, as described in the Interface section.

### CONVERTER OPERATION

The AD7383-4/AD7384-4 have four successive approximation ADCs, each based around two capacitive DACs. Figure 24 and Figure 25 show simplified schematics of one of these ADCs in acquisition phase and conversion phase, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 24 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor ($C_S$) arrays can acquire the differential signal on the input.

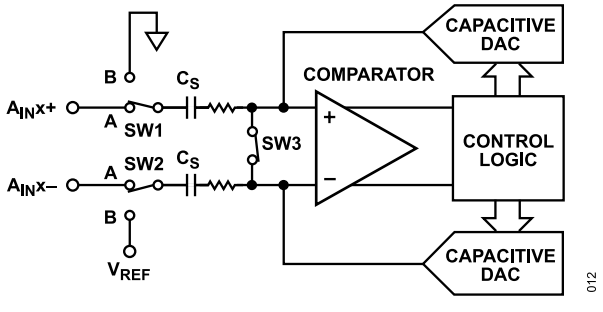


*Figure 24. ADC Acquisition Phase*

When the ADC starts a conversion (see Figure 25), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Match the output impedance of the sources driving the $A_{IN}x+$ and $A_{IN}x-$ pins. Otherwise, the two inputs have different settling times, resulting in errors.

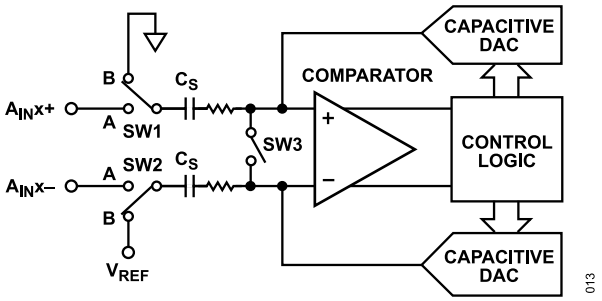


*Figure 25. ADC Conversion Phase*

### ANALOG INPUT STRUCTURE

Figure 26 shows the equivalent circuit of the analog input structure of the AD7383-4/AD7384-4. The four diodes provide ESD protection for the analog inputs. Ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the devices.

The C1 capacitors in Figure 26 are typically 3 pF and are primarily attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically 200 Ω. The C2 capacitors are the ADC sampling capacitors with a typical capacitance of 15 pF.

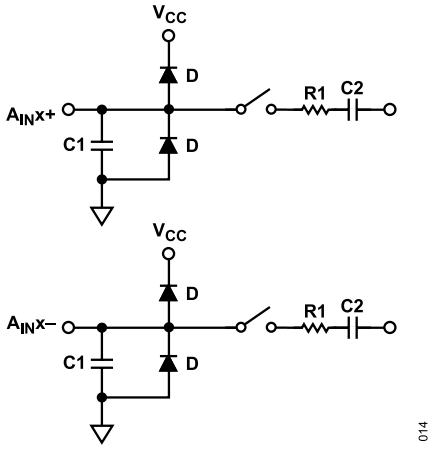


*Figure 26. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed*

## THEORY OF OPERATION

### ADC TRANSFER FUNCTION

The AD7383-4/AD7384-4 use a 2.5 V to 3.3 V reference voltage. The AD7383-4/AD7384-4 convert the differential voltage of the analog inputs ($A_{IN}A+$ and $A_{IN}A-$, $A_{IN}B+$ and $A_{IN}B-$, $A_{IN}C+$ and $A_{IN}C-$, and $A_{IN}D+$ and $A_{IN}D-$) into a digital output.

The conversion result is MSB first, twos complement. The LSB size is $V_{REF}/2^N$, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen and if resolution boost mode is enabled. Table 10 outlines the LSB size expressed in microvolts for different resolutions and reference voltage options.

The ideal transfer characteristic of the AD7383-4/AD7384-4 is shown in Figure 27.

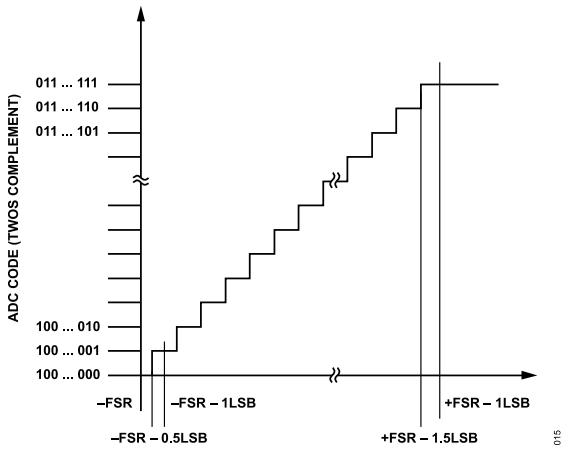


*Figure 27. ADC Ideal Transfer Function (FSR = Full-Scale Range)*

*Table 10. LSB Size*

| Resolution (Bits) | 2.5 V Reference (µV) | 3.3 V Reference (µV) |
|---|---|---|
| 14 | 152.6 | 201.4 |
| 16 | 38.1 | 50.3 |
| 18 | 9.53 | 12.6 |

## APPLICATIONS INFORMATION

Figure 28 shows an example of a typical application circuit for the AD7383-4/AD7384-4. Decouple the $V_{CC}$, $V_{LOGIC}$, REGCAP, and REFIO pins with suitable decoupling capacitors as shown in Figure 28. The exposed pad is a ground reference point for circuitry on the devices and must be connected to the board ground.

For optimal performance, a differential RC filter must be placed on the analog inputs. In a typical application, R = 33 Ω, C1 = 68 pF, and C2 = 68 pF are recommended. These RC combinations must be the same for all channels of the AD7383-4/AD7384-4.

The four pseudo differential channels of the AD7383-4/AD7384-4 accept an input voltage range from 0 V to $V_{REF}$ on $A_{IN}A+$ , $A_{IN}B+$, $A_{IN}C+$, and $A_{IN}D+$ and accept $V_{REF}/2$ voltage on $A_{IN}A-$, $A_{IN}B-$, $A_{IN}C-$ and $A_{IN}D-$. See Table 11 for the recommended driver amplifiers that can best fit and add value to the application.

The performance of the AD7383-4/AD7384-4 is impacted by noise on the digital interface. This impact is dependent on board layout and design. Keep a minimal distance of the digital line to the digital interface, or place a 100 Ω resistor in series and close to the SDOA, SDOB, SDOC, and SDOD/$\overline{\text{ALERT}}$ pins to reduce noise from the digital interface coupling of the AD7383-4/AD7384-4.

The AD7383-4/AD7384-4 have a buffered internal 2.5 V reference that is accessed via the REFIO pin. The buffered internal 2.5 V reference must use an external buffer, like the ADA4807-2, before connecting the reference to the external circuitry. The AD7383-4/AD7384-4 have an option to use an ultralow noise, high accuracy voltage reference like the ADR4533 or the ADR4525 as a 3.3 V and 2.5 V external voltage reference source to drive the AD7383-4/AD7384-4 REFIO pin. A 1 µF reservoir capacitor is recommended to be connected as close as possible between the REFIO pin and the ground in a short and wide trace. When using this external reference voltage in another circuit within the application, for example, as a common-mode voltage for the driver amplifier, it is recommended to use a buffer amplifier like the ADA4807-2 for a stable reference.

### POWER SUPPLY

For a typical application, the AD7383-4/AD7384-4 circuitry, shown in Figure 28, is driven from a 5 V (V+) supply to power the system.

***Table 11. Signal Chain Components***

| Companion Devices | Model | Description | Typical Application |
|---|---|---|---|
| ADC Driver | ADA4896-2 | 1 nV/√Hz, rail-to-rail output amplifier | Precision, low noise, high frequency |
| | ADA4940-2 | Ultra low power, full differential, low distortion amplifier | Precision, low density, low power |
| | ADA4807-2 | 1 mA, rail-to-rail output amplifier | Precision, low power, high frequency |
| External Reference | ADR4525 | Ultralow noise, high accuracy voltage reference | 2.5 V reference voltage |
| | ADR4533 | Ultralow noise, high accuracy voltage reference | 3.3 V reference voltage |
| Reference Buffer | ADA4807-2 | 1 mA, rail-to-rail output amplifier | Precision, low power, high frequency |
| LDO Regulator | ADP166 | Very low quiescent, 150 mA LDO regulator | 3.0 V to 3.6 V supply for $V_{CC}$ and $V_{LOGIC}$ |
| | ADP7104 | 500 mA low noise, CMOS LDO regulator | 5 V supply |
| | ADP7182 | Low noise line regulator | −2.5 V supply for ADC driver amplifier |
| | ADP5600 | Interleaved inverting charge pump with negative LDO | Voltage inverter for negative supply |

The 5 V (V+) is supplied from the ADP7104. The ADC driver is supplied by a +5 V (V+) and a −2.5 V (V−) that is derived from the inverting charge pump, the ADP5600, which converts +5 V to −5 V, and then to the ADP7182 for the low noise voltage regulator to output −2.5 V. Two independent power supply sources are derived from a low dropout (LDO) regulator to power the $V_{CC}$ supply for the analog circuitry and the $V_{LOGIC}$ supply for the digital interface of the AD7383-4/AD7384-4. A very low quiescent current LDO regulator like the ADP166 is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical $V_{CC}$ and $V_{LOGIC}$ levels. The $V_{CC}$ supply and the $V_{LOGIC}$ supply must be decoupled separately with a 1 µF capacitor, placed close to the device pin using short and wide traces to provide a low impedance path that reduces glitches in the power supply lines. Additionally, there is an internal LDO regulator that supplies the AD7383-4/AD7384-4. The on-chip regulator provides a 1.9 V supply only for internal use on the device. Decouple the AD7383-4/AD7384-4 REGCAP pin with a 1 µF capacitor to the GND pin with short and wide traces, and place the capacitor as close as possible to the RECGAP pin of the device.

### Power-Up

The AD7383-4/AD7384-4 are not easily damaged by power supply sequencing. $V_{CC}$ and $V_{LOGIC}$ can be applied in any sequence. The external reference must be applied after $V_{CC}$ and $V_{LOGIC}$ are applied. Analog and digital signals must be applied after the external reference is applied.

The AD7383-4/AD7384-4 require $t_{POWERUP}$ from applying $V_{CC}$ and $V_{LOGIC}$ until the ADC conversion results are stable. Figure 4 shows the recommended signal condition during power-up with the $\overline{\text{CS}}$ pin held high. Issue a software reset after power-up (see the Software Reset section for details).

## APPLICATIONS INFORMATION

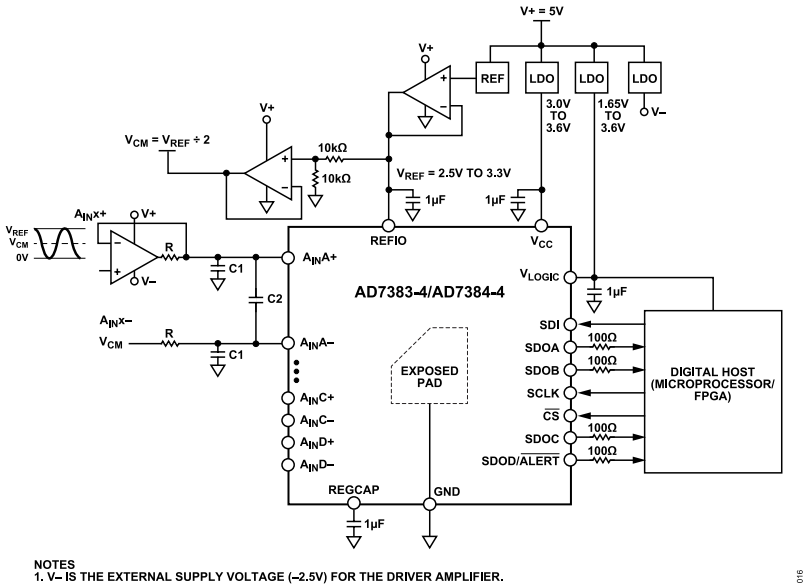


*Figure 28. Typical Applications Circuit*

## MODES OF OPERATION

The AD7383-4/AD7384-4 have several on-chip configuration registers for controlling the operational mode of the device.

### OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC noise) of the ADC. The AD7383-4/AD7384-4 offer an oversampling function on-chip with two user configurable oversampling modes: normal averaging and rolling average.

The oversampling functionality is configured by programming the OS_MODE bit and OSR bits in the CONFIGURATION1 register.

### Normal Averaging Oversampling

Normal averaging oversampling mode is used in applications where slower output data rates are allowed and where a higher SNR or dynamic range is desirable. Normal averaging involves taking a number of samples, adding them together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is cleared when the process completes.

Normal averaging oversampling mode is configured by setting the OS_MODE bit to Logic 0 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the OSR bits (see Table 12).

Table 12 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution. If required, additional resolution can be achieved by configuring the resolution boost bit (RES) in the CONFIGURATION1 register. See the Resolution Boost section for further details.

The number of samples (n), defined by the OSR bits, are taken, added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of $\overline{CS}$, and the AD7383-4/AD7384-4 control all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n samples at the device maximum sampling rate is 3 MSPS. The data is ready for readback on the next serial interface access. After the averaging technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and is initiated by the next falling edge of $\overline{CS}$.

As the output data rate is reduced by the oversampling ratio, the SPI frequency required to transmit the data is reduced accordingly.

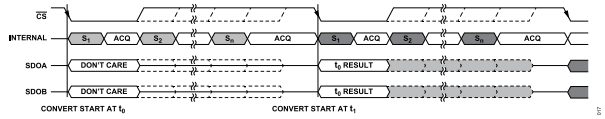


*Figure 29. Normal Averaging Oversampling Operation*

*Table 12. Normal Averaging Oversampling Mode*

| | | AD7383-4 SNR (dB Typical) | | | | |
|---|---|---|---|---|---|---|
| | | 2.5 V Reference | | 3.3 V Reference | | |
| OSR, Bits[2:0] | Oversampling Ratio | RES = 0 | RES = 1 | RES = 0 | RES = 1 | Data Output Rate (kSPS Maximum) |
| 000 | No OS | 85.03 | 85.22 | 87.00 | 87.04 | 4000 |
| 001 | 2 | 87.95 | 88.29 | 89.50 | 90.01 | 1500 |
| 010 | 4 | 90.45 | 91.22 | 91.76 | 92.83 | 750 |
| 011 | 8 | 92.67 | 94.00 | 93.71 | 95.50 | 375 |
| 100 | 16 | 94.42 | 94.67 | 95.12 | 97.50 | 187.5 |
| 101 | 32 | 95.27 | 96.74 | 95.68 | 98.32 | 93.75 |
| 110 | Invalid | Not applicable | Not applicable | Not applicable | Not applicable | Not applicable |
| 111 | Invalid | Not applicable | Not applicable | Not applicable | Not applicable | Not applicable |

## MODES OF OPERATION

### Rolling Average Oversampling

Rolling average oversampling mode is used in applications where higher output data rates are required and where a higher SNR or dynamic range is desirable. Rolling averaging involves taking a number of samples, adding them together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared when the process completes. The rolling oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

Rolling average oversampling mode is configured by setting the OS_MODE bit to Logic 1 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the OSR bits (see Table 13).

Table 13 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the AD7383-4 and 14-bit for the AD7384-4. Additional resolution can be achieved by configuring the RES bit in the CONFIGURATION1 register. See the Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. When a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8, regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on reset on the first conversion after a software controlled hard or soft reset. A new conversion result is shifted into the FIFO on completion of every ADC conversion regardless of the status of the OSR bits and the OS_MODE bit. This conversion allows a seamless transition from no oversampling to rolling average oversampling, or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples, n, defined by the OSR bits are taken from the FIFO, added together and the result is divided by n.

***Table 13. Rolling Average Oversampling Overview***

| | | AD7383-4 SNR (dB Typical) | | | | |
|---|---|---|---|---|---|---|
| | | 2.5 V Reference | | 3.3 V Reference | | |
| OSR, Bits[2:0] | Oversampling Ratio | RES = 0 | RES = 1 | RES = 0 | RES = 1 | Data Output Rate (kSPS Maximum) |
| 000 | No oversampling | 85.14 | 85.21 | 87.02 | 87.03 | 4000 |
| 001 | 2 | 87.05 | 87.42 | 88.55 | 89.02 | 4000 |
| 010 | 4 | 89.76 | 90.27 | 91.00 | 91.85 | 4000 |
| 011 | 8 | 92.22 | 93.25 | 93.23 | 94.78 | 4000 |
| 110 | Invalid | Not applicable | Not applicable | Not applicable | Not applicable | Not applicable |
| 111 | Invalid | Not applicable | Not applicable | Not applicable | Not applicable | Not applicable |

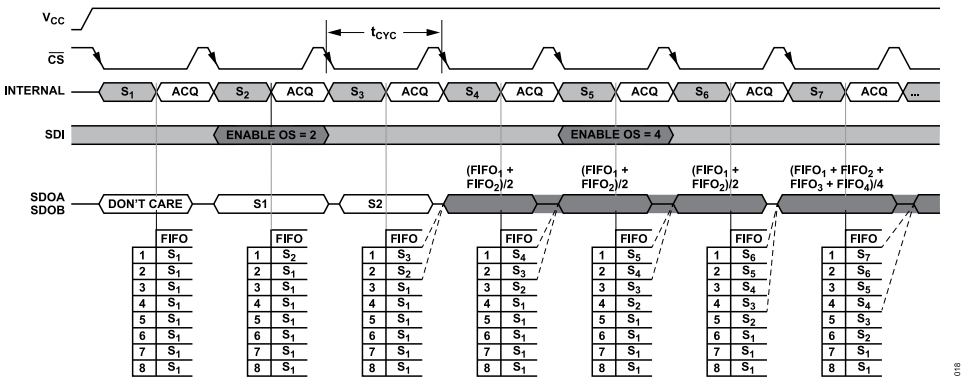


***Figure 30. Rolling Average Oversampling Mode Configuration***

## MODES OF OPERATION

### RESOLUTION BOOST

The default resolution and output data size are 16 bits for the AD7383-4 and 14 bits for the AD7384-4. When the on-chip oversampling function is enabled, the performance of the ADC can exceed the default resolution. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the CONFIGURATION1 register is set to Logic 1 and the AD7383-4/AD7384-4 are in a valid oversampling mode, the conversion result size for the AD7383-4 is 18 bits and the AD7384-4 is 16 bits. In this mode, 18 SCLK cycles are required to propagate the data for the AD7383-4 and 16 SCLK cycles are required for the AD7384-4.

### ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the value in the conversion result register exceeds the alert high limit value in the ALERT_HIGH_THRESHOLD register or falls below the alert low limit value in the ALERT_LOW_THRESHOLD register. The ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the $\overline{\text{ALERT}}$ indication register.

The register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs create a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOD/$\overline{\text{ALERT}}$ pin. The SDOD/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the bits in CONFIGURATION1 and CONFIGURATION2 as follows:

1. Set the SDO bit to any value other than 0b10.
2. Set the ALERT_EN bit to 1.
3. Set a valid value in the ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register.

The alert indication function is available in oversampling (rolling average, normal averaging, and in non-oversampling modes).

The alert function of the SDOD/$\overline{\text{ALERT}}$ pin updates at the end of conversion. The alert indication status bits in the $\overline{\text{ALERT}}$ register are updated as well and must be read before the end of the next conversion.

Bits[7:0] in the alert indication register are cleared by reading the alert indication register contents. The alert function of the SDOD/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the alert indication register.

See Figure 8 for the $\overline{\text{ALERT}}$ timing diagram.

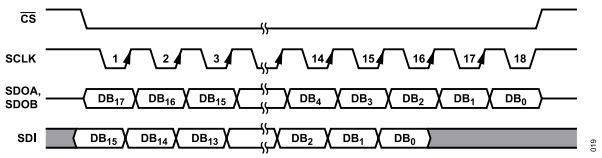


*Figure 31. Resolution Boost*

### POWER MODES

The AD7383-4/AD7384-4 have two power modes that can be set in the CONFIGURATION1 register, normal mode and shutdown mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the CONFIGURATION1 register to configure the power modes in the AD7383-4/AD7384-4. Set PMODE to Logic 0 for normal mode and Logic 1 for shutdown mode.

#### Normal Mode

Keep the AD7383-4/AD7384-4 in normal mode to achieve the fastest throughput rate. All blocks within the AD7383-4/AD7384-4 remain fully powered, and an ADC conversion can be initiated by a falling edge of $\overline{\text{CS}}$ when required. When the AD7383-4/AD7384-4 are not converting, the devices are in static mode and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption of the AD7383-4/AD7384-4 scales with throughput.

#### Shutdown Mode

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD7383-4/AD7384-4 are in shutdown mode, all analog circuitry powers down. The SPI remains active during shutdown mode to allow the AD7383-4/AD7384-4 to exit shutdown mode.

To enter shutdown mode, write to the PMODE bit in the CONFIGURATION1 register. The AD7383-4/AD7384-4 shuts down and current consumption reduces.

To exit shutdown mode and return to normal mode, set the PMODE bit in the CONFIGURATION1 register to Logic 0. All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode, allow sufficient time for the circuitry to turn on before starting a conversion.

### INTERNAL AND EXTERNAL REFERENCE

The AD7383-4/AD7384-4 have a buffered 2.5 V internal reference primarily used for internal device operation and access via the REFIO pin. When using the buffered internal 2.5 V reference externally, the reference must use an external buffer before connecting

## MODES OF OPERATION

to the external circuitry. Alternatively, if a more accurate reference or higher dynamic range is required, an external reference can be supplied. An externally supplied reference can range from 2.5 V to 3.3 V.

Reference selection, internal or external, is configured by the REFSEL bit in the CONFIGURATION1 register. If the REFSEL bit is set to 0, the internal reference buffer is enabled. If the REFSEL bit is set to 1, the internal reference buffer is disabled. If an external reference is preferred, set the REFSEL bit to 1 and supply an external reference to the REFIO pin.

The external reference voltage of the AD7383-4/AD7384-4 is driven through the REFIO pin. The external reference voltage must have enough current to drive the AD7383-4/AD7384-4, which is a maximum of 2.4 mA. Connecting a 1 µF capacitor to the REFIO pin is recommended. The recommended external voltage references are the ADR4525 for 2.5 V and the ADR4533 for 3.3 V.

### SOFTWARE RESET

The AD7383-4/AD7384-4 have two reset modes, a soft reset and a hard reset. A $\overline{\text{RESET}}$ is initiated by writing to the reset bits in the CONFIGURATION2 register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The $\overline{\text{ALERT}}$ indication register is cleared. The reference and LDO regulator remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, and resets the internal oscillator block.

### DIAGNOSTIC SELF TEST

The AD7383-4/AD7384-4 run a diagnostic self test after a power-on reset or after a software hard reset to ensure that the correct configuration is loaded into the device.

The result of the self test is displayed in the SETUP_F bit in the $\overline{\text{ALERT}}$ indication register. If the SETUP_F bit is set to Logic 1, the diagnostic self test has failed. If the test fails, perform a software hard reset to reset the AD7383-4/AD7384-4 registers to the default status.

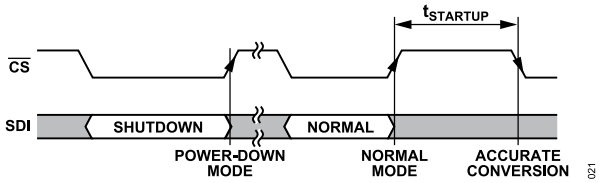


*Figure 32. Shutdown Mode Operation*

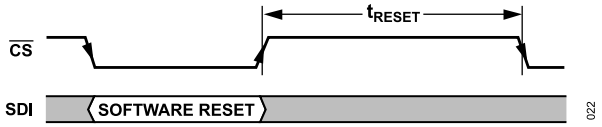


*Figure 33. Software Reset Operation*

## INTERFACE

The interface to the AD7383-4/AD7384-4 is via a SPI. The interface consists of the $\overline{CS}$, SCLK, SDOA, SDOB, SDOC, SDOD, and SDI pins. When referencing a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed, such as SDOD. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

The $\overline{CS}$ signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled, and the bus is taken out of three-state. The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, SDOC, SDOD, and SDI signals. A minimum of 16 SCLK cycles are required for a write to or read from a register. The minimum number of SCLKs for a conversion read is dependent on the resolution of the device and the configuration settings (see Table 14).

The AD7383-4/AD7384-4 have four serial output signals, SDOA, SDOB, SDOC, and SDOD. Programming the SDO bit in the CONFIGURATION2 register configures 4-wire, 2-wire, or 1-wire mode. To achieve the highest throughput of the devices, use either the 2-wire or 4-wire mode to read the conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results.

Configuring a cyclic redundancy check (CRC) operation for SPI reads, SPI writes, and oversampling mode with resolution boost mode enabled alters the operation of the interface. Refer to the CRC section to ensure correct operation.

### READING CONVERSION RESULTS

The $\overline{CS}$ signal initiates the conversion process. A high to low transition on the $\overline{CS}$ signal initiates a simultaneous conversion of the four ADCs, ADC A, ADC B, ADC C, and ADC D. The AD7383-4/AD7384-4 have a one cycle readback latency. Therefore, the conversion results are available on the next SPI access. Take the $\overline{CS}$ signal low, and the conversion result clocks out on the serial data output pins. The next conversion is also initiated at this point.

The conversion result is shifted out of the device as a 16-bit result for the AD7383-4 and 14-bit result for the AD7384-4. The MSB of the conversion result is shifted out on the $\overline{CS}$ falling edge. The remaining data is shifted out of the device under the control of the SCLK input. The data is shifted out on the rising edge of the SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take $\overline{CS}$ high again to return the SDOx to a high impedance state.

The number of SCLK cycles to propagate the conversion SDOx pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled (see Figure 34 and Table 14 for details). If CRC reading is enabled, additional SCLK pulses are required to propagate the CRC information (see the CRC section for more details).

Because the $\overline{CS}$ signal initiates a conversion as well as framing the data, any data access must be completed within a single frame.

*Table 14. Number of SCLK Cycles (n) Required for Reading Conversion Results*

| Interface Configuration | Resolution Boost Mode | CRC Read | No. of SCLK Cycles |
|---|---|---|---|
| 4-Wire | Disabled | Disabled | 16 |
| | | Enabled | 24 |
| | Enabled | Disabled | 18 |
| | | Enabled | 26 |
| 2-Wire | Disabled | Disabled | 32 |
| | | Enabled | 40 |
| | Enabled | Disabled | 36 |
| | | Enabled | 44 |
| 1-Wire | Disabled | Disabled | 64 |
| | | Enabled | 72 |
| | Enabled | Disabled | 72 |
| | | Enabled | 80 |

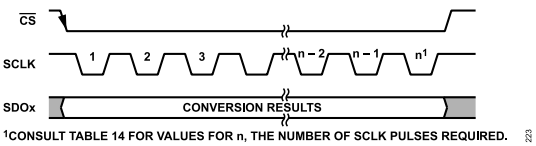


*Figure 34. Reading Conversion Results*

## INTERFACE

### Serial 4-Wire Mode

Configure 4-wire mode by setting the SDO bits in the CONFIGURATION2 register to 0b10. In 4-wire mode, the conversion result for ADC A is output on the SDOA pin, ADC B on the SDOB pin, ADC C on the SDOC pin, and ADC D on the SDOD/$\overline{\text{ALERT}}$ pin.

### Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bits in the CONFIGURATION2 register to 0b00. In 2-wire mode, the conversion results for ADC A and ADC C are output on the SDOA pin. The conversion results for ADC B and ADC D are output on the SDOB pin.

### Serial 1-Wire Mode

In applications where slower throughput rates are allowed or normal averaging oversampling is used, the serial interface can be configured to operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A, ADC B, ADC C, and ADC D are output on the SDOA pin. Additional SCLK cycles are required to propagate all data. ADC A data is output first, followed by the ADC B, ADC C, and ADC D conversion results.

## LOW LATENCY READBACK

The interface on the AD7383-4/AD7384-4 has a one-cycle latency as shown in Figure 36. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. When the conversion time elapses, a second $\overline{\text{CS}}$ pulse after the initial $\overline{\text{CS}}$ pulse that initiates the conversion can read back the conversion result. This operation is shown in Figure 38.

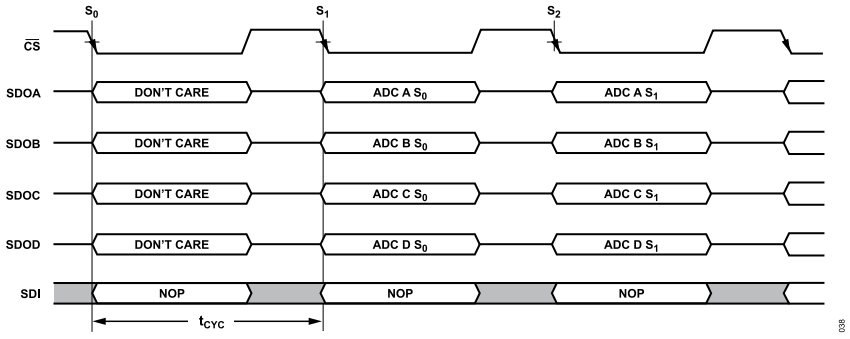


*Figure 35. Read Conversion Results, 4-Wire Mode*

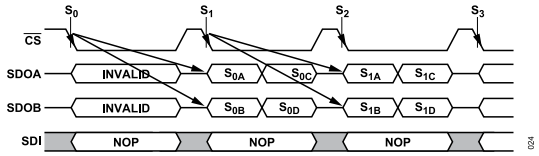


*Figure 36. Read Conversion Results, 2-Wire Mode*

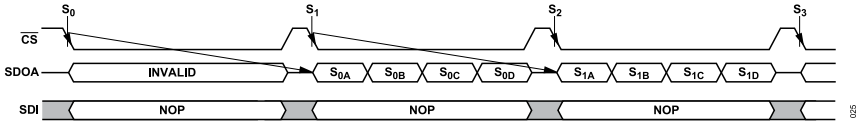


*Figure 37. Reading Conversion Results, 1-Wire Mode*

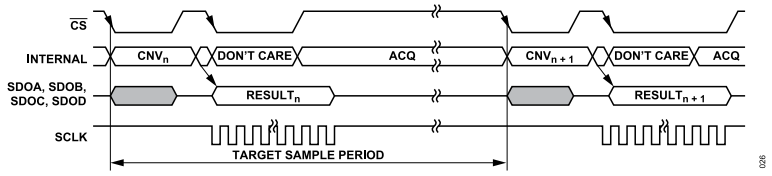


*Figure 38. Low Throughput Low Latency*

## INTERFACE

### READING FROM DEVICE REGISTERS

All of the registers in the device can be read over the SPI. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or a no operation (NOP) command. The format for a read command is shown in Table 17. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], are ignored.

### WRITING TO DEVICE REGISTERS

All of the read/write registers in the AD7383-4/AD7384-4 can be written to over the SPI. The length of a SPI write access is determined by the CRC write function. An SPI access is 16 bits, if CRC write is disabled, and 24 bits when CRC write is enabled. The format for a write command is shown in Table 17. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], contain the data to be written to the selected register.

### CRC

The AD7383-4/AD7384-4 have CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for the SPI reads and writes. For example, enable the CRC function for SPI writes to prevent unexpected changes to the device configuration, but do not enable the CRC function on SPI reads to maintain a higher throughput rate. The CRC feature is controlled by programming of the CRC_W bit and CRC_R bit in the CONFIGURATION1 register.

### CRC Read

If enabled, a CRC consisting of an 8-bit word is appended to the conversion result or register reads. The CRC is calculated on the conversion result for ADC A, ADC B, ADC C, and ADC D, and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, 4-wire SPI mode, and resolution boost mode.

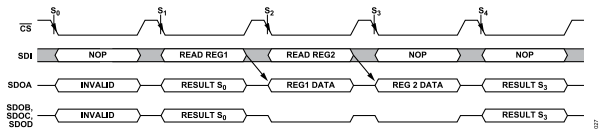


*Figure 39. Register Read*

### CRC Write

To enable the CRC write function, set CRC_W bit in the CONFIGURATION1 register 1. To set the CRC_W bit to 1 to enable the CRC feature, ensure the request frame has a valid CRC command.

After the CRC feature is enabled, all register write requests are ignored unless they are accompanied by a valid CRC command.

A valid CRC is required to both enable and disable the CRC write feature.

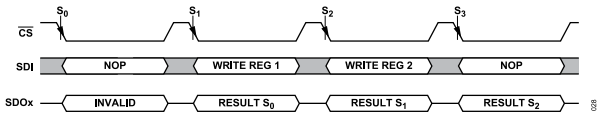


*Figure 40.*

### CRC Polynomial

For CRC checksum calculations, the following polynomial is always used:

$$x^8 + x^2 + x + 1 \quad (1)$$

To generate the checksum, the 16-bit data conversion result of the four channels is combined to produce a 64-bit data stream. The 8 MSBs of the 64-bit data are inverted and the data is appended by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is next to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is next to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum.

For example, the AD7383-4 polynomial is 100000111. Let the original data of four channels be 0xAAAA, 0x5555, 0xAAAA, and 0x5555. The 8 MSBs of the data are inverted. The data is then appended to include eight 0s on right. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

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*Table 15. Example CRC Calculation for 4-Channel, 16-Bit Data*

| Data | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | X[1] | X[1] | X[1] | X[1] | X[1] | X[1] | X[1] | X[1] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Process Data** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1 1 | 0 0 | 1 0 | 0 0 | 0 0 | 0 0 | 1 1 | 1 1 | 0 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 0 0 | 0 0 | 1 1 | 1 1 | 0 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | 1 1 | 1 0 | 0 0 | 0 0 | 1 0 | 0 0 | 1 1 | 0 1 | 1 1 | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 1 0 | 0 0 | 0 0 | 1 1 | 0 1 | 0 1 | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 | 1 0 | 1 1 | 0 1 | 1 1 | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 | 1 1 | 0 1 | 0 1 | 1 1 | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 | 0 0 | 1 1 | 0 1 | 1 1 | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 | 1 0 | 1 1 | 0 1 | 1 1 | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 1 0 | 0 0 | 0 0 | 1 0 | 0 0 | 1 1 | 0 1 | 1 1 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 | 0 0 | 1 1 | 0 1 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 | 1 1 | 1 1 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 | 1 0 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 1 | 0 0 | 0 0 | 0 0 |
| **CRC** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

[1] X means don't care.

## INTERFACE

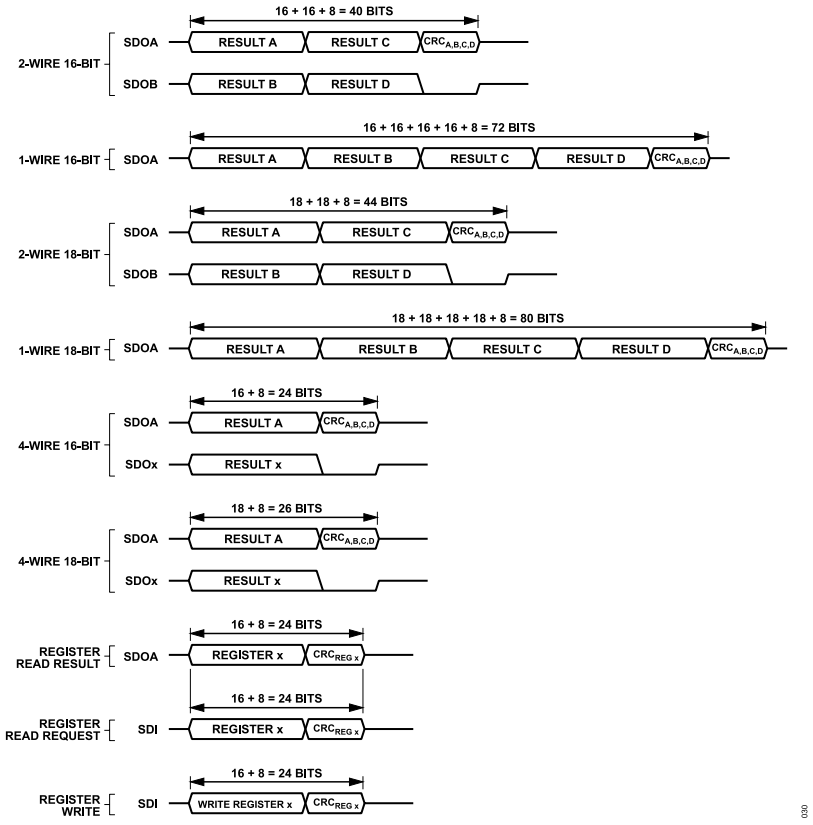



*Figure 41. CRC Operation*

## REGISTERS

The AD7383-4/AD7384-4 have user-programmable on-chip registers for configuring the device. Table 16 shows a complete overview of the registers available on the AD7383-4/AD7384-4.

The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored, and any write request to a read only register is ignored. Writes to the NOP registers and the reserved register are ignored. Any read request to the NOP registers or reserved registers is considered an NOP, and the data transmitted in the next SPI frame are the conversion results.

*Table 16. Register Description*

| Reg | Name | Bits | Bit 15 / Bit 7 | Bit 14 / Bit 6 | Bit 13 / Bit 5 | Bit 12 / Bit 4 | Bit 11 / Bit 3 | Bit 10 / Bit 2 | Bit 9 / Bit 1 | Bit 8 / Bit 0 | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x1 | CONFIGURATION1 | [15:8] | WR | ADDRESSING | | | RESERVED | | OS_MODE | OSR, Bit 2 | 0x0000 | R/W |
| | | [7:0] | OSR, Bits[1:0] | | CRC_W | CRC_R | ALERT_EN | RES | REFSEL | PMODE | | |
| 0x2 | CONFIGURATION2 | [15:8] | WR | ADDRESSING | | | RESERVED | | SDO, Bits[1:0] | | 0x0000 | R/W |
| | | [7:0] | RESET, Bits[7:0] | | | | | | | | | |
| 0x3 | $\overline{\text{ALERT}}$ | [15:8] | WR | ADDRESSING | | | RESERVED | | CRCW_F | SETUP_F | 0x0000 | R |
| | | [7:0] | AI_D_HIGH | AI_D_LOW | AI_C_HIGH | AI_C_LOW | AI_B_HIGH | AI_B_LOW | AI_A_HIGH | AI_A_LOW | | |
| 0x4 | ALERT_LOW_THRESHOLD | [15:8] | WR | ADDRESSING | | | ALERT_LOW, Bits[11:8] | | | | 0x0800 | R |
| | | [7:0] | ALERT_LOW, Bits[7:0] | | | | | | | | | |
| 0x5 | ALERT_HIGH_THRESHOLD | [15:8] | WR | ADDRESSING | | | ALERT_HIGH, Bits[11:8] | | | | 0x07FF | R/W |
| | | [7:0] | ALERT_HIGH, Bits[7:0] | | | | | | | | | |

## ADDRESSING REGISTERS

A serial register transfer on the AD7383-4/AD7384-4 consists of 16 SCLK cycles. The 4 MSBs written to the device are decoded to determine which register is addressed and consist of the register address (REGADDR), Bits[2:0], and the read/write bit (WR). The register address bits determine which on-chip register is selected. If the addressed register is a valid write register, the WR bit determines whether the remaining 12 bits of data on the SDI input are loaded into the addressed register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request, and the addressed register data is available to be read during the next read operation.

*Table 17. Addressing Register Format*

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| WR | REGADDR, Bits[2:0] | | | Data, Bits[11:0] | | | | | | | | | | | |

*Table 18. Bit Descriptions for Addressing Registers*

| Bit | Mnemonic | Description |
|---|---|---|
| D15 | WR | When a 1 is written to this bit, Bits[11:0] of this register are written to the register specified by REGADDR if it is a valid address.<br>Alternatively, when a 0 is written, the next data sent out on the SDOA pin is a read from the designated register if it is a valid address. |
| D14 to D12 | REGADDR | When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 16.<br>When WR = 0 and the REGADDR bits contain a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access.<br>When WR = 0 and the REGADDR bits contain 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back. |
| D11 to D0 | DATA | The DATA bits are written into the corresponding register specified by the REGADDR bits when the WR bit = 1 and the REGADDR bits contain a valid address. |

## CONFIGURATION1 REGISTER

**Address: 0x1, Reset: 0x0000, Name: CONFIGURATION1**

## REGISTERS

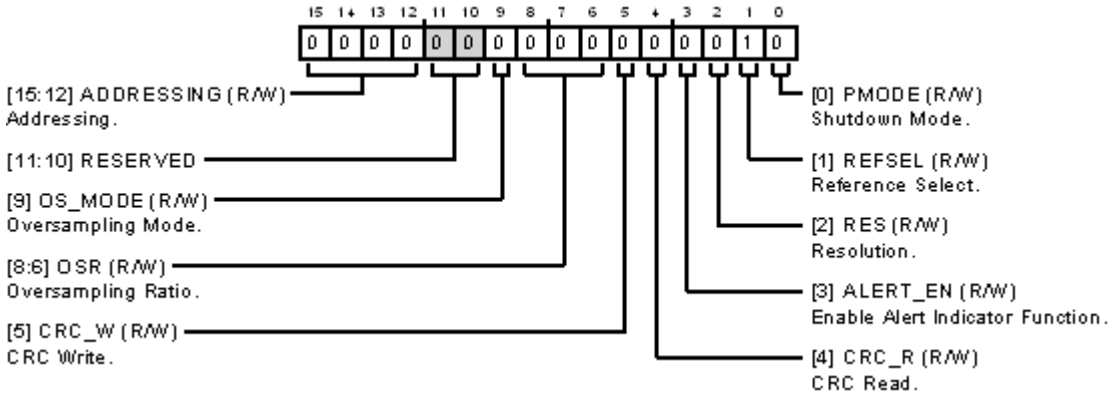



*Table 19. Bit Descriptions for CONFIGURATION1 Register*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:10] | RESERVED | Reserved. | 0x0 | R |
| 9 | OS_MODE | Oversampling Mode. Sets the oversampling mode of the ADC.<br>0: normal averaging.<br>1: rolling average. | 0x0 | R/W |
| [8:6] | OSR | Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal averaging mode supports oversampling ratios of 2×, 4×, 8×, 16×, and 32×. Rolling average mode supports oversampling ratios of 2×, 4×, and 8×.<br>000: disabled.<br>001: 2×.<br>010: 4×.<br>011: 8×.<br>100: 16×.<br>101: 32×.<br>110: disabled.<br>111: disabled. | 0x0 | R/W |
| 5 | CRC_W | CRC Write. Controls the CRC functionality for the SDI interface When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0.<br>0: no CRC function.<br>1: CRC function. | 0x0 | R/W |
| 4 | CRC_R | CRC Read. Controls the CRC functionality for the SDOx interface.<br>0: no CRC function.<br>1: CRC function. | 0x0 | R/W |
| 3 | ALERT_EN | Enable Alert Indicator Function. This bit functions when the SDO bit = 01. Otherwise, the ALERT_EN bit is ignored.<br>0: SDOB.<br>1: $\overline{\text{ALERT}}$. | 0x0 | R/W |
| 2 | RES | Resolution. Sets the size of the conversion result data. If OSR = 0, the RES bit is ignored, and the resolution is set to default resolution.<br>0: normal resolution.<br>1: 2-bit higher resolution. | 0x0 | R/W |
| 1 | REFSEL | Reference Select. Selects the ADC reference voltage source.<br>0: selects internal reference.<br>1: selects external reference. | 0x0 | R/W |
| 0 | PMODE | Power-Down Mode. Sets the power modes. | 0x0 | R/W |

## REGISTERS

*Table 19. Bit Descriptions for CONFIGURATION1 Register (Continued)*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| | | 0: normal mode.<br>1: shutdown mode. | | |

## CONFIGURATION2 REGISTER

### Address: 0x2, Reset: 0x0000, Name: CONFIGURATION2

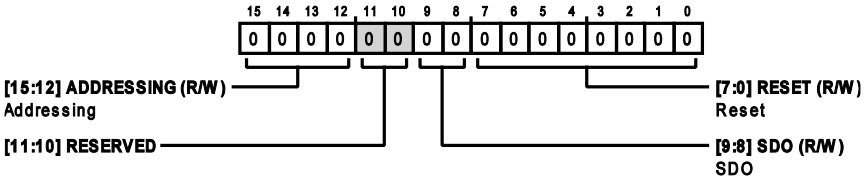



*Table 20. Bit Descriptions for CONFIGURATION2 Register*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:10] | RESERVED | Reserved. | 0x0 | R |
| [9:8] | SDO | SDO. Conversion Results Serial Data Output.<br>00: 2-wire output. Conversion data are output on both SDOA and SDOB.<br>01: 1-wire output. Conversion data are output on SDOA only.<br>10: 4-wire output. Conversion data are output on SDOA, SDOB, SDOC, and SDOD/$\overline{\text{ALERT}}$.<br>11: 1-wire output. Conversion data are output on SDOA only. | 0x0 | R/W |
| [7:0] | RESET | Reset.<br>0x3C: performs a soft reset. Refreshes some blocks. Register contents remain unchanged. Clears the $\overline{\text{ALERT}}$ indication register and flushes any oversampling stored variables or active state machine.<br>0xFF: performs a hard reset. Resets all possible blocks in the AD7383-4/AD7384-4. Register contents are set to defaults. All other values are ignored. | 0x0 | R/W |

## $\overline{\text{ALERT}}$ INDICATION REGISTER

### Address: 0x3, Reset: 0x0000, Name: $\overline{\text{ALERT}}$

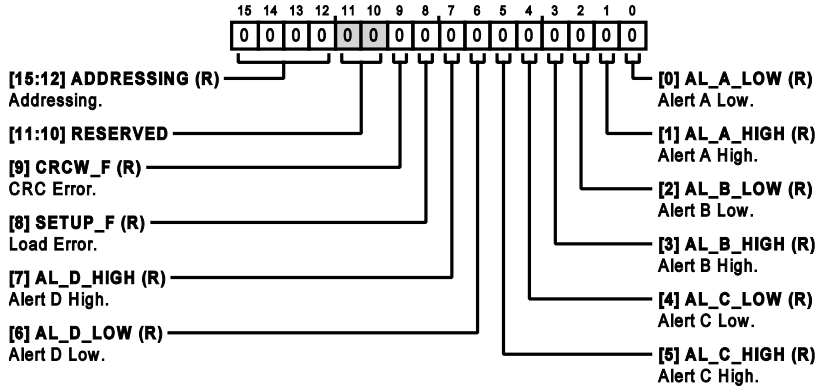



*Table 21. Bit Descriptions for $\overline{\text{ALERT}}$ Indication Register*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R |

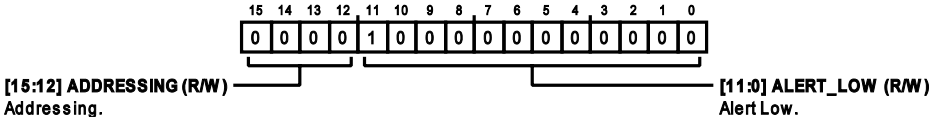
## REGISTERS

*Table 21. Bit Descriptions for $\overline{ALERT}$ Indication Register (Continued)*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [11:10] | RESERVED | Reserved. | 0x0 | R |
| 9 | CRCW_F | CRC Error. The CRCW_F indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read.<br>0: no CRC error.<br>1: CRC error. | 0x0 | R |
| 8 | SETUP_F | Load Error. The SETUP_F indicates that the device configuration data did not load correctly on startup. This bit does not clear on an alert indication register read. A hard reset via the CONFIGURATION 2 register is required to clear this bit and restart the device setup.<br>0: no setup error.<br>1: setup error. | 0x0 | R |
| 7 | AL_D_HIGH | Alert D High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| 6 | AL_D_LOW | Alert D Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>0: no alert indication.<br>1: alert indication. | 0x0 | R |
| 5 | AL_C_HIGH | Alert C High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| 4 | AL_C_LOW | Alert C Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| 3 | AL_B_HIGH | Alert B High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| 2 | AL_B_LOW | Alert B Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| 1 | AL_A_HIGH | Alert A High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>0: no alert indication.<br>1: alert indication. | 0x0 | R |
| 0 | AL_A_LOW | Alert A Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |

## ALERT_LOW_THRESHOLD REGISTER

### Address: 0x4, Reset: 0x0800, Name: ALERT_LOW_THRESHOLD



## REGISTERS

*Table 22. Bit Descriptions for ALERT_LOW_THRESHOLD Register*

| Bits | Bit Name | Descriptions | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:0] | ALERT_LOW | Alert Low. Bits[11:0] from ALERT_LOW move to the MSBs of the internal alert low register, D[15:4]. The remaining bits, D[3:0] of the internal register are fixed at 0x0. Sets an alert when the converter result is below the value in the ALERT_LOW_THRESHOLD register, and the alert is disabled when it is above the value in the ALERT_LOW_THRESHOLD register. | 0x800 | R/W |

### ALERT_HIGH_THRESHOLD REGISTER

#### Address: 0x5, Reset: 0x07FF, Name: ALERT_HIGH_THRESHOLD

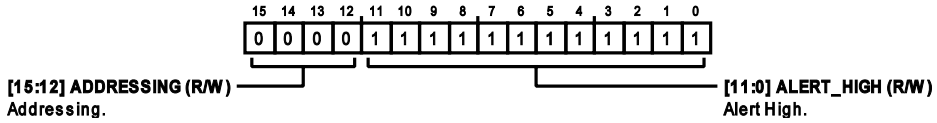



*Table 23. Bit Descriptions for ALERT_HIGH_THRESHOLD Register*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits [15:12] define the address of the relevant register. See the Addressing Registers Section for further details. | 0x0 | R/W |
| [11:0] | ALERT_HIGH | Alert High. Bits D[11:0] from ALERT_HIGH move to the MSBs of the internal alert high register, D[15:4]. The remaining bits, D[3:0] of the internal are fixed at 0xF. Sets an alert when the converter result is above the value in the ALERT_HIGH_THRESHOLD register, and the alert is disabled when it is below the value in the ALERT_HIGH_THRESHOLD register. | 0xFFF | R/W |

## OUTLINE DIMENSIONS

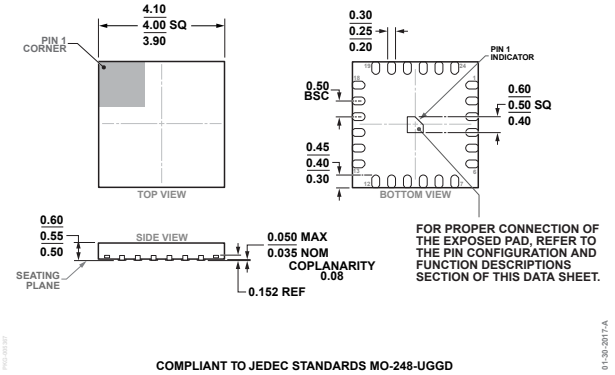



*Figure 42. 24-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.55 mm Package Height*
*(CP-24-25)*
*Dimensions shown in millimeters*

Updated: April 18, 2023

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option | Marking Code |
|---|---|---|---|---|---|
| AD7383-4BCPZ | -40°C to +125°C | 24-Lead LFCSP (4mm x 4mm x 0.55mm) | Tray, 490 | CP-24-25 | |
| AD7383-4BCPZ-RL | -40°C to +125°C | 24-Lead LFCSP (4mm x 4mm x 0.55mm) | Reel, 5000 | CP-24-25 | |
| AD7383-4BCPZ-RL7 | -40°C to +125°C | 24-Lead LFCSP (4mm x 4mm x 0.55mm) | Reel, 1000 | CP-24-25 | |
| AD7384-4BCPZ | -40°C to +125°C | 24-Lead LFCSP (4mm x 4mm x 0.55mm) | Tray, 490 | CP-24-25 | CA6 |
| AD7384-4BCPZ-RL | -40°C to +125°C | 24-Lead LFCSP (4mm x 4mm x 0.55mm) | Reel, 5000 | CP-24-25 | CA6 |
| AD7384-4BCPZ-RL7 | -40°C to +125°C | 24-Lead LFCSP (4mm x 4mm x 0.55mm) | Reel, 1000 | CP-24-25 | CA6 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

*Table 24. Evaluation Boards*

| Model[1] | Description |
|---|---|
| EVAL-AD7383-4FMCZ | Evaluation Board |

[1] Z=RoHS-Compliant Part