Evaluating the ADL8100 GaAs, pHEMT, MMIC, Low Noise Amplifier, 0.01 GHz to 20 GHz

FEATURES

- 2-layer Rogers 4350B evaluation boards with heat spreaders
- End launch, 2.9 mm RF connectors
- Through calibration path (depopulated connectors)

EVALUATION KIT CONTENTS

- ADL8100ACPZN-EVALZ evaluation board that requires external bias tee
- ADL8100ACPZN-EVAL1Z evaluation board that has an on-board bias tee

EQUIPMENT NEEDED

- RF signal generator
- RF spectrum analyzer
- RF network analyzer
- 5 V, 500 mA power supply
- External DC block for ADL8100ACPZN-EVALZ
- Marki Microwave BT2-0040 wideband bias tee for ADL8100ACPZN-EVALZ

GENERAL DESCRIPTION

The ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z are 2-layer printed circuit boards (PCB) fabricated from 10 mil thick, Rogers 4350B, copper clad, mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow attachment to larger heat sinks for improved thermal management.

The RFIN and RFOUT ports on the ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z are populated with 2.9 mm, female coaxial connectors, and the respective RF traces have a 50 Ω characteristic impedance. The ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z are populated with components suitable for use over the entire −40°C to +85°C operating temperature range.

To calibrate out board trace losses, a through calibration path, THRUCAL, is provided between the THRUCAL connectors (J1 and J2). THRUCAL must be populated with RF connectors to use the through calibration path.

The power voltages and ground path are accessed through surface-mounted technology (SMT) test points.

An external wideband bias tee must be connected to RFOUT of the ADL8100ACPZN-EVALZ to provide bias current and AC coupling on RFOUT. The BT2-0040 from Marki Microwave is recommended. The ADL8100ACPZN-EVAL1Z has an on-board SMT bias tee.

For full details on the ADL8100, see the ADL8100 data sheet, which must be consulted in conjunction with this user guide when using the ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z.

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REVISION HISTORY

7/2023—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

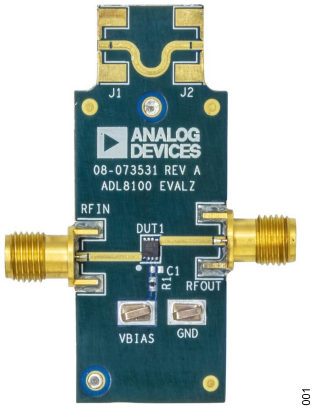

Figure 1. ADL8100ACPZN-EVALZ Component Side (Requires External Bias Tee)

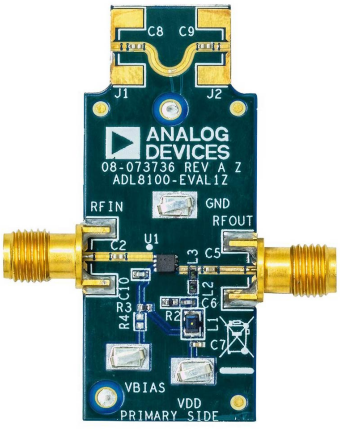

Figure 2. ADL8100ACPZN-EVAL1Z Component Side (Includes On Board Bias Tee)

Figure 3. ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z Bottom Side

EVALUATION BOARD HARDWARE

PROVIDING DC BIAS TO ADL8100ACPZN-EVALZ USING A CONNECTORIZED BIAS TEE

A 5 V, 500 mA supply is required to provide the bias to the ADL8100ACPZN when using the ADL8100ACZPN-EVALZ. Connect the 5 V supply through an external bias tee, such as the Marki Microwave BT2-0040, to the RFOUT port (see Figure 4). Connect the same 5 V supply to the VBIAS SMT test point. A connectorized DC blocking capacitor must be connected to the RFIN port because there no AC coupling capacitors on the RF input trace on the ADL8100ACPZN-EVALZ. The R1 value (default value is 560 Ω) sets the total current (I_{DQ}) to 220 mA.

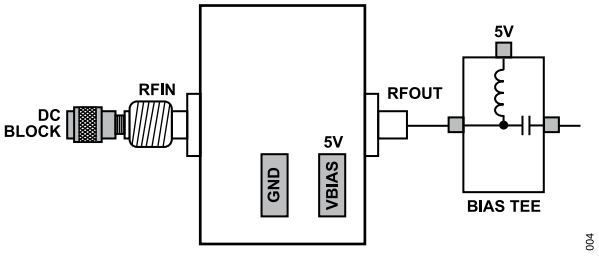

Figure 4. ADL8100ACPZN-EVALZ Operation Using a Connectorized Bias Tee

RECOMMENDED BIAS SEQUENCING FOR ADL8100ACPZN-EVALZ AND ADL8100ACPZN-EVAL1Z

To avoid damaging the device, pay careful attention to the sequencing of the RF input, the bias voltage, and the drain bias voltage. The following power-up sequence is recommended:

1. Connect GND.
2. Increase the voltage on the VBIAS SMT test point and the external bias tee to 5 V.
3. Apply the RF signal.

The following power-down sequence is recommended:

1. Turn off the RF signal.
2. Reduce the voltage on the VBIAS SMT test point and the external bias tee to 0 V.

PERFORMANCE COMPARISON OF ADL8100ACPZN-EVALZ AND ADL8100ACPZN-EVAL1Z

Figure 5 and Figure 6 show the return loss of the ADL8100ACPZN-EVALZ and the ADL8100ACPZN-EVAL1Z. The external bias tee of the ADL8100ACPZN-EVALZ has been de-embedded for the performance measurement. The SMT bias tee components on the ADL8100ACPZN-EVAL1Z slightly reduce gain across frequency, as shown in Figure 6.

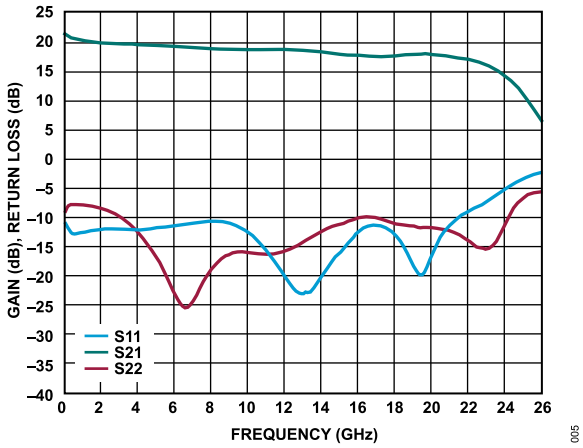

Figure 5. ADL8100ACPZN-EVALZ Performance (Requires External Bias Tee)

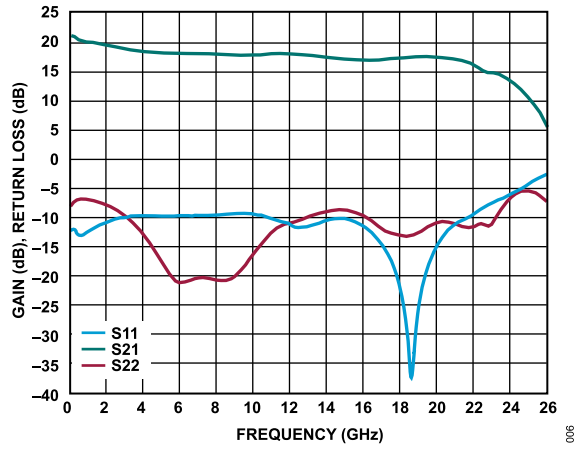

Figure 6. ADL8100ACPZN-EVAL1Z Performance (SMT Bias Tee)

THROUGH CALIBRATION PATH

The ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z include a calibration path (see the evaluation board schematic in Figure 9 and Figure 11). THRUCAL (J1 and J2) must be populated with RF connectors to use the through calibration path. In the case of the ADL8100ACPZN-EVAL1Z, the through calibration path includes two AC coupling capacitors (populated) to mimic the AC coupling capacitors in the main signal path. Figure 7 and Figure 8 show the insertion loss, input return loss, and output return loss of the through calibration path for the ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z, respectively. Table 1 and Table 2 list the insertion loss of the through calibration paths for the ADL8100ACPZN-EVALZ and ADL8100ACPZN-EVAL1Z, respectively.

EVALUATION BOARD HARDWARE

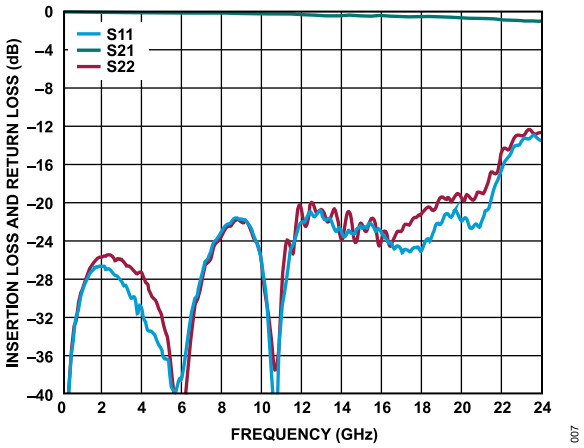

Figure 7. Insertion Loss and Return Loss (Input and Output) of the Through Calibration Path (ADL8100ACPZN-EVALZ)

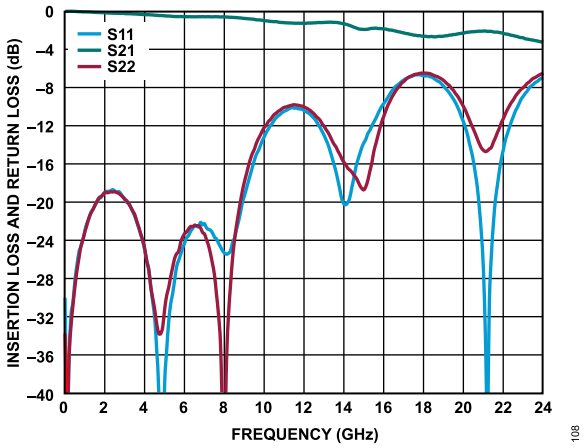

Figure 8. Insertion Loss and Return Loss (Input and Output) of the Through Calibration Path (ADL8100ACPZN-EVAL1Z)

Table 1. Insertion Loss of the Through Calibration Path (ADL8100ACPZN-EVALZ)

Frequency (GHz)	Insertion Loss (dB)
0.01	−0.001
0.20	−0.01
0.5	−0.02
0.70	−0.03
1	−0.05
3	−0.12
5	−0.15
7	−0.17
9	−0.23
11	−0.25
13	−0.37
15	−0.41
17	−0.48
19	−0.59
21	−0.73
23	−0.95
25	−0.94

Table 2. Insertion Loss of the Through Calibration Path (ADL8100ACPZN-EVAL1Z)

Frequency (GHz)	Insertion Loss (dB)
0.01	−0.02
0.20	−0.02
0.5	−0.03
0.70	−0.06
1	−0.08
3	−0.25
5	−0.49
7	−0.59
9	−0.76
11	−1.20
13	−1.19
15	−1.92
17	−2.28
19	−2.62
21	−2.09
23	−2.79
25	−3.54

EVALUATION BOARD SCHEMATICS AND ARTWORK

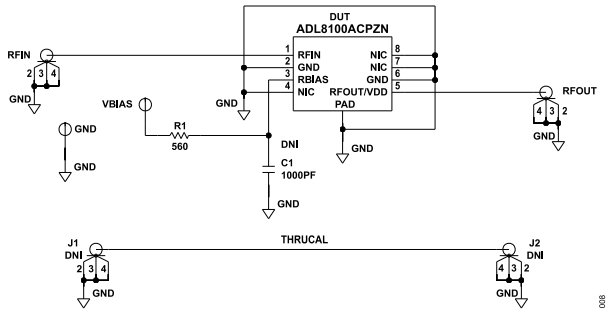

Figure 9. ADL8100ACPZN-EVALZ Schematic

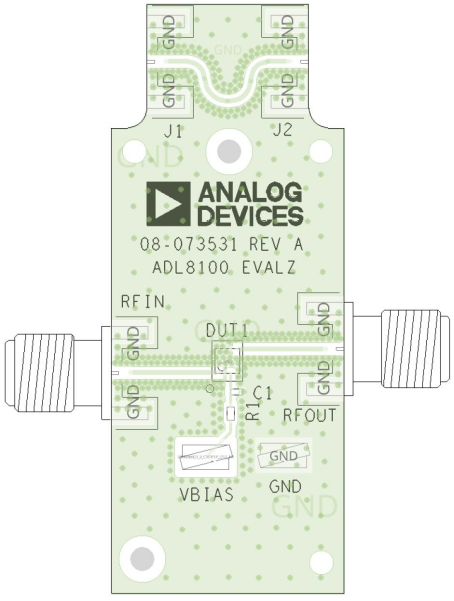

Figure 10. ADL8100ACPZN-EVALZ Assembly Drawing (J1 and J2 Not Installed)

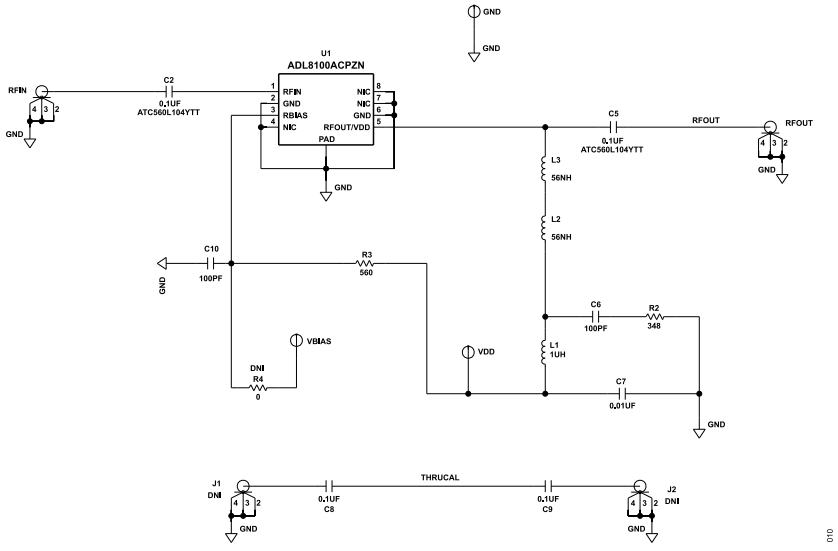

Figure 11. ADL8100ACPZN-EVAL1Z Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

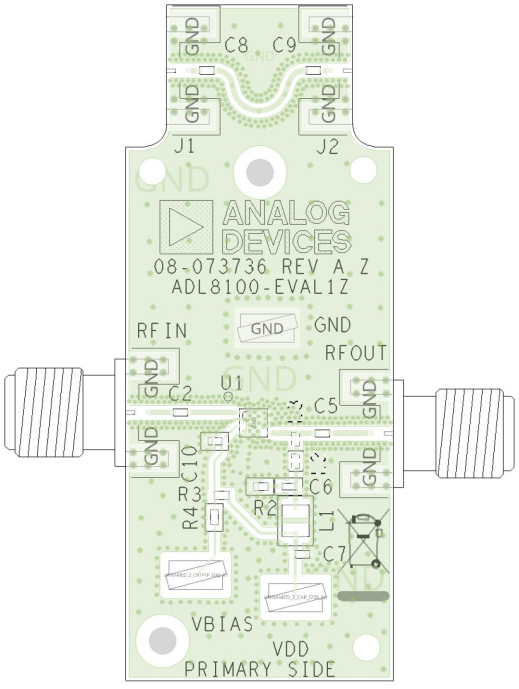

Figure 12. ADL8100ACPZN-EVAL1Z Assembly Drawing (J1 and J2 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. ADL8100ACPZN-EVALZ Bill of Materials

Reference Designator	Description	Manufacturer	Manufacturer Number
C1	1000 pF capacitor, 0402, do not install (DNI)	MURATA	GRM1555C1H102JA01
R1	560 Ω resistor, surface-mounted device (SMD), 0402	PANASONIC	ERJ-2RKF5600X
VBIAS, GND	Connectors, SMT test points	Keystone Electronics	5016
RFIN, RFOUT	Connectors, K jack edge	SRI Connector Gage Co.	25-146-1000-92
J1, J2	Connectors, K jack edge, DNI	SRI Connector Gage Co.	25-146-1000-92
U1	Wideband, low noise amplifier, single positive supply, 0.01 GHz to 20 GHz	Analog Devices, Inc.	ADL8100ACPZN

Table 4. ADL8100ACPZN-EVAL1Z Bill of Materials

Reference Designator	Description	Manufacturer	Manufacturer Number
C6, C10	Ceramic capacitor, 100 pF, 50 V, 5% C0G, 0402	Yageo	CC0402JRNPO9BN101
C2, C5, C8, C9	Ceramic capacitor, 0.1 µF, 16 V, 20% to +25% , 0402	AMERICAN TECHNICAL CERAMICS	ATC560L104YTT
C7	Ceramic capacitor, 0.01 µF, 25 V, 10% X8R, 0402	TDK	C1005X8R1E103K
VBIAS, GND, VDD	Connectors, SMT test points	Keystone Electronics	5016
L1	Inductor fixed unshielded, 1 µH, 0.5 A, 0.69 Ω 0805	Coilcraft	0805LS-102XJLC
L2, L3	Inductor chip, 56 NH, 5%, 0.061 Ω, DCR, 1.2 A	Coilcraft	0402DF-560XJR
R2	Resistor SMD, 348 Ω, 1%, 1/10 W, 0402	Panasonic	ERJ2RKF3480X
R3	Resistor SMD, 560 Ω 1%, 1/10 W, 0402	Panasonic	ERJ-2RKF5600X
R4	Resistor SMD, 0 Ω jumper, 1/10 W, 0402, DNI	Panasonic	ERJ-2GE0R00X
RFIN, RFOUT	Connectors, K jack edge	SRI Connector Gage Co.	25-146-1000-92
J1, J2	Connectors, K jack edge, DNI	SRI Connector Gage Co.	25-146-1000-92
U1	Wideband, low noise amplifier, single positive supply, 0.01 GHz to 20 GHz	Analog Devices, Inc.	ADL8100ACZPN

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.