Data Sheet

ADA4511-2

Precision, 40 V, Rail-to-Rail Input and Output Op Amp

FEATURES

- Low-offset voltage drift: ±2 µV/°C maximum
- Low-offset voltage: ±75 µV maximum
- Low-voltage noise: 1 µV p-p from 0.1 Hz to 10 Hz typical
- Low-voltage noise density: 5 nV/√Hz typical at f = 1 kHz
- High common-mode rejection: 140 dB typical
- Low-input bias current: ±10 pA maximum
- Wide gain bandwidth product: 10.4 MHz typical
- High slew rate: 19 V/µs typical
- Low THD: −134 dB at f = 1 kHz
- Low-quiescent supply current: 1.45 mA per amplifier typical
- Wide supply voltage operation: 6 V to 40 V, ±3 V to ±20 V
- Integrated EMI filter
- Multiplexer compatible inputs
  - Rail-to-rail high impedance inputs: differential and common-mode
  - Fast settling time
- Rail-to-rail output
- No phase reversal
- Heavy capacitive load drive capability: 1 nF
- Wide specified temperature range: −40°C to +125°C
- Available in 8-lead standard small-outline package (SOIC_N)

GENERAL DESCRIPTION

The ADA4511-2[1] is a dual-channel, 40 V, high precision, low-input bias current, low-offset voltage, low-offset voltage drift, low noise, rail-to-rail input and output operational amplifier (op amp) that can be used at any point of the signal chain, which includes sensing, conditioning, and output drive. Through trimming, the ADA4511-2 achieves low offset drift (±0.4 µV/°C typical, ±2 µV/°C maximum) and low offset voltage (±25 µV typical, ±75 µV maximum).

The ADA4511-2 delivers top DC accuracy and AC precision, which makes it suitable for a wide variety of signal chain applications. By integrating a robust mux-compatible architecture, the ADA4511-2 effectively solves common system distortion and settling problems and provides the superior accuracy required in multiplexed multi-channel precision signal chains. The ADA4511-2 is specified from −40°C to +125°C and is available in an 8-lead, SOIC_N package.

APPLICATIONS

- Data acquisition systems
- Multiplexed input signal chains
- Industrial automation
- Medical instruments
- Electronic test and measurement
- Precision current measurement
- Photodiode amplifiers

TYPICAL APPLICATION CIRCUIT

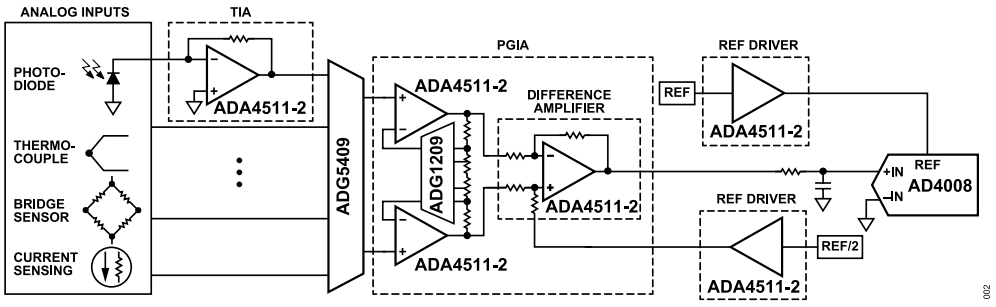

Figure 1. Multiplexed Data Acquisition Signal Chain

[1] Protected by U.S. patent number 11,329,612; other patents pending.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

1/2024—Revision 0: Initial Version

COMPANION PRODUCTS

- **ADC:** AD4695/AD4696, AD4697/AD4698, AD4000/AD4004/AD4008
- **ADC Drivers:** ADA4945-1, LTC6363, AD8475
- **Voltage References:** LTC6655, ADR4525
- **Power:** LT3032, ADP5070, LT3093, LT3042

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V+ = +20 V, V− = −20 V, common-mode voltage (V_{CM}) = 0 V, load resistor (R_L) = 10 kΩ to midsupply, ambient temperature (T_A) = 25°C, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Offset Voltage (V_{OS})	V_{CM} = 0 V, (V+) − 1.5 V		±25	±75	μV
Offset Voltage Drift ($\Delta V_{OS}/\Delta T$)	V_{CM} = 0 V				
	−40°C < T_A < +125°C		±0.4	±2	μV/°C
	V_{CM} = (V+) − 1.5 V				
	−40°C < T_A < +125°C		±0.7	±4.4	μV/°C
Input Bias Current (I_B)			±4	±10	pA
	−40°C < T_A < +85°C			±0.8	nA
	−40°C < T_A < +125°C			±18	nA
Input Offset Current (I_{OS})			±1.5	±5	pA
	−40°C < T_A < +85°C			±0.15	nA
	−40°C < T_A < +125°C			±5	nA
Input Voltage Range (IVR)	CMRR > 99 dB	(V−) − 0.15		V+	V
Common-Mode Rejection Ratio (CMRR)	(V−) − 0.15 < V_{CM} < (V+) − 3 V	121	140		dB
	−40°C < T_A < +125°C, (V−) < V_{CM} < (V+) − 3 V	109			dB
Open-Loop Voltage Gain (A_{VOL})	R_L = 10 kΩ, (V−) + 0.3 V < V_{OUT} < (V+) − 0.3 V	126	140		dB
	−40°C < T_A < +125°C	112			dB
	R_L = 2 kΩ, (V−) + 0.9 V < V_{OUT} < (V+) − 0.9 V	121	134		dB
	−40°C < T_A < +125°C	106			dB
Input Capacitance					
Differential Mode (C_{INDM})			20		pF
Common Mode (C_{INCM})			2		pF
Input Resistance					
Differential Mode (R_{INDM})			1		TΩ
Common Mode (R_{INCM})			10		TΩ
NOISE PERFORMANCE					
Voltage Noise ($e_{n\ p-p}$)	0.1 Hz to 10 Hz		1		μV p-p
	0.1 Hz to 10 Hz, V_{CM} = (V+) − 1.5 V		2.7		μV p-p
Voltage Noise Density (e_n)	f = 100 Hz		8		nV/√Hz
	f = 1 kHz		5		nV/√Hz
	f = 100 Hz, V_{CM} = (V+) − 1.5 V		20		nV/√Hz
	f = 1 kHz, V_{CM} = (V+) − 1.5 V		10		nV/√Hz
Current Noise Density (I_n)	f = 10 Hz		4		fA/√Hz
OUTPUT CHARACTERISTICS					
Output Swing High (V_{OH})	((V+) − V_{OUT})				
	R_L = 10 kΩ		100	116	mV
	R_L = 2 kΩ		430	473	mV
Output Swing Low (V_{OL})	(V_{OUT} − (V−))				
	R_L = 10 kΩ		73	85	mV
	R_L = 2 kΩ		310	342	mV
Output Current (I_{OUT})	(V_{OH}, V_{OL}) < 1 V		±22		mA
Short-Circuit Current (I_{SC})	Sourcing/sinking		55/70		mA
Closed-Loop Output Impedance (Z_{OUT})	f = 1 kHz				

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Gain = 1		19		mΩ
	Gain = 10		190		mΩ
	Gain = 100		1.9		Ω
Open-Loop Output Impedance (Z_O)	f = 1 kHz to 1 MHz,		190		Ω
POWER SUPPLY					
(V+) − (V−) (V_{SY})	Guaranteed by PSRR	6		40	V
Power-Supply Rejection Ratio (PSRR)	V_{SY} = ±3 V to ±20 V	121	140		dB
	−40°C < T_A < +125°C	116			dB
Supply Current per Amplifier (I_{SY})	I_{OUT} = 0 mA		1.45	1.55	mA
	−40°C < T_A < +125°C			2	mA
DYNAMIC PERFORMANCE					
Slew Rate	V_{OUT} = ±5 V, Gain = 1, 10% to 90%		19		V/µs
Gain Bandwidth Product (GBP)	f = 100 kHz		10.4		MHz
−3 dB Bandwidth	Gain = 1		13.5		MHz
Settling Time (t_S)					
	To 0.01%				
	Gain = −1, V_{OUT} = 5 V step		1.9		µs
	Gain = −1, V_{OUT} = 10 V step		2.2		µs
	To 0.001%				
	Gain = −1, V_{OUT} = 5 V step		3.1		µs
	Gain = −1, V_{OUT} = 10 V step		3.5		µs
Output Overload Recovery Time	Gain = −10, positive/negative		300/100		ns
Total Harmonic Distortion (THD)	V_{OUT} = 10 V p-p, Gain = 1				
	f = 1 kHz		0.00002		%
	f = 1 kHz		−134		dB
	f = 50 kHz		0.00446		%
	f = 50 kHz		−87		dB
ELECTROMAGNETIC INTERFERENCE REJECTION RATIO (EMIRR)	EMIRR = 20 × $\log_{10}(\Delta V_{IN}/\Delta V_{OS})$, ΔV_{IN} = 200 mV p-p				
	f = 1000 MHz		71		dB
	f = 2400 MHz		81		dB

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
V_{SY} ((V+) − (V−))	−0.3 V to +45 V
Input V_{CM}	
(+IN A, −IN A, +IN B, −IN B) to V−	−0.3 V to +45 V
(+IN A, −IN A, +IN B, −IN B) to V+	+0.3 V to −45 V
Differential Input Voltage	
+IN A to −IN A, +IN B to −IN B	±45 V
Input Current	±10 mA
Output Short-Circuit Duration[1]	Thermally limited
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
T_J	150°C
Lead (soldering, 10 seconds)	300°C
T_C	260°C

[1] A heatsink may be required to keep the T_J below the absolute maximum rating when the output is shorted indefinitely.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
R-8	108.5	34.12	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2017.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002-2018.

ESD Ratings for ADA4511-2

Table 4. ADA4511-2, 8-Lead SOIC_N

ESD Model	Withstand Threshold (V)	Class
HBM	±1000	1C
FICDM	±400	C1

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

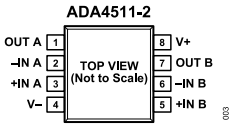

Figure 2. ADA4511-2 Pin Configuration

Table 5. Pin Function Descriptions, 8-Lead SOIC

Pin Number	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

V+ = +20 V, V− = −20 V, V_{CM} = 0 V, R_L = 10 kΩ to midsupply, T_A = 25°C, unless otherwise noted.

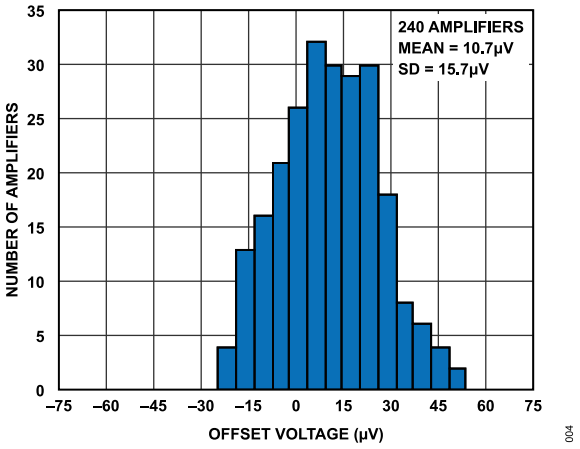

Figure 3. V_{OS} Distribution at 25°C

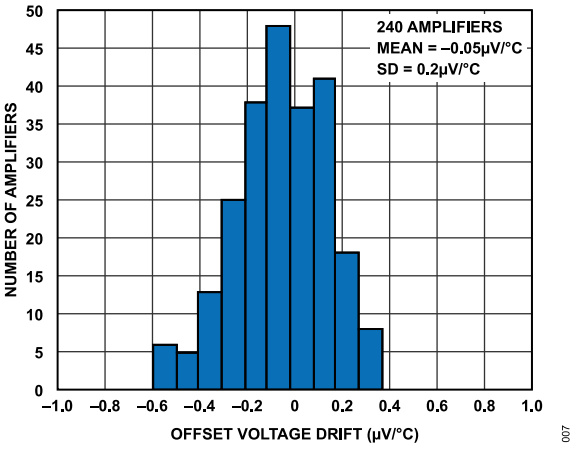

Figure 6. TCV_{OS} Distribution from −40°C to +125°C

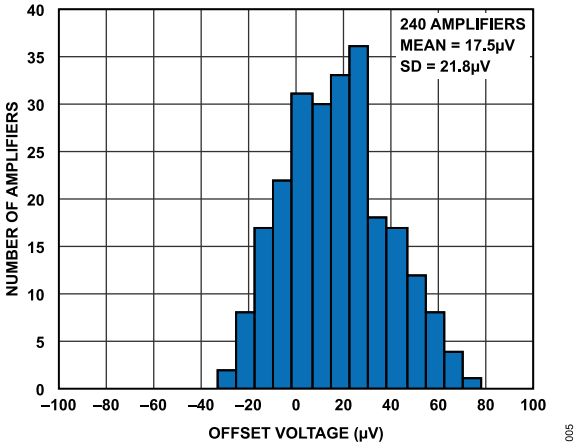

Figure 4. V_{OS} Distribution at −40°C

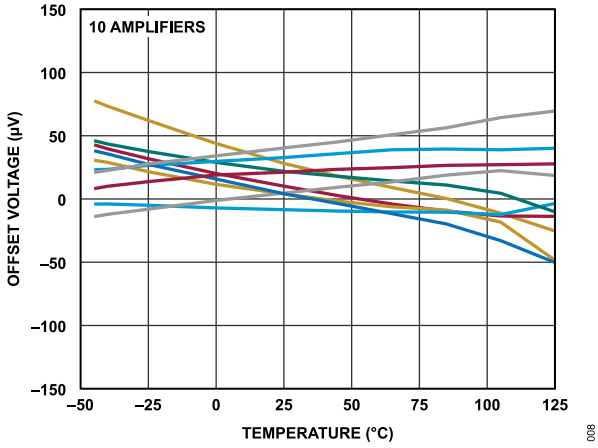

Figure 7. V_{OS} vs. Temperature

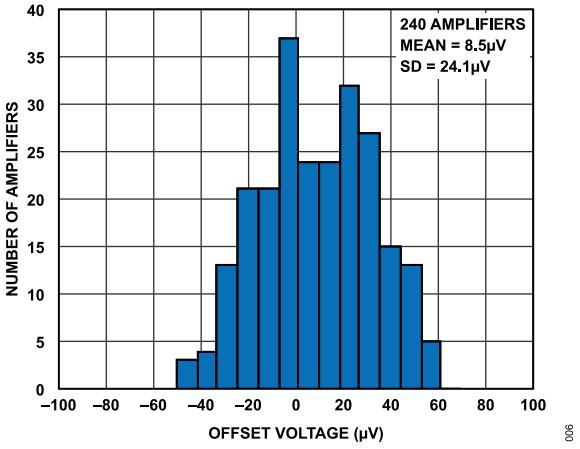

Figure 5. V_{OS} Distribution at 125°C

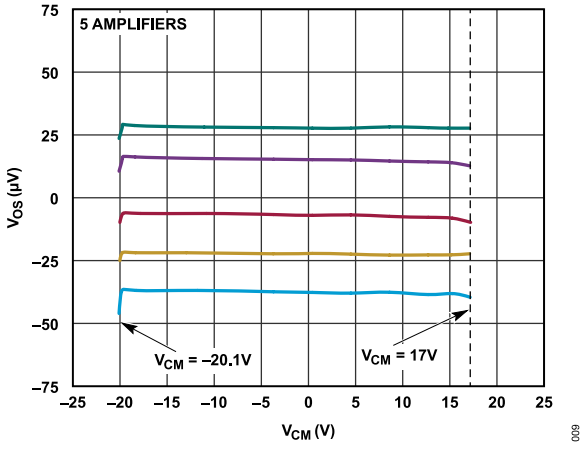

Figure 8. V_{OS} vs. V_{CM}

TYPICAL PERFORMANCE CHARACTERISTICS

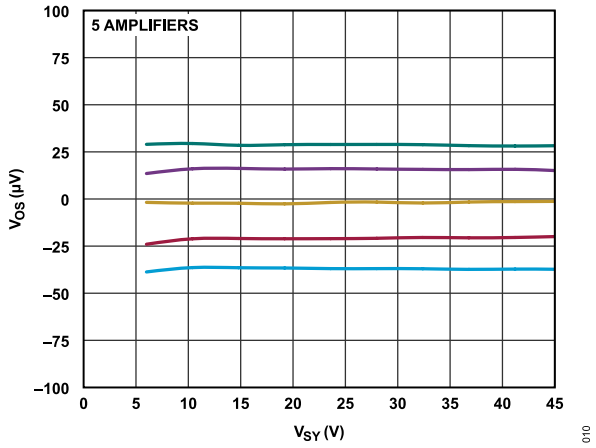

Figure 9. V_{OS} vs. V_{SY}

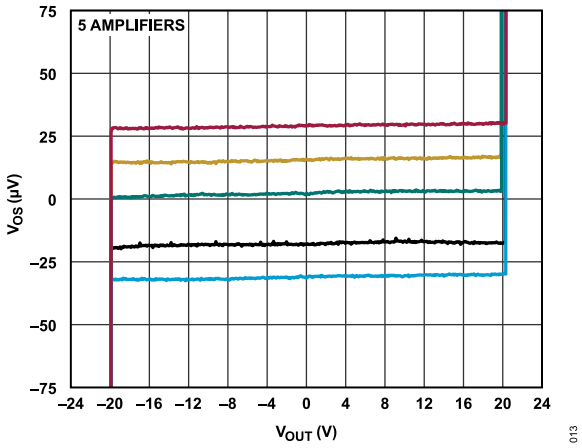

Figure 12. V_{OS} vs. V_{OUT}

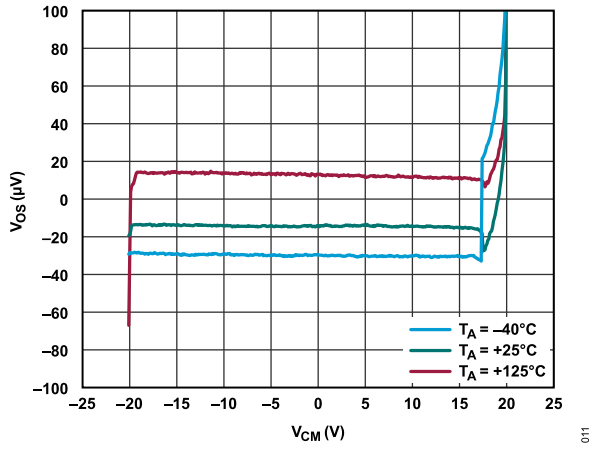

Figure 10. V_{OS} vs. V_{CM}, Three Temperatures

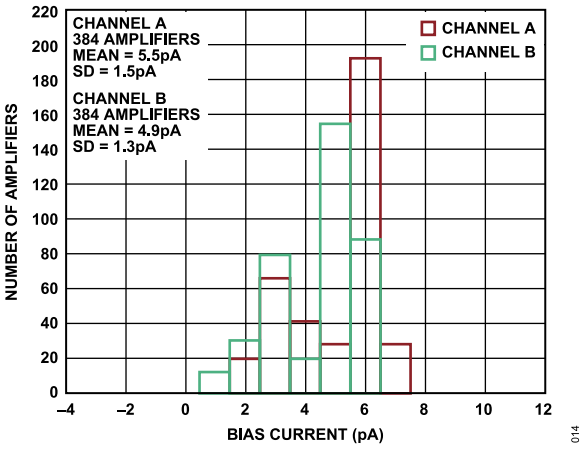

Figure 13. I_B Distribution at 25°C

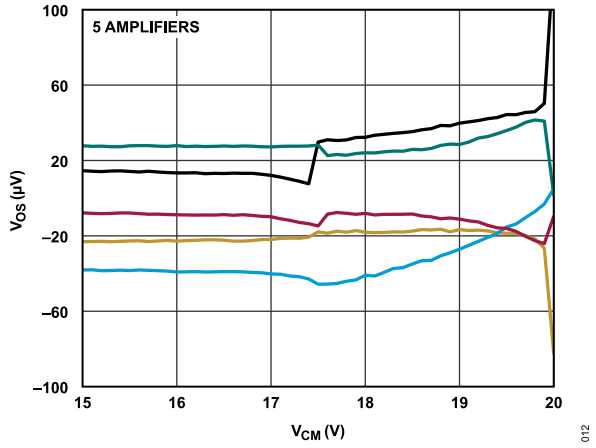

Figure 11. V_{OS} vs. V_{CM}, High V_{CM} Operation

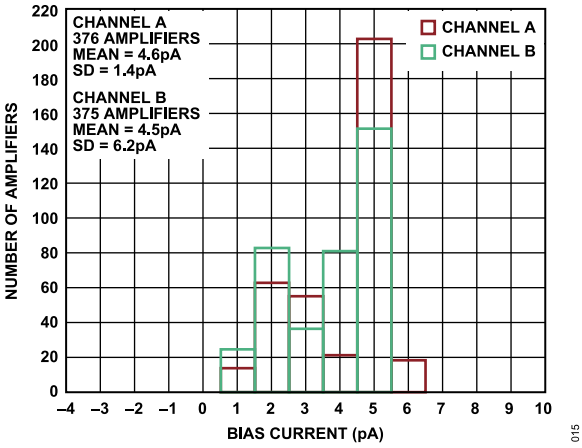

Figure 14. I_B Distribution at −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

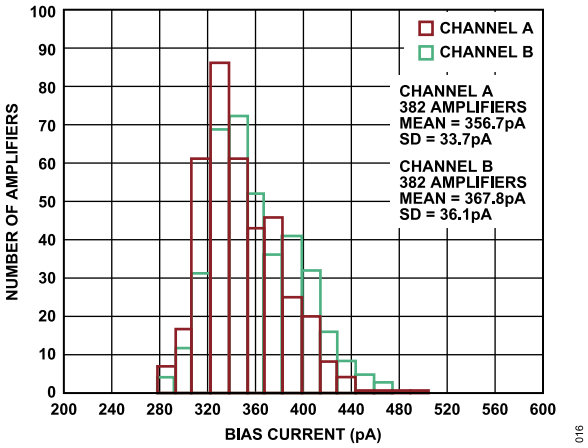

Figure 15. I_B Distribution at 85°C

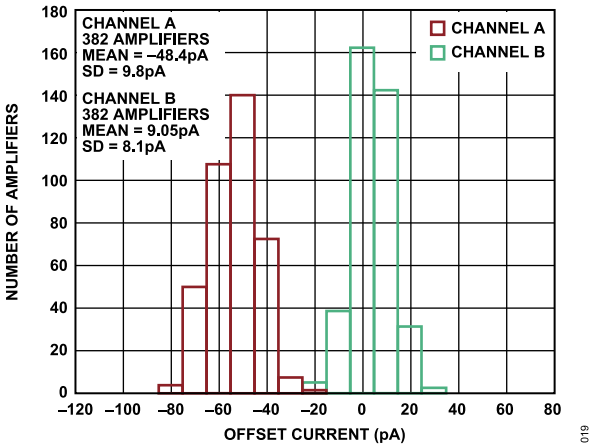

Figure 18. I_{OS} Distribution at 85°C

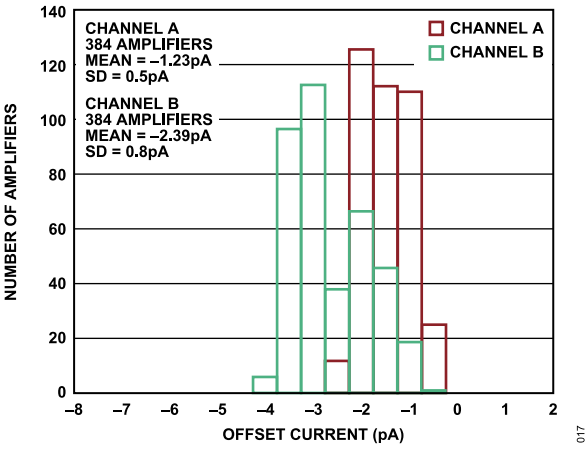

Figure 16. I_{OS} Distribution at 25°C

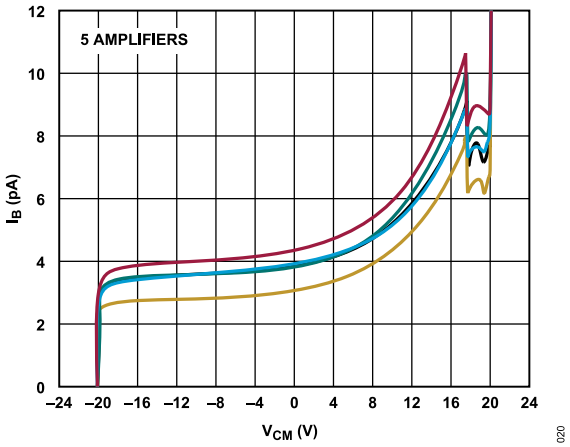

Figure 19. I_B vs. V_{CM}

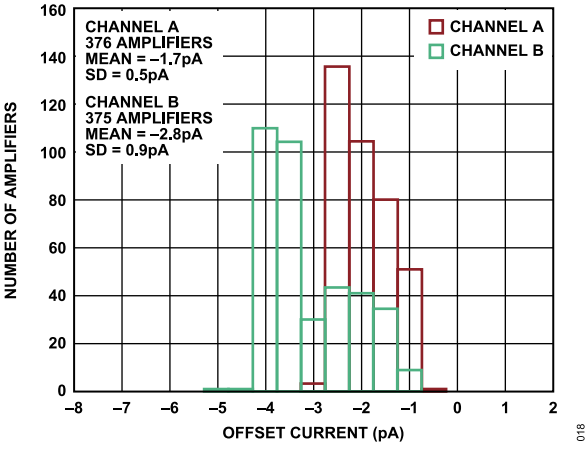

Figure 17. I_{OS} Distribution at −40°C

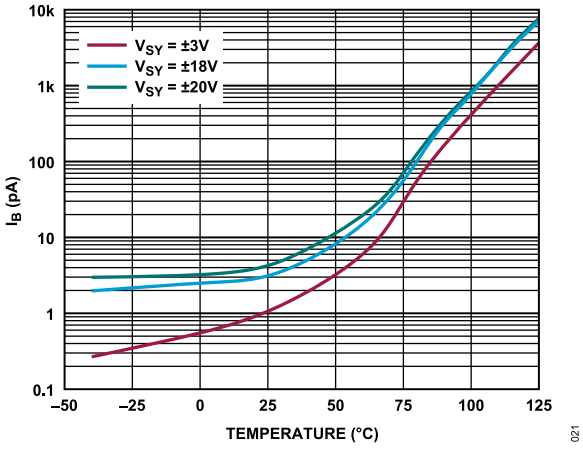

Figure 20. I_B vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

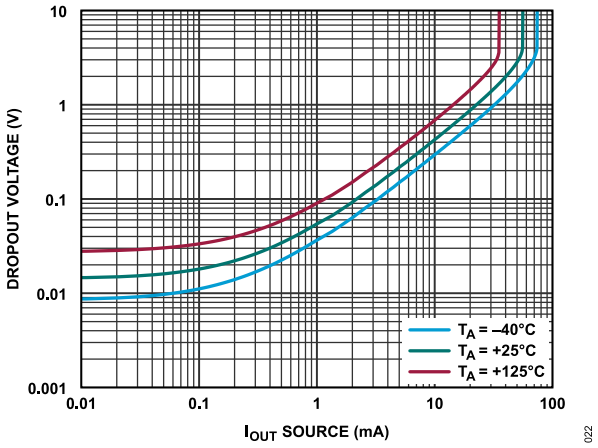

Figure 21. $V_{DROPOUT}$ ((V+) − V_{OUT}) vs. I_{OUT} Source

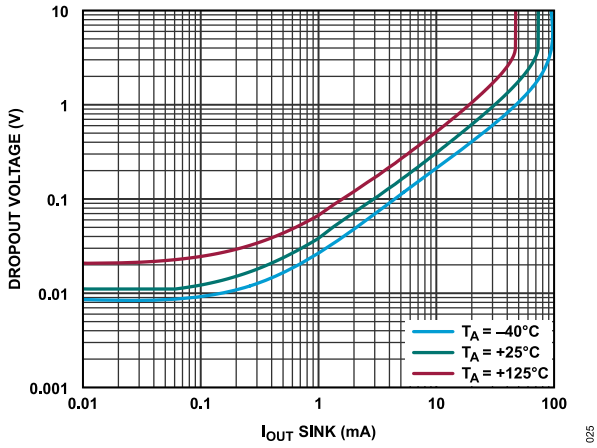

Figure 24. $V_{DROPOUT}$ (V_{OUT} − (V−)) vs. I_{OUT} Sink

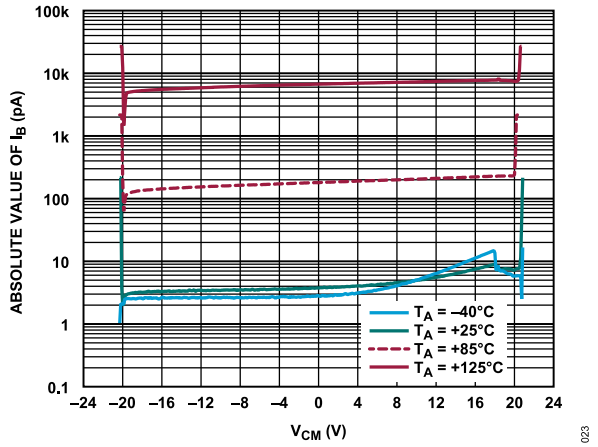

Figure 22. I_B vs. V_{CM}, Four Temperatures

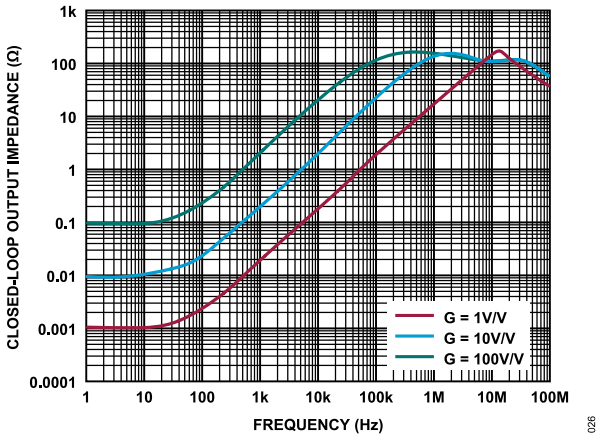

Figure 25. Z_{OUT} vs. Frequency

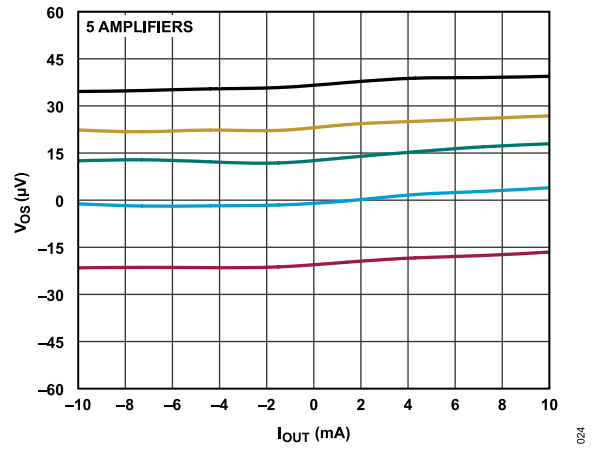

Figure 23. V_{OS} vs. I_{OUT}

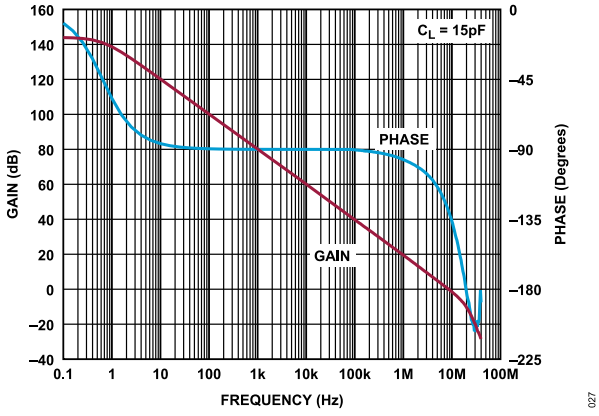

Figure 26. Open-Loop Gain and Phase vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

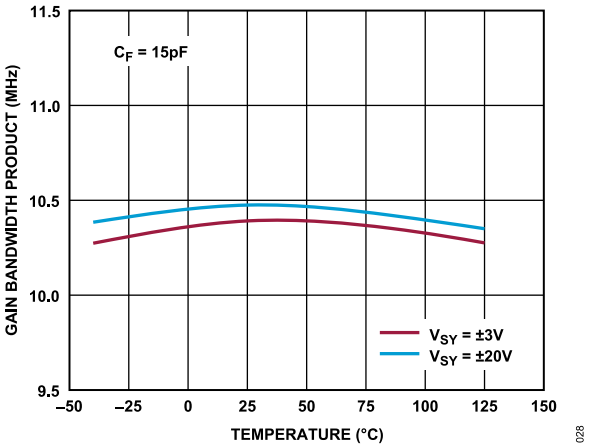

Figure 27. Gain Bandwidth Product vs. Temperature

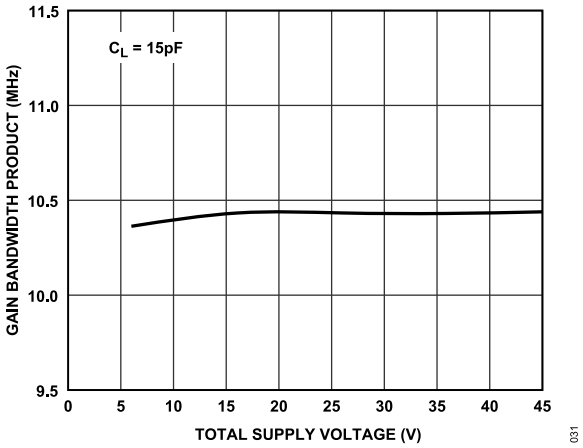

Figure 30. Gain Bandwidth Product vs. Total Supply Voltage

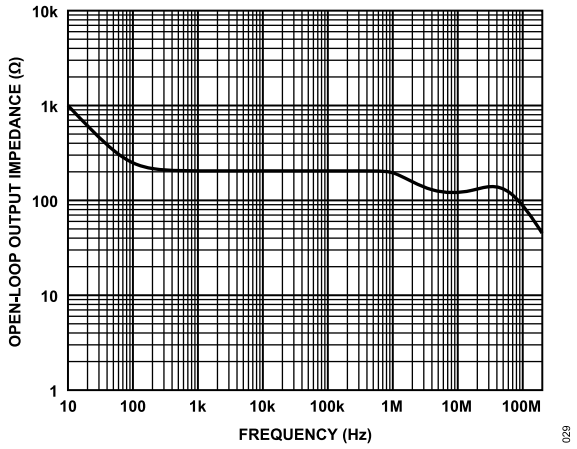

Figure 28. Z_O vs. Frequency

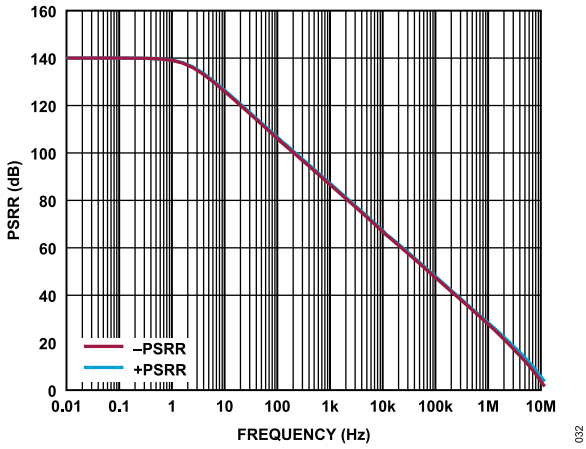

Figure 31. PSRR vs. Frequency

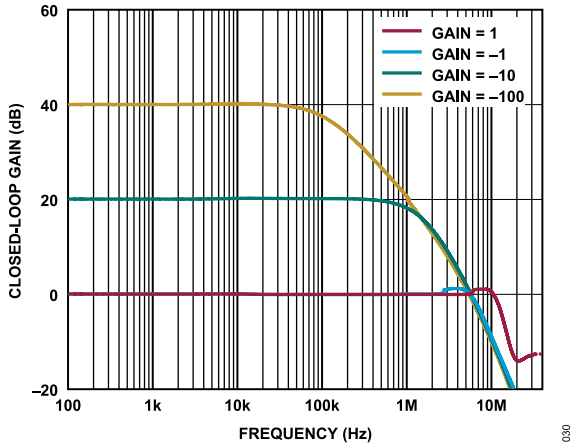

Figure 29. Closed-Loop Gain vs. Frequency

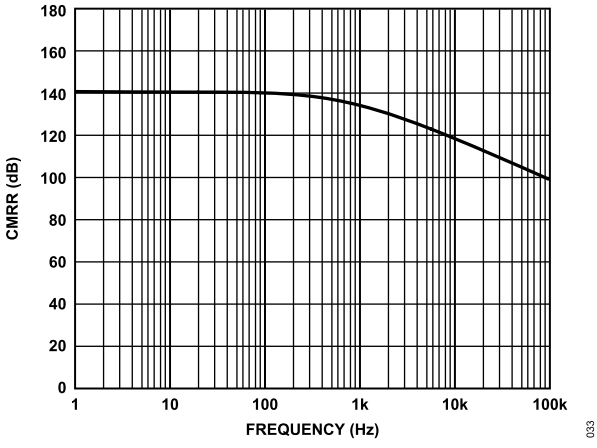

Figure 32. CMRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

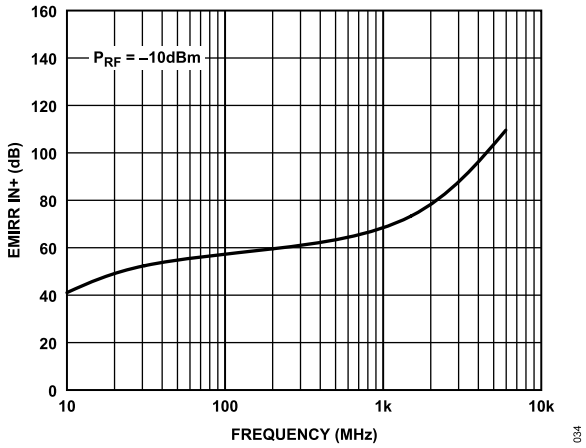

Figure 33. EMIRR IN+ vs. Frequency (P_{RF} = RF Power)

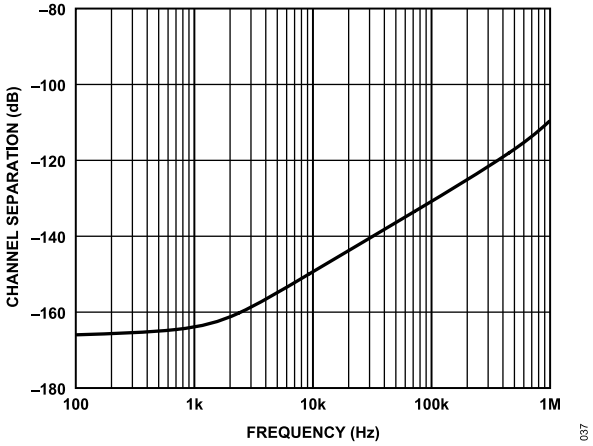

Figure 36. Channel Separation vs. Frequency

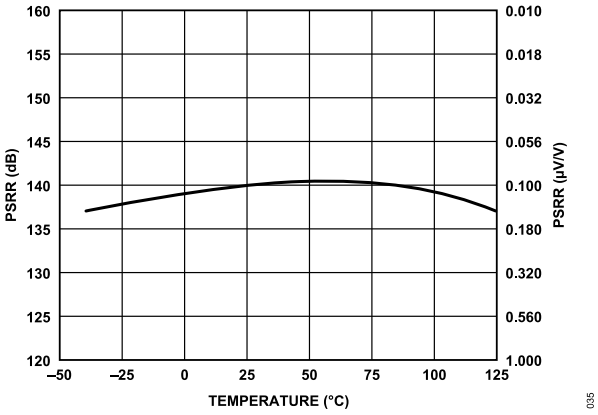

Figure 34. PSRR vs. Temperature

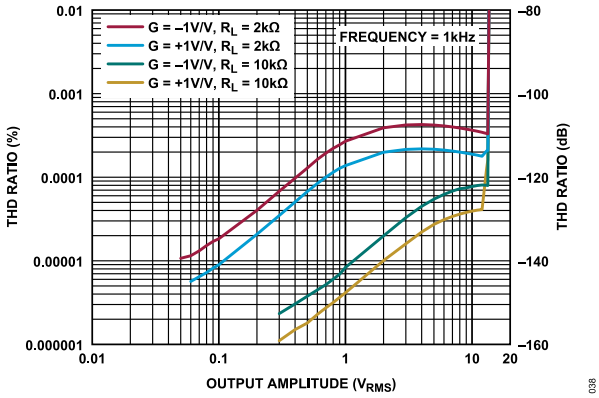

Figure 37. THD Ratio vs. Output Amplitude

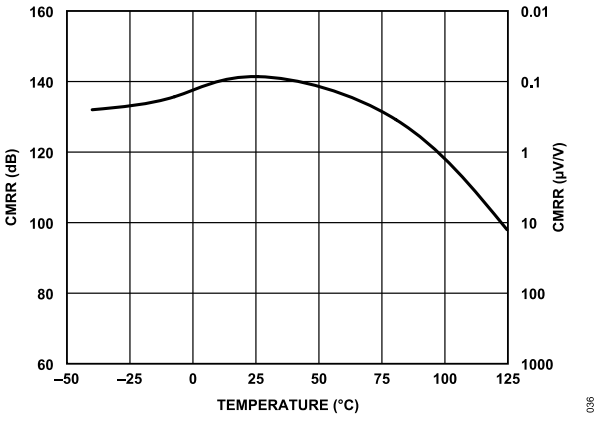

Figure 35. CMRR vs. Temperature

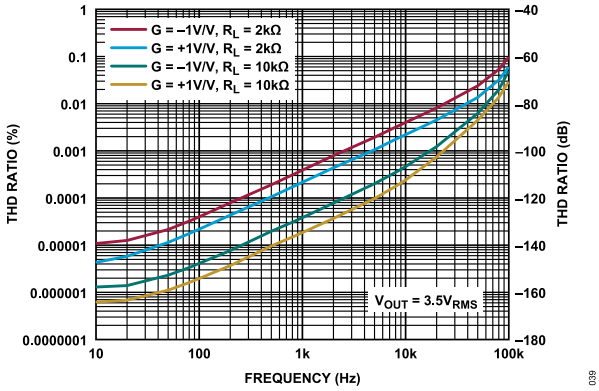

Figure 38. THD Ratio vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

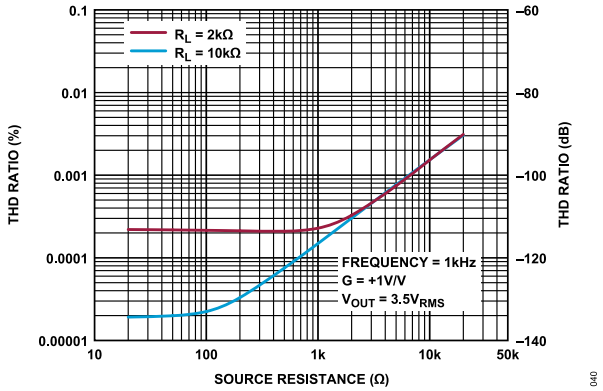

Figure 39. THD Ratio vs. Source Resistance

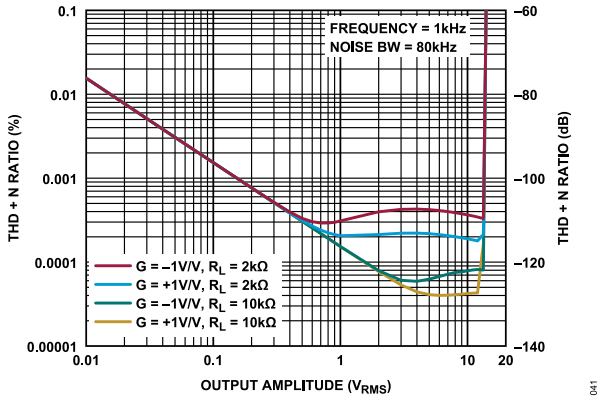

Figure 40. THD Plus Noise (THD + N) Ratio vs. Output Amplitude

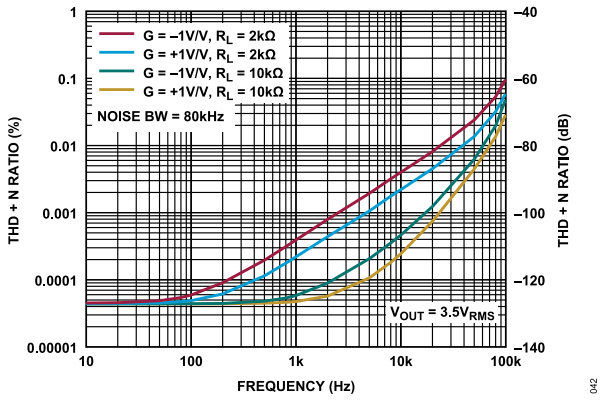

Figure 41. THD + N vs. Frequency

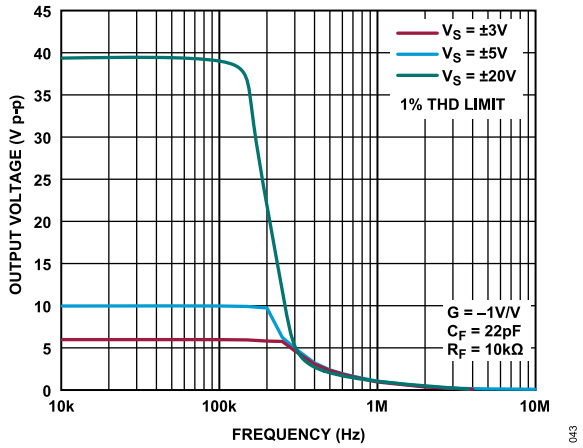

Figure 42. Maximum Undistorted Output Swing vs. Frequency

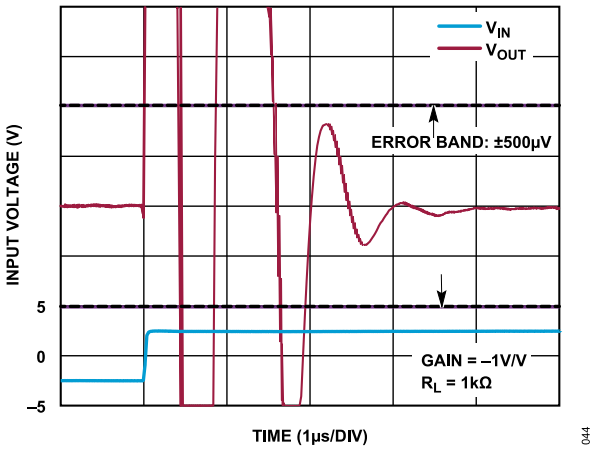

Figure 43. Positive Step Settling Time to 0.01%, V_{OUT} = 5 V

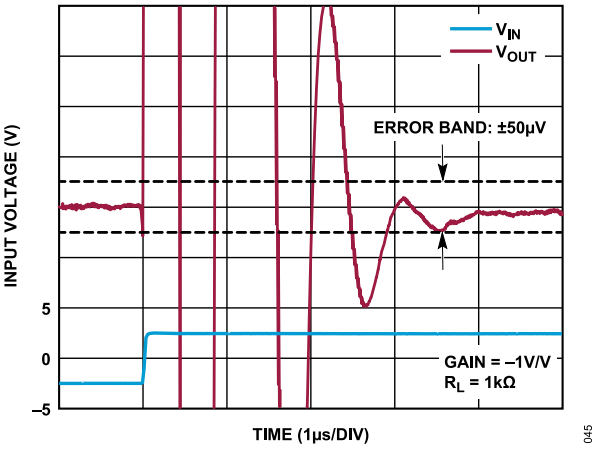

Figure 44. Positive Step Settling Time to 0.001%, V_{OUT} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

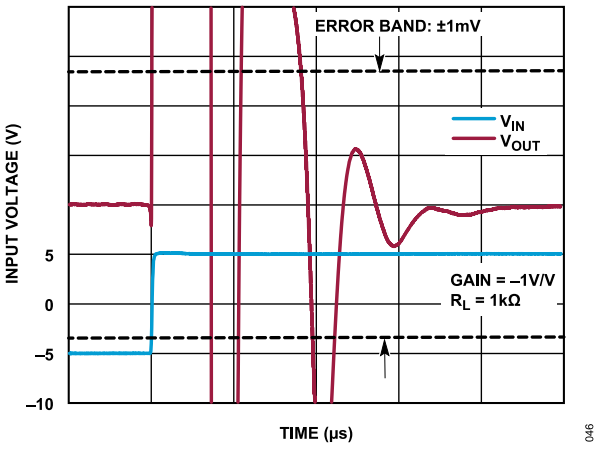

Figure 45. Positive Step Settling Time to 0.01%, V_{OUT} = 10 V

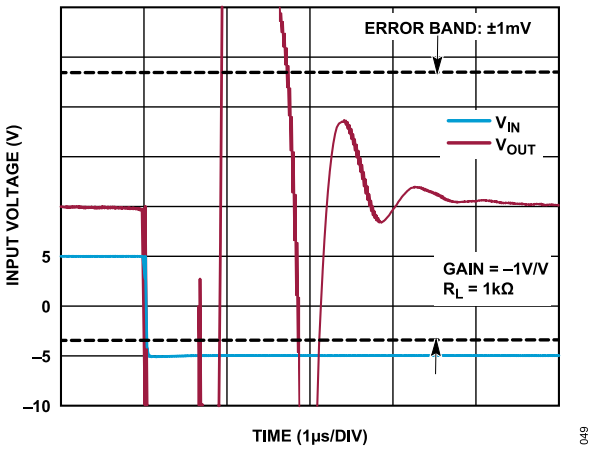

Figure 48. Negative Step Settling Time to 0.01%, V_{OUT} = 10 V

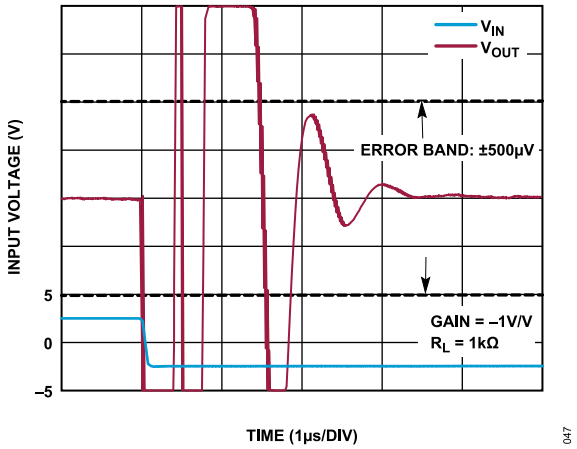

Figure 46. Negative Step Settling Time to 0.01%, V_{OUT} = 5 V

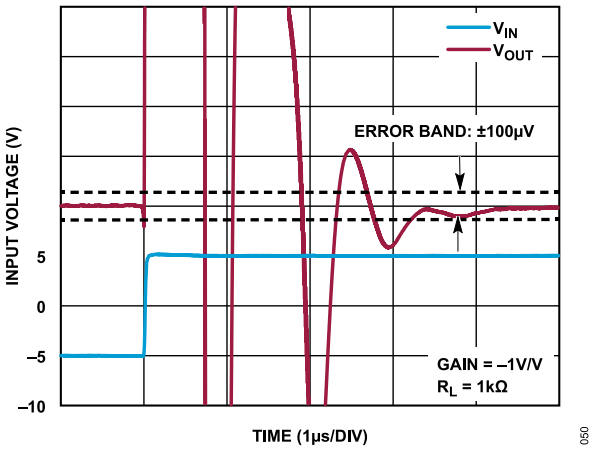

Figure 49. Positive Step Settling Time to 0.001%, V_{OUT} = 10 V

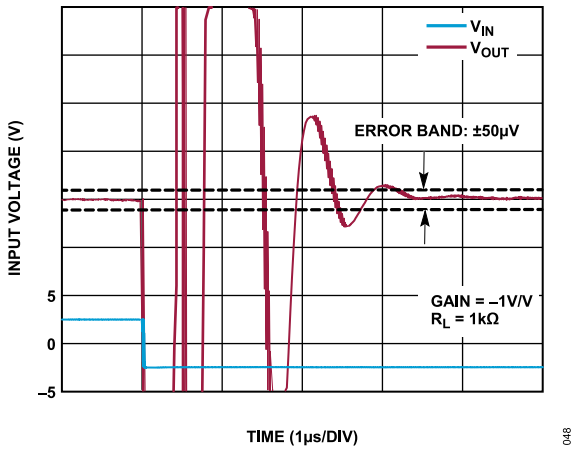

Figure 47. Negative Step Settling Time to 0.001%, V_{OUT} = 5 V

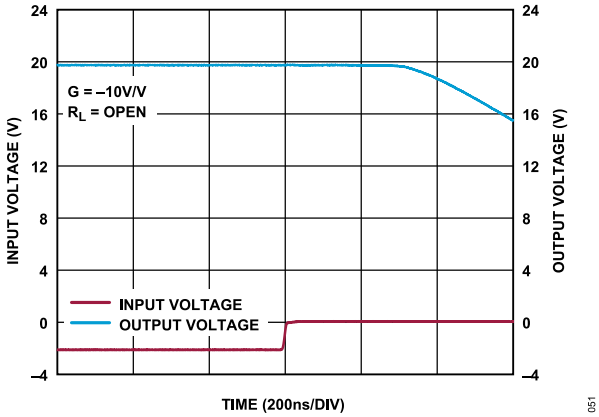

Figure 50. Positive Overload Recovery

TYPICAL PERFORMANCE CHARACTERISTICS

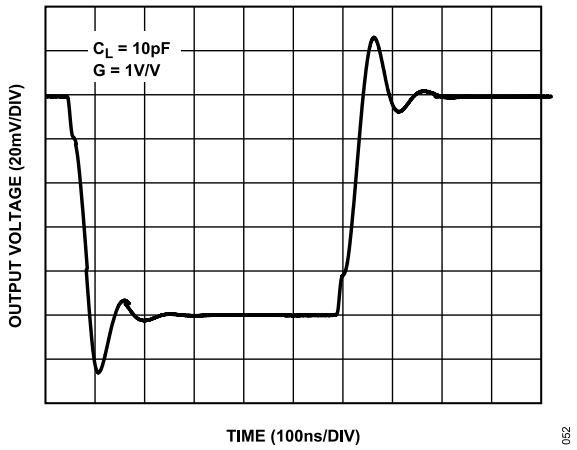

Figure 51. Small Signal Transient Response, G = 1 V/V

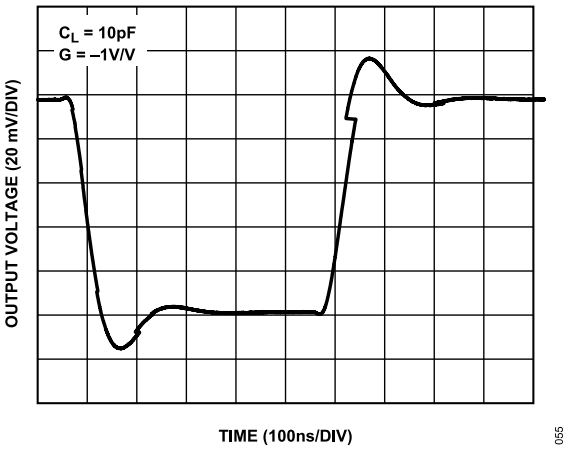

Figure 54. Small Signal Transient Response, G = −1 V/V

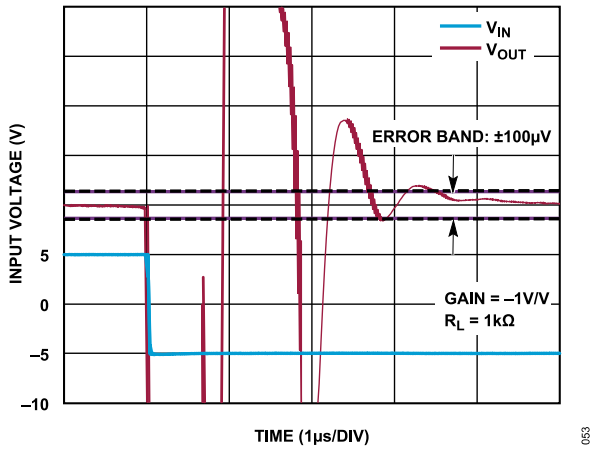

Figure 52. Negative Step Settling Time to 0.001%, V_{OUT} = 10 V

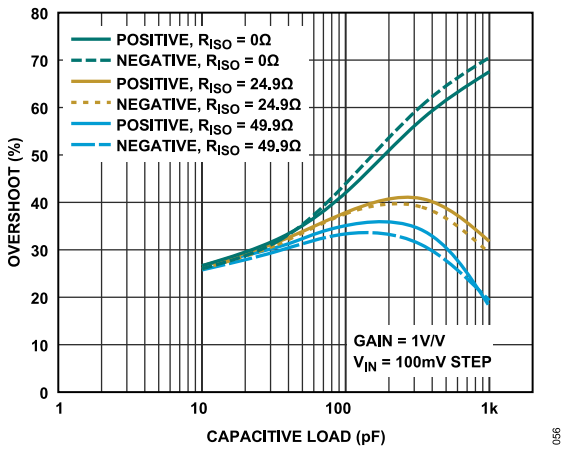

Figure 55. Overshoot vs. Capacitance Load, G = 1 V/V

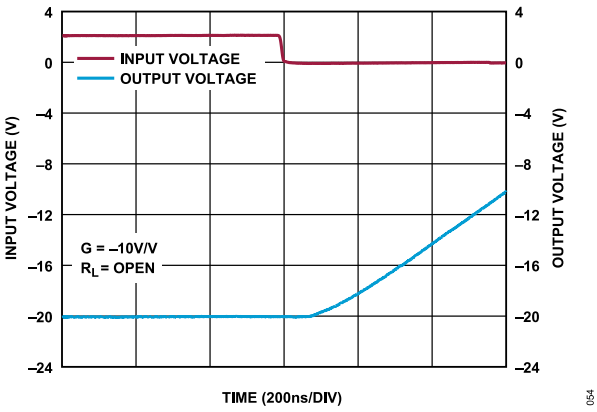

Figure 53. Negative Overload Recovery

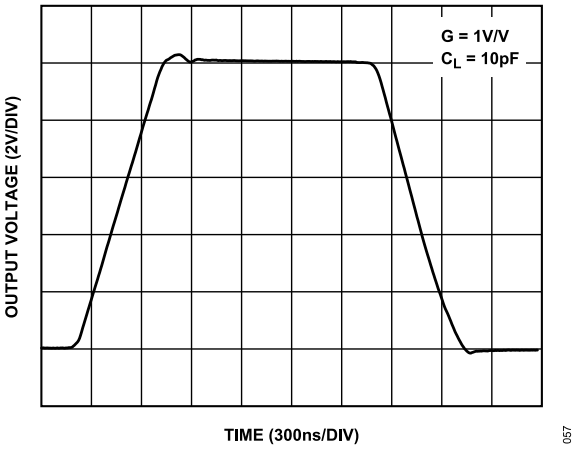

Figure 56. Large Signal Transient Response, G = 1 V/V

TYPICAL PERFORMANCE CHARACTERISTICS

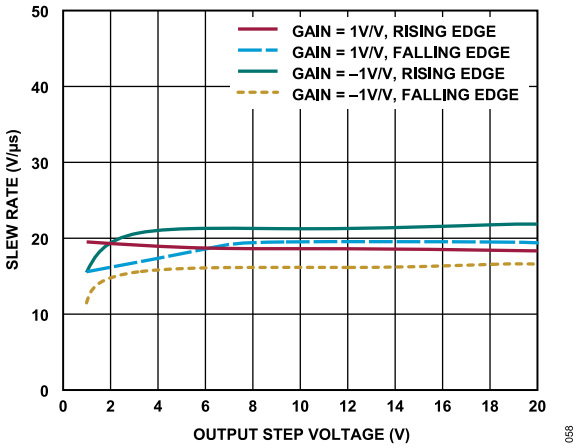

Figure 57. Slew Rate vs. Output Step Voltage

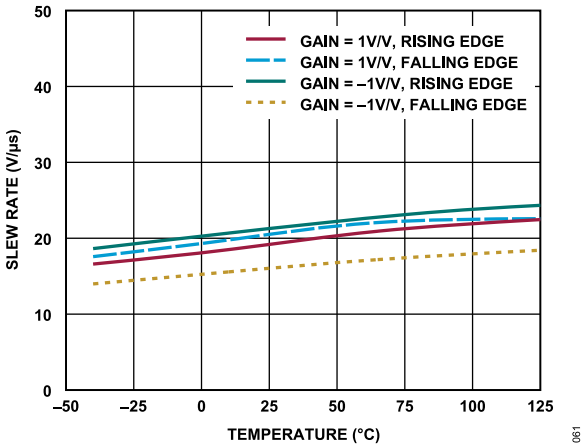

Figure 60. Slew Rate vs. Temperature

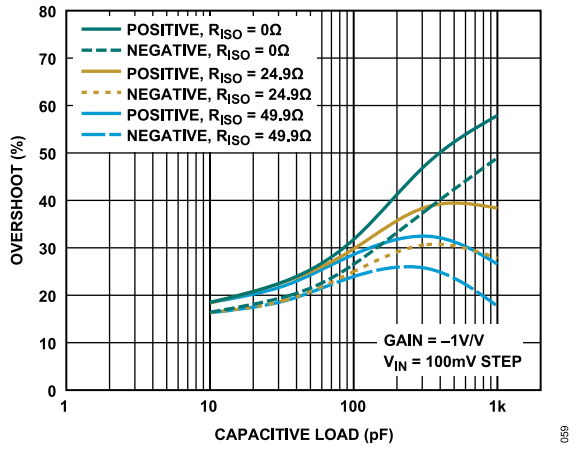

Figure 58. Overshoot vs. Capacitance Load, G = −1 V/V

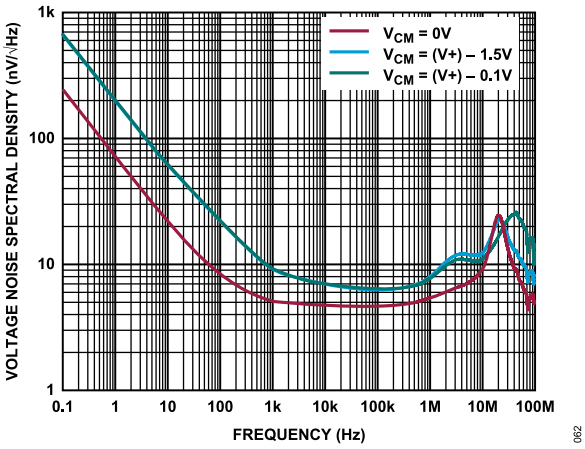

Figure 61. Input Voltage Noise Spectral Density vs. Frequency

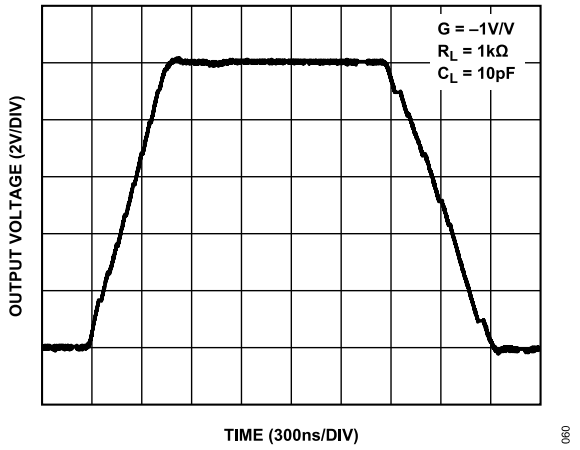

Figure 59. Large Signal Transient Response, G = −1 V/V

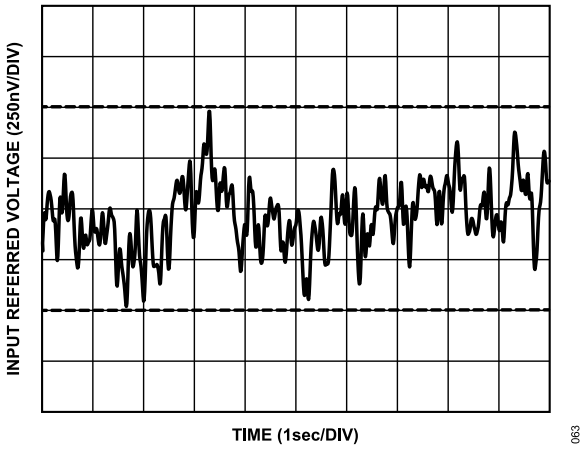

Figure 62. 0.1 Hz to 10 Hz Voltage Noise

TYPICAL PERFORMANCE CHARACTERISTICS

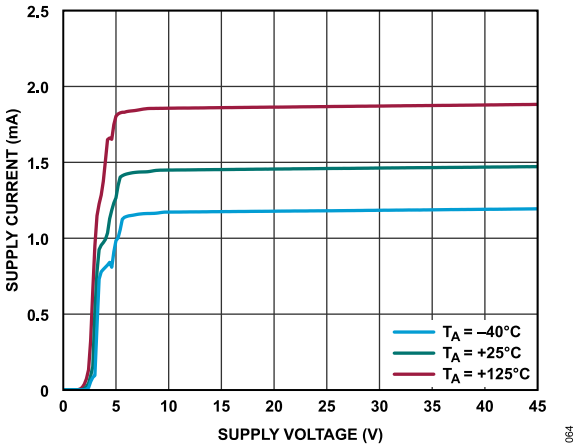

Figure 63. I_S per Amplifier vs. Supply Voltage at Various Temperatures

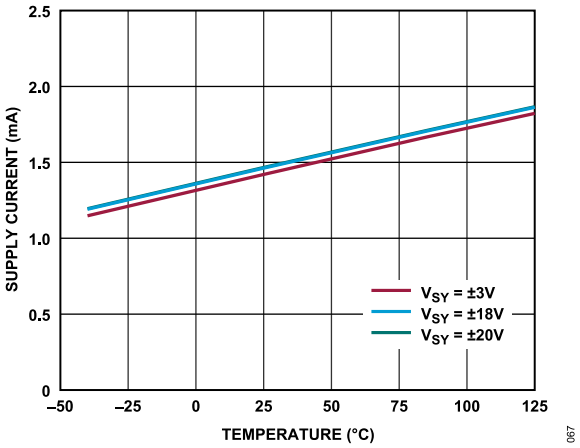

Figure 66. I_S per Amplifier vs. Temperature for Various Supplies

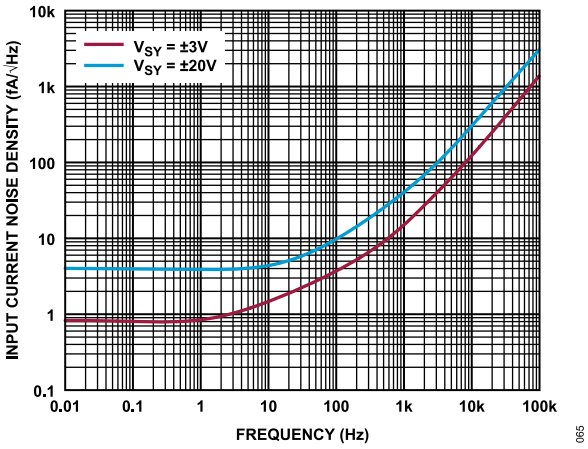

Figure 64. Current Noise Spectral Density vs. Frequency

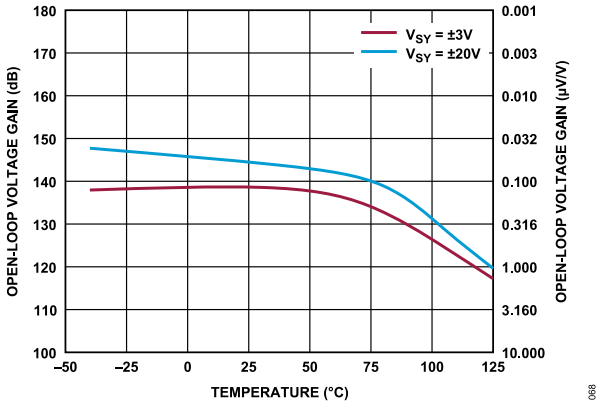

Figure 67. DC Open-Loop Gain vs. Temperature

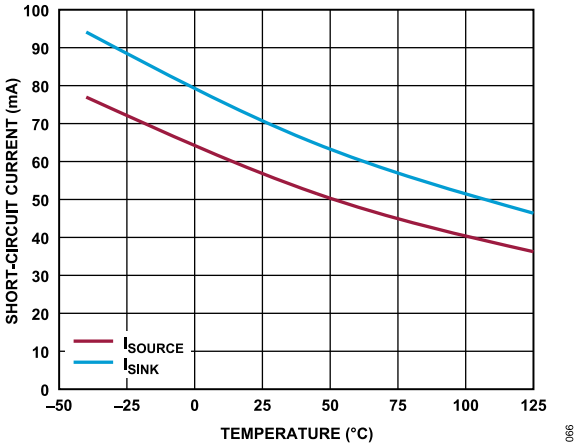

Figure 65. Short-Circuit Output Current vs. Temperature

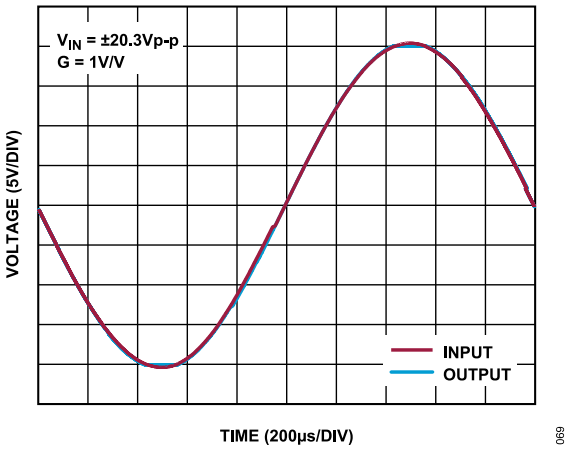

Figure 68. No Phase Reversal

TYPICAL PERFORMANCE CHARACTERISTICS

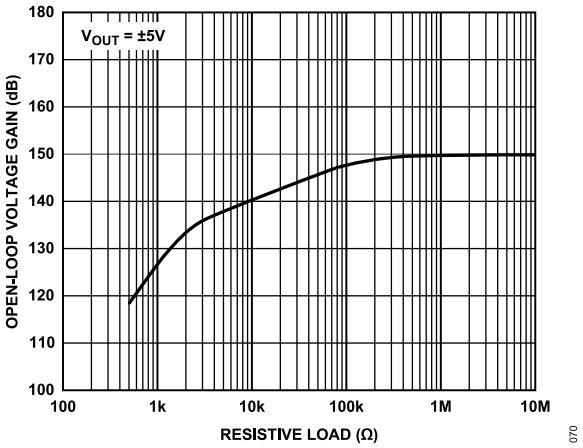

Figure 69. DC Open-Loop Gain vs. R_L

THEORY OF OPERATION

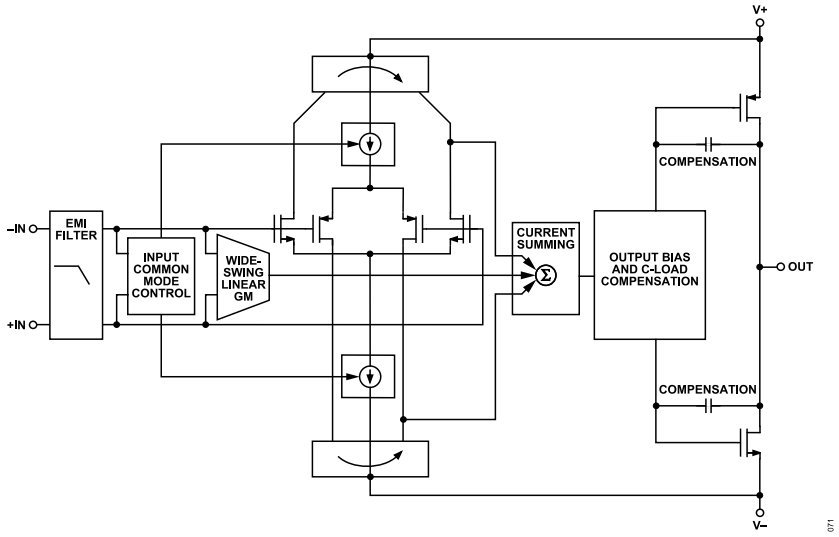

Figure 70. Simplified Schematic

The ADA4511-2 is a dual-channel, low-power, rail-to-rail input and output, precision complementary metal-oxide semiconductor (CMOS) op amp that operates over a wide supply voltage range of 6 V to 40 V.

INPUT AND GAIN STAGES

Figure 70 shows the simplified circuit diagram for the ADA4511-2. The input architecture provides high-impedance, rail-to-rail differential and common-mode input swing, low noise, low-input bias current, and low-offset voltage.

An integrated EMI filter increases the signal robustness and helps prevent EMI signals from coupling into the amplifier. Depending on the input common-mode voltage, either the negative channel metal-oxide semiconductor (NMOS) or the positive channel metal-oxide semiconductor (PMOS) input stage can be active at any time. The low-offset voltage and low-offset voltage drift specifications are possible by trimming both the NMOS and PMOS input stages.

The ADA4511-2 includes circuitry that extends the linear input range, which provides higher slew rates than a traditional input differential pair and improves the THD. The wide gain bandwidth product of 10.4 MHz is achieved through internal Miller compensation.

OUTPUT STAGE

The output of the ADA4511-2 swings rail-to-rail to within 100 mV of either supply rail. A capacitive load compensation block senses the load capacitor and adds additional phase margin, if required, to drive a large capacitor (at least 1 nF) and maintain amplifier stability.

EMI REJECTION

High-frequency EMI is a threat to precision amplifier performance in an intended application. Op amps must accurately amplify input signals despite low signal strength and long transmission lines. All op amp pins are susceptible to EMI signals. These high-frequency signals are coupled into an op amp by various means, such as conduction, near-field radiation, or far-field radiation. For example, wires and PCB traces act as antennas to pick up high-frequency EMI signals.

Op amps do not amplify EMI or RF signals due to the relatively low bandwidth of the amplifier. However, due to the nonlinearities of the input devices, op amps can rectify these out-of-band signals, which then appear as a DC offset at the output.

The ADA4511-2 is designed with integrated EMI filters at the input stage of the op amp. The EMIRR describes the ability of the ADA4511-2 to perform as intended in the presence of electromagnetic energy. The EMIRR is specified for the noninverting pin in Electrical Specifications. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log \times (\Delta V_{IN}\_PEAK / \Delta V_{OS}) \quad (1)$$

The EMIRR performance of the ADA4511-2 is shown in Figure 33.

NO PHASE INVERSION

The ADA4511-2 does not suffer from output voltage phase reversal that occurs in some op amps when the specified input V_{CM} range is exceeded. Output voltage phase reversal causes the output voltage to swing to the opposite rail until the input comes back within the common-mode range. Typically, the inputs of conventional op amps fail to reach or exceed the common-mode limit toward the negative range. Phase-reversal is most often associated with junction field effect transistor (JFET) and/or bipolar field effect transistor (BiFET) amplifiers, but some bipolar single-supply amplifiers are also susceptible phase-reversal. The ADA4511-2 guarantees no phase inversion beyond the entire specified input V_{CM} range all the way to the absolute maximum input voltage limit.

THEORY OF OPERATION

CAPACITIVE LOAD DRIVE CAPABILITY

The ADA4511-2 is stable with any capacitive load up to 1 nF. This is accomplished by dynamically sensing the load-induced output pole and adjusting the compensation at the internal gain node of the amplifier. As the capacitive load increases, the bandwidth decreases. The phase margin may increase or decrease with different capacitive loads, so there may be overshoot in the transient response for some capacitive loads (see Figure 55 and Figure 58). Coaxial cable less than 1 nF can be driven directly, but, for best pulse fidelity, the cable must be properly terminated by placing a resistor of a value equal to the characteristic impedance of the cable (for example 50 Ω) in series with the output. The other end of the cable must be terminated with the same value resistor to ground.

Figure 55 and Figure 58 show the overshoot of the ADA4511-2 with various capacitive loads in unity gain and gain of −1 configurations. To further improve the capacitive load drive of the ADA4511-2, an isolation resistor (R_{ISO}) may be used in series with the output to significantly reduce the overshoot and ringing to stabilize the amplifier.

Table 6. Capacitive Load Drive at Various R_{ISO}

Capacitive Load	100 pF			1000 pF		
R_{ISO}	0 Ω	24.9 Ω	49.9 Ω	0 Ω	24.9 Ω	49.9 Ω
Positive Overshoot Percent	42%	38%	35%	68%	32%	18%
Negative Overshoot Percent	43%	38%	30%	71%	29%	19%

APPLICATIONS INFORMATION

MUX-COMPATIBLE DATA ACQUISITION SYSTEM

Data acquisition in multichannel systems can be accomplished by multiplexing as shown in Figure 71. This technique is very popular in instrumentation, industrial process control, and automated test equipment (ATE), because it reduces the number of components needed to sense multiple sensors, which saves significant power, size, and cost.

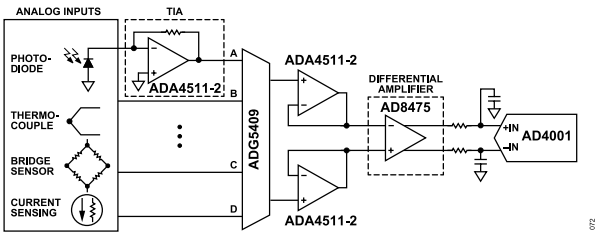

Figure 71. Multiplexed Data Acquisition System

One risk in designing this system is the possibility of exposing the buffer amplifier to a large differential voltage due to the fast switching from a large positive voltage to a large negative voltage by the mux. If the buffer amplifier is not chosen properly, it may experience a large inrush current that can degrade the performance of the system or, worse, permanently damage the part.

The ADA4511-2 solves this problem using a robust mux-compatible architecture that can tolerate large differential voltages up to the supply rails without the use of differential back-to-back diodes. This significantly reduces inrush current, improves settling and distortion performance without experiencing any input loading effect compared to classic op amps with back-to-back diodes, as shown in Figure 72.

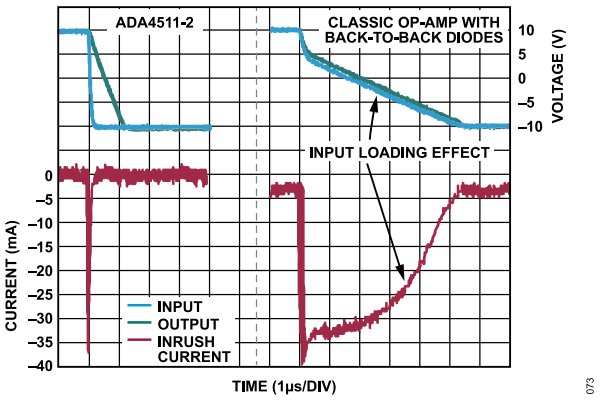

Figure 72. ADA4511-2 Inrush Current Reduction

Design Example

The circuit shown in Figure 73 is a classic multichannel data acquisition signal chain consisting of a mux, amplifiers, and an analog-to-digital converter (ADC). The architecture allows fast sampling of multiple channels using a single ADC, which provides low cost and excellent channel-to-channel matching. Channel-to-channel switching speed is limited by the settling time of the various components following the mux in the signal chain, because the mux can present a full-scale step V_{OUT} to the downstream amplifier and the ADC. The components in this circuit have been specifically chosen to minimize settling time and maximize channel-to-channel switching speed.

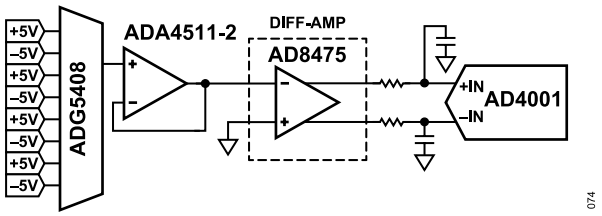

Figure 73. 16-bit, 8-Channel, Single-Ended to Differential, Multiplexed Data Acquisition System

This circuit operates in continuous switching mode. The multiplexer ADG5408 switches continuously with a switching rate that is in sync with the ADC conversion cycle. The signal is buffered by the ADA4511-2 and drives to the AD8475, which attenuates, level shifts, and converts the signal from single-ended to a differential output. An RC filter is used at the input of the ADC to minimize out-of-band noise and attenuate the kickback from the switched capacitor at the ADC input.

To calculate the settling time, the circuit can be divided into parts shown in Figure 74.

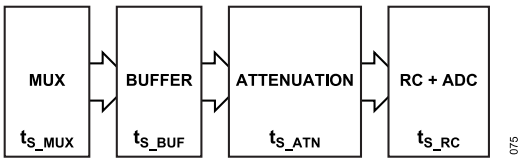

Figure 74. Block Diagram for Settling Time Analysis

The entire settling time is then approximated as the root-sum-square (RSS) of the settling time of each stage.

APPLICATIONS INFORMATION

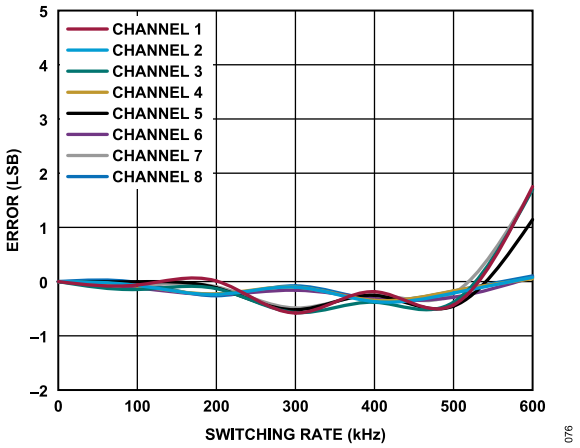

Figure 75. Error (LSB) vs. Switching Rate, 8-Channel 10 V Step

Figure 75 shows the error in least significant bit (LSB) vs. switching rate for an 8-channel 10 V step mux data acquisition system. An LSB error <1 is achieved up to 570 kHz switching rate.

TRANSIMPEDANCE AMPLIFIER

The ADA4511-2 is an excellent choice for low-noise transimpedance amplifier (TIA) applications. The low voltage and current noise of the ADA4511-2 maximize signal-to-noise ratio (SNR), and the low V_{OS} and I_B of the ADA4511-2 minimize the DC error at the amplifier output.

Common applications for current-to-voltage conversion include photodiode circuits where the amplifier converts a current emitted by a diode placed at the negative input terminal into an output voltage. Some photodiode applications include fiber optic controls, motion sensors, and barcode readers. The circuit shown in Figure 76 shows one channel of the ADA4511-2 as a current-to-voltage converter with an electrical model of a photodiode.

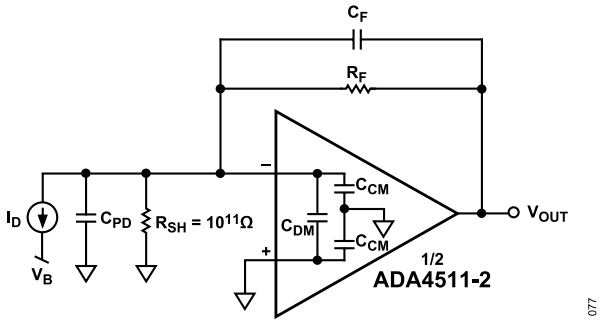

Figure 76. Equivalent TIA Circuit

Photodiodes operate in either photovoltaic mode (zero bias) or photoconductive mode (with an applied reverse-bias across the diode). Mode selection depends on the speed and dark current requirements of the application and the choice of photodiode. In photovoltaic mode, the dark current is at a minimum and is preferred for low-frequency and/or low-light level applications (that is, PN photodiodes). Photoconductive mode is better for applications that require faster and linear responses (that is, PIN photodiodes); however, the trade-offs include increases in dark and noise currents.

The following transfer function describes the transimpedance gain of Figure 76:

$$V_{OUT} = \frac{I_D R_F}{1 + sC_F R_F} \quad (2)$$

where:
V_{OUT} is the required output DC voltage of the op amp.
I_D is the output current of the photodiode.
R_F is the feedback resistor.
C_F is the feedback capacitor.
The parallel combination of R_F and C_F sets the signal bandwidth.
s is the complex frequency variable jω.
j is the imaginary unit.
ω is the angular frequency.

Set R_F such that the maximum attainable V_{OUT} corresponds to the maximum diode I_{OUT}. Because signal levels increase directly with R_F, while the noise due to R_F increases with the square root of the resistor value, which employs the full output swing maximizes the SNR.

It is important to distinguish between the transimpedance gain and the loop gain, because the loop gain characteristics determine the net circuit stability. The closed-loop transfer function takes the form shown in the following equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \quad (3)$$

where:
A is the open loop gain of the amplifier.
β is the feedback network.
$A\beta$ is the loop gain.

In this application, β is given by the following:

$$\beta = \left(\frac{R_{SH}}{R_{SH} + R_F}\right)\frac{1 + sR_F C_F}{1 + s(R_F \parallel R_{SH})(C_{IN} + C_F)} \quad (4)$$

where:
R_{SH} is the diode shunt resistance.
C_{IN} is the total input capacitance consisting of the sum of the diode shunt capacitance (C_{PD}), the input capacitance of the amplifier (C_{DM} + C_{CM}), and the external stray capacitance.

C_{IN}, R_F, C_F, and R_{SH} produce a zero in the 1/β transfer function. The zero frequency (f_Z) is as in the equation that follows:

$$f_Z = \frac{1}{2\pi\,(R_F \parallel R_{SH})(C_{IN} + C_F)} \quad (5)$$

Because the photodiode shunt resistance R_{SH} >> R_F, the circuit behavior is not impacted by the effect of the junction resistance, and f_Z simplifies to the following:

$$f_Z = \frac{1}{2\pi R_F (C_{IN} + C_F)} \quad (6)$$

APPLICATIONS INFORMATION

Figure 77 shows the TIA 1/β curve superimposed upon the open loop gain of the amplifier. For the system to be stable, the 1/β curve must have a slope of less than 20 dB/decade when it intersects with the open loop response. In Figure 77 the dotted line shows an uncompensated 1/β response (C_F = 0 pF) intersecting with the open loop gain at the frequency (f_X) with a slope of 20 dB/decade which indicates an unstable condition.

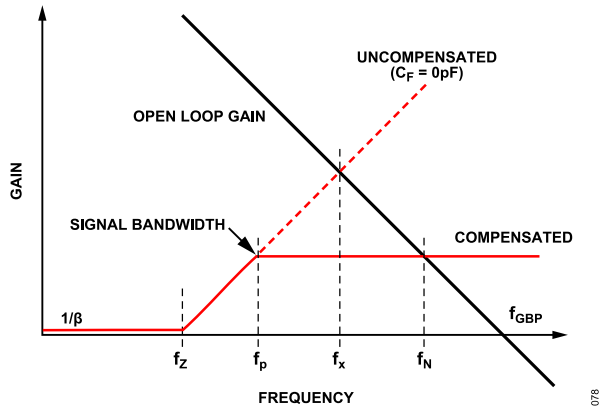

Figure 77. Generalized TIA 1/β and Transfer Function

The instability caused by C_{IN} can be compensated by adding C_F to introduce a pole at a frequency equal to or lower than f_X. The pole frequency is as follows:

$$f_P = \frac{1}{2\pi R_F C_F} \quad (7)$$

Setting the pole at the f_X frequency maximizes the signal bandwidth with a 45° phase margin but is marginal for stability, as indicated by the dashed line. Because f_X is the geometric mean of f_Z and the gain bandwidth product frequency (f_{GBP}) of the amplifier, calculate f_X by the following equation:

$$f_X = \sqrt{f_Z f_{GBP}} \quad (8)$$

Substituting Equation 6 and Equation 7 into Equation 8, the C_F value that produces f_X follows:

$$C_F = \frac{1 + \sqrt{1 + 8\pi R_F C_{IN} f_{GBP}}}{4\pi R_F f_{GBP}} \quad (9)$$

If $8\pi \times R_F \times C_{IN} \times f_{GBP} >> 1$, Equation 9 simplifies to the following:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi R_F f_{GBP}}} \quad (10)$$

Adding C_F also sets the signal bandwidth at f_P. Substitute Equation 10 into Equation 7 and rearrange the equation for the signal bandwidth in terms of f_{GBP}, R_F, and C_{IN} as follows:

$$f_P = \sqrt{\frac{f_{GBP}}{2\pi R_F C_{IN}}} \quad (11)$$

Note that the attainable signal bandwidth is a function of the time constant $R_F C_{IN}$ and the f_{GBP} of the amplifier. To maximize the signal bandwidth, choose an op amp with high bandwidth and low input capacitance, and operate the photodiode in reverse bias to reduce its junction capacitance.

Design Example

As a design example, Figure 78 shows one channel of the ADA4511-2 configured as a TIA amplifier in a photodiode preamp application. Assuming the photodiode has a C_D of 5 pF, an I_D of 2 µA, and the required full-scale V_{OUT} is 100 mV, R_F is 49.9 kΩ according to Equation 2.

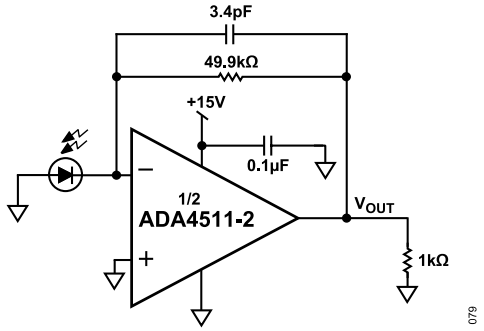

Figure 78. Single-Supply TIA Circuit Using the ADA4511-2

The ADA4511-2 input capacitance (C_{CM} + C_{DM}) is 22 pF, so the total input capacitance (C_{IN}) is 27 pF. By substituting C_{IN} = 27 pF, R_F = 49.9 kΩ, and f_{GBP} = 10 MHz into Equation 9 and Equation 11, the resulting C_F value and the −3 dB signal bandwidth (f_P) are 3.1 pF and 1.1 MHz, respectively.

Figure 79 and Figure 80 show the compensations of the TIA circuit. The system has a bandwidth of 1.1 MHz when it is maximized for a signal bandwidth with C_F = 3.1 pF. Increasing C_F to 5.5 pF reduces the bandwidth to 579 kHz. However, increasing the C_F greatly reduces the overshoot (see Figure 81). In practice, an optimum C_F value is determined experimentally by varying it slightly to optimize the output pulse response.

Use the Analog Devices Analog Photodiode Wizard to design a transimpedance amplifier circuit to interface with a photodiode.

APPLICATIONS INFORMATION

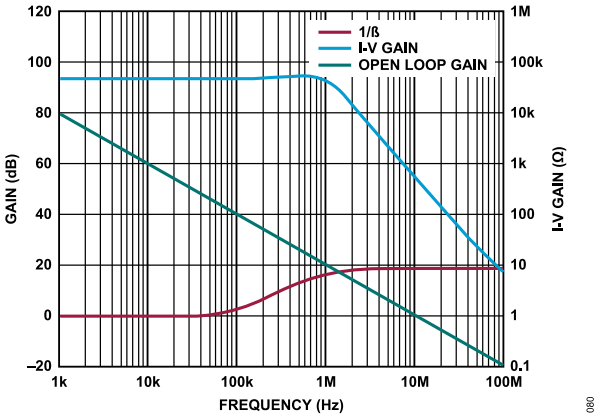

Figure 79. Compensating the TIA, C_F = 3.1 pF

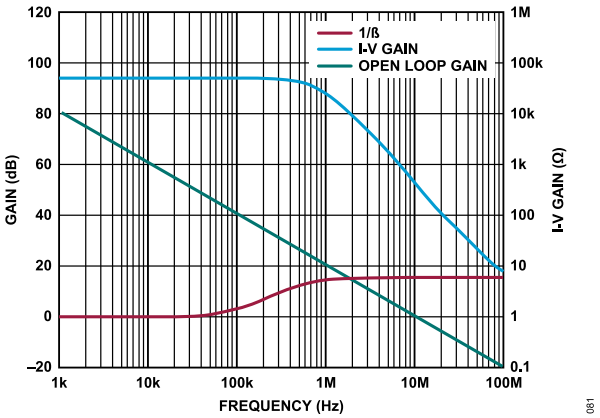

Figure 80. Compensating the TIA, C_F = 5.5 pF

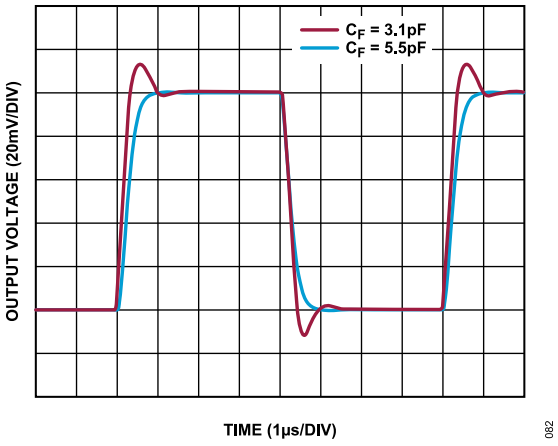

Figure 81. Pulse Response for Various C_F

ACTIVE FILTER

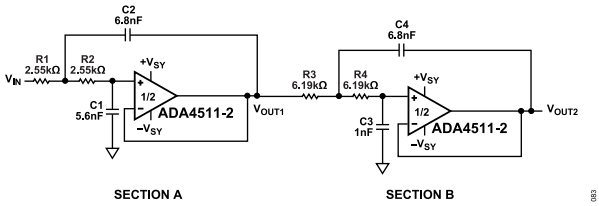

Figure 82. 4-Pole Low-Pass Filter with −3 dB Bandwidth of 10 kHz

Active filters are used to separate signals, passing signals of interest and attenuating signals at unwanted frequencies. For example, low-pass filters are often used as antialiasing filters in data acquisition systems or as noise filters to limit high-frequency noise.

The high-input impedance, high bandwidth, low-input bias current, and DC precision make the ADA4511-2 a good fit for active filter applications. Figure 82 shows the ADA4511-2 in a 4-pole Sallen-Key Butterworth low-pass filter configuration. The 4-pole low-pass filter has two complex conjugate pole pairs and is implemented by cascading two 2-pole low-pass filters. Section A and B are configured as 2-pole low-pass filters in unity gain. Table 7 shows the quality factor (Q) requirement and pole position associated with each stage of the Butterworth filter. For pole locations on the s plane and Q requirements for filters of a different order, refer to the *Chapter 8, Analog Filters*, in the Linear Circuit Design Handbook, available at www.analog.com/AnalogDialogue.

Table 7. Q Requirements and Pole Positions

Section	Poles	Q
A	−0.9239 ± j0.3827	0.5412
B	−0.3827 ± j0.9239	1.3065

The Sallen-Key topology is widely used due to its simple design with few circuit elements. This topology provides the user the flexibility of implementing either a low-pass or a high-pass filter by simply interchanging the resistors and capacitors. The ADA4511-2 is configured in unity gain with a corner frequency at 10 kHz. An active filter requires an op amp with a unity-gain bandwidth that is at least 100 times greater than the product of the corner frequency (f_C) and the Q. The resistors and capacitors are also important in determining the performance over manufacturing tolerances, time, and temperature. At least 1% or better tolerance resistors and 5% or better tolerance capacitors are recommended.

Figure 83 shows the frequency response of the low-pass Sallen-Key filter, where:
V_{OUT1} is the output of the first stage.
V_{OUT2} is the output of the second stage.

V_{OUT1} shows a 40 dB/decade roll-off and V_{OUT2} shows an 80 dB/decade roll-off. The transition band becomes sharper as the order of the filter increases.

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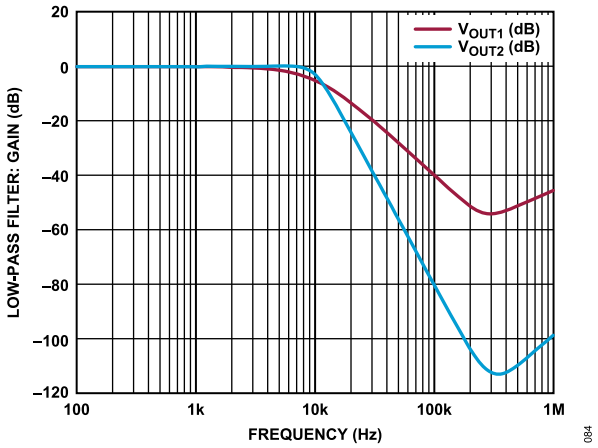

Figure 83. Low-Pass Filter: Gain vs. Frequency

FEEDBACK COMPONENTS

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the resistors and the parasitic capacitance at the inverting input does not degrade stability. If the pole formed is near the required crossover frequency of the amplifier, then it negatively impacts the stability.

In general, if the parasitic pole lies within the closed-loop bandwidth of the amplifier, add a capacitor in parallel with the R_F to introduce a zero that has a frequency close to the frequency of the pole to improve stability.

For a more detailed discussion, refer to the Analog Dialogue article: The Truth About Voltage Feedback Resistors.

PRECISION BUFFER

The overall precision of high-resolution systems with ADCs and digital-to-analog converters (DACs) depends on the accuracy, stability, and drive capability of the voltage reference of the system. Typically, the best performance requires a costly external reference, because on-chip references and buffers often have poor performance or insufficient drive.

With its low-noise specifications, the ADA4511-2 can be used to preserve the accuracy of the chosen reference for successive approximation register (SAR) ADC reference inputs. The Analog Dialogue article: Voltage Reference Design for Precision Successive-Approximation ADCs details several considerations and how to compute for noise from the reference circuit to ensure that ADC performance is not affected.

DAC outputs that drive real world sensors also depend on the accuracy of the reference voltage. The low V_{OS}, $\Delta V_{OS}/\Delta T$, I_B, e_n p-p, and very high linearity, in combination with the fast settling time and slew rate, make the ADA4511-2 an ideal fit for an output DAC buffer.

RECOMMENDED POWER SOLUTION

Analog Devices, Inc., has a wide range of power management products that meet the requirements of most high performance signal chains. For a dual-supply application, the ADA4511-2 may need as high as ±20 V supply. Low dropout (LDO) linear regulators such as the LT3042 for the positive supply and the LT3093 for the negative supply help improve the PSRR at high frequency and generate a low-noise power rail. In addition, if a negative supply is not available, the ADP5070 can generate the negative supply from a positive supply. Table 8 shows the list of the recommended power management devices for the ADA4511-2.

Table 8. Recommended Power Management Devices

Product	Description
ADP5070	DC-to-DC switching regulator with independent positive and negative outputs
LT3032	Dual 150 mA positive/negative low-noise LDO linear regulator
LT3093	−20 V, 200 mA, ultra-low noise, ultra-high PSRR negative linear regulator
LT3042	20 V, 200 mA, ultra-low noise, ultra-high PSRR RF linear regulator

It is recommended to use a low ESR, 0.1 µF bypass capacitor close to each of the power supply pins of the ADA4511-2 and ground to reduce errors coupling in from the power supplies. For noisy power supplies, place an additional 10 µF capacitor in parallel with the 0.1 µF for better performance.

LAYOUT GUIDELINES

The ADA4511-2 has extremely high impedance inputs. Shunt impedances from leakage resistance and parasitic capacitance in the PCB layout can severely degrade the performance of the low bias input. Protect against parasitic leakage currents by using guarding techniques to reduce the voltage gradient seen by the input node. Physically, a guard is a low impedance conductor that surrounds a high impedance node and is driven to the voltage of that node. It serves to buffer leakage by diverting the leakage away from the sensitive node and into the low impedance guard. Remove the solder mask from the guard traces to guard against surface leakage due to contamination. Place any input resistors close to the ADA4511-2 inputs to avoid interaction with trace parasitics. If one of the channels is not in use, connect the input to a voltage that is within the linear range of the channel to avoid overdrive conditions that can interfere with other channels. Leave the output unconnected. Place decoupling capacitors, such as 0.1 µF, near the ADA4511-2. Larger capacitors, such as 10 µF, can be used farther away from the op amp.

OUTLINE DIMENSIONS

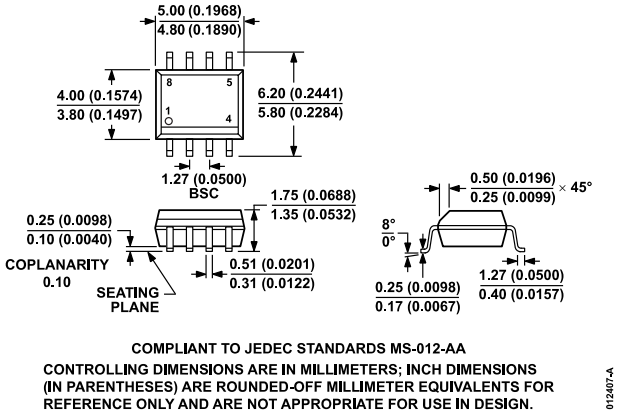

Figure 84. 8-Lead Standard Small-Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions Shown in millimeters and (inches)

Updated: January 24, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADA4511-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]		R-8
ADA4511-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	Reel, 1000	R-8
ADA4511-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	Reel, 2500	R-8

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADA4511-2ARZ	Evaluation Board

[1] Z = RoHS-Compliant Part.