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Campbell (MAXREFDES4#): 16-Bit High-Accuracy 4-20mA Input Isolated Analog Front End (AFE)

Abstract: This document explains how the Campbell (MAXREFDES4#) subsystem reference design meets the higher resolution and isolation needs of industrial control and industrial automation applications. Hardware and firmware design files as well as FFTs and histograms from lab measurements are provided.

Introduction

In industrial control and industrial automation applications, high-resolution data converters are often required. Although today's field programmable gate arrays (FPGAs) and microcontrollers may integrate analog-to-digital converters (ADCs), in many cases, the resolution is not high enough and isolation is lacking.

More detailed image (2MB)

The Campbell (MAXREFDES4#) subsystem reference design is a 16-bit high-accuracy industrial analog front end (AFE) that accepts a 4–20mA current loop or a 0.2V to 4.096V voltage input signal, and features isolated power and data—all integrated into a small form factor. The Campbell design integrates a precision low-noise buffer (MAX44250), a high-accuracy ADC (MAX11100), an ultra-high-precision 4.096V voltage reference (MAX6126), 600V$_{RMS}$ data isolation (MAX14850), and isolated/regulated 5V power rails (MAX256/MAX1659).

This AFE solution can be used in any application that needs high-accuracy analog-to-digital conversion, but it is mainly targeted for industrial sensors, industrial automation, process control, programmable logic controllers (PLCs), and medical applications.
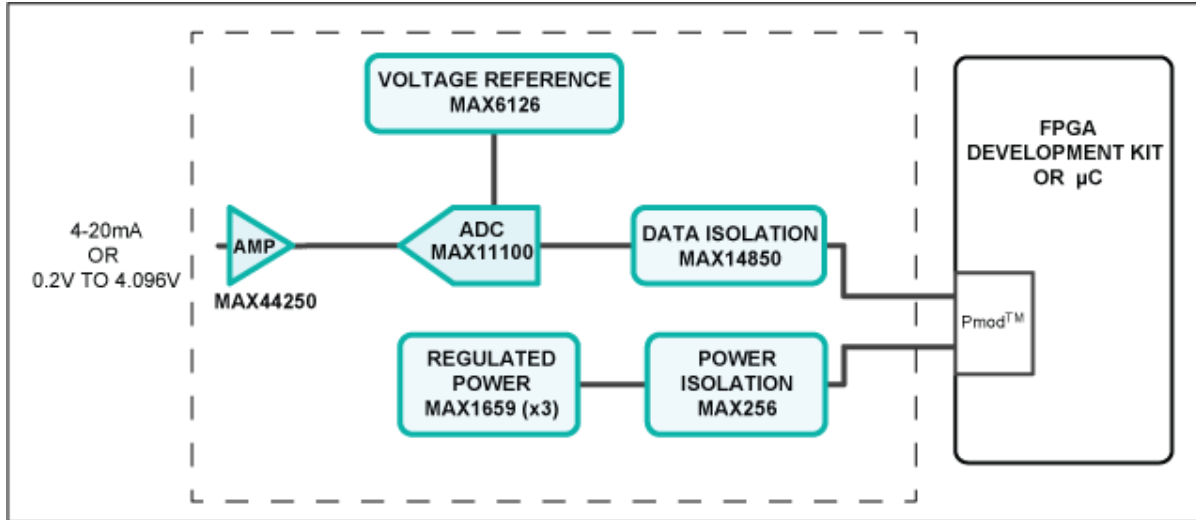
Figure 1. The Campbell subsystem design block diagram.

Features

- High accuracy
- 4–20mA current loop input
- 0.2V to 4.096V input range
- Isolated power and data
- Small printed circuit board (PCB) area
- Device drivers
- Example C source code
- Pmod™-compatible form factor

Applications

- Industrial sensors
- Process control
- Industrial automation
- PLC
- Medical

Detailed Description of Hardware

The Pmod specification allows for both 3.3V and 5V modules as well as various pin assignments. This module is designed only for a supply voltage of 3.3V and uses the SPI pin assignments as illustrated on the right.

The power requirements are shown in **Table 1**. The currently supported platforms and ports are shown in **Table 2**.

Table 1. Power Options for the Campbell Subsystem Reference Design			
Power Type	**Jumper Shunt**	**Input Voltage (V)**	**Input Current (mA, typ)**
On-board isolated power	JU3: 1–2 JU4: 2–3	3.3	72.5
External power	JU3: 2–3 JU4: 1–2	12	10.7
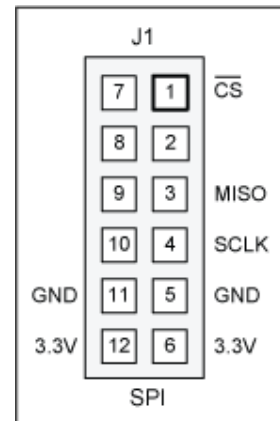
Table 2. Supported Platforms and Ports	
Supported Platforms	**Port**
Nexys™ 3 Platform (Spartan®-6)	JB1
ZedBoard™ platform (Zynq®-7020)	JA1

The Campbell subsystem is best suited for a high-accuracy 4–20mA current loop or a 0.2V to 4.096V input voltage analog-to-digital data acquisition system. The hardware design provides both isolated power (MAX256) and isolated data (MAX14850).

The MAX44250 op amp (U1) input circuit buffers a 4–20mA current-loop sense voltage on a 200Ω load resistor (with JU2 closed) or a 0.2V to 4.096V (with JU2 open) voltage signal.

The MAX11100 (U2) is a 16-bit, successive-approximation register (SAR) ADC with AutoShutdown™ and fast 1.1µs wake-up features. The ADC's reference input is driven by the MAX6126 ultra-high-precision 4.096V voltage reference (U3) with 0.02% initial accuracy and a 3ppm/°C maximum temperature coefficient (tempco).

The MAX256 (U4) provides an isolated, functional insulation class power solution that accepts 3.3V and converts it to 12V using an off-the-shelf TGM-H281NF Halo® transformer with a 1:2.6 primary to secondary turns ratio plus an external on-board voltage-doubler circuit. Post-regulation is accomplished using the MAX1659 low dropout (LDO) regulators (U5 for a 12V output, U6 for an analog 5V output, and U8 for a digital 5V output). Data isolation is accomplished using the MAX14850 (U5) digital data isolator. The combined power and data isolation achieved is 600V$_{RMS}$.

To use the on-board isolated power supplies, move the shunt on jumper JU3 to the 1–2 position and move the shunt on jumper JU4 to the 2–3 position. If power isolation is not required, an external 12V DC power supply can be used. Move the shunt on jumper JU3 to the 2–3 position and move the shunt on jumper JU4 to the 1–2 position. Connect the ground terminal of the external power supply to the GND2 connector. Connect the 12V DC power supply to the EXT_V connector. See Table 1 for the jumper settings and the input current requirements.

Detailed Description of Firmware for Nexys 3 Platform

The Campbell firmware design was initially released for the Nexys 3 development kit and targeted a MicroBlaze™ soft core microcontroller placed inside a Xilinx® Spartan-6 FPGA. Support for additional platforms may be added periodically under Firmware Files in the All Design Files section. The currently supported platforms and ports are shown in Table 2.

The firmware is a working example of how to interface to the hardware, collect samples, and save them to memory. The simple process flow is shown in **Figure 2a**. The firmware is written in C using the Xilinx SDK tool, which is based on the Eclipse™ open source standard. Custom Campbell-specific design functions were created utilizing the standard Xilinx XSpi core version 3.03a. The SPI clock frequency is set to 3.125MHz.
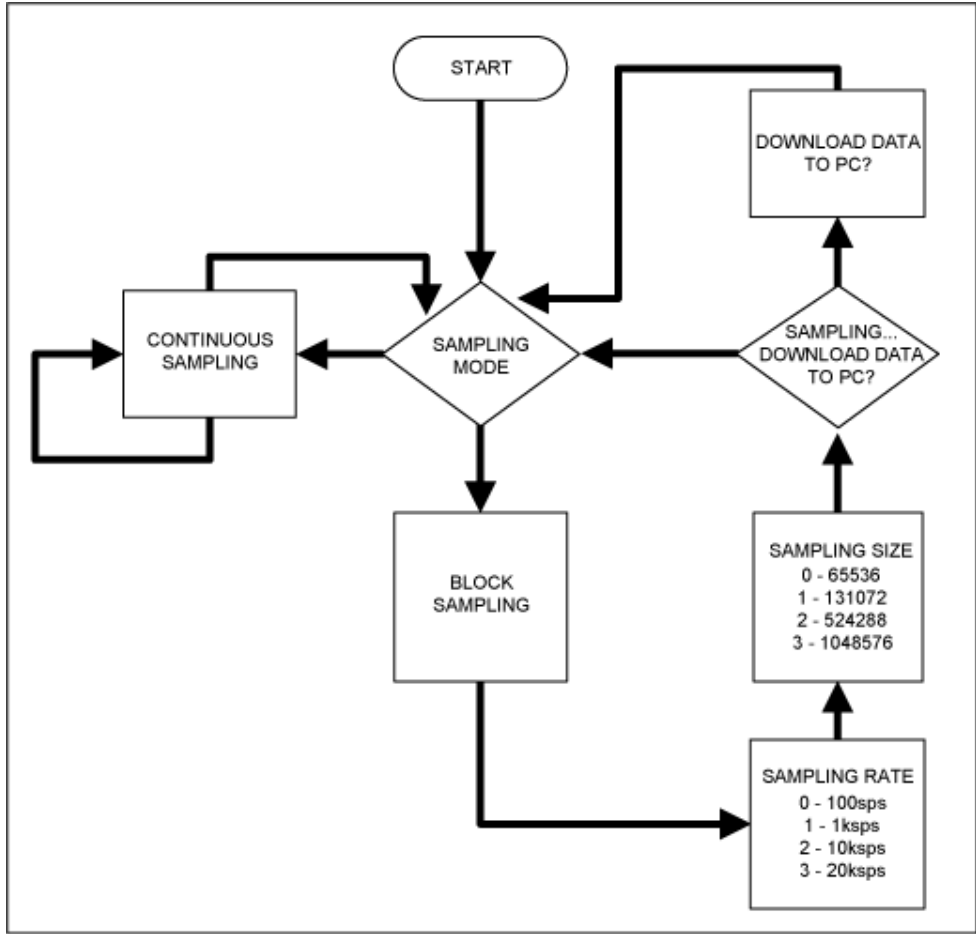
Figure 2a. The Campbell firmware flowchart for Nexys 3 Platform.

The firmware accepts commands, writes status, and is capable of downloading blocks of sampled data to a standard terminal program via a virtual COM port. The complete source code is provided to speed up customer development. Code documentation can be found in the corresponding firmware platform files.

Detailed Description of Firmware for ZedBoard Platform

The Campbell firmware design is also developed and tested for the ZedBoard kit and targets an ARM® Cortex® -A9 processor placed inside a Xilinx Zynq system-on-chip (SoC).

An AXI MAX11100 custom IP core is created for this reference design to optimize the sampling rate and SPI timing stability.

The firmware is a working example of how to interface to the hardware, collect samples, and save them to memory. The simple process flow is shown in **Figure 2b**. The firmware is written in C using the Xilinx SDK tool, which is based on the Eclipse open source standard. Custom Campbell-specific design functions were created utilizing the AXI MAX11100 custom IP core. The SPI clock frequency is set to 4.54MHz when a 189.4ksps sampling rate is selected. The SPI clock frequency is set to 2.5MHz for all other sampling rate.
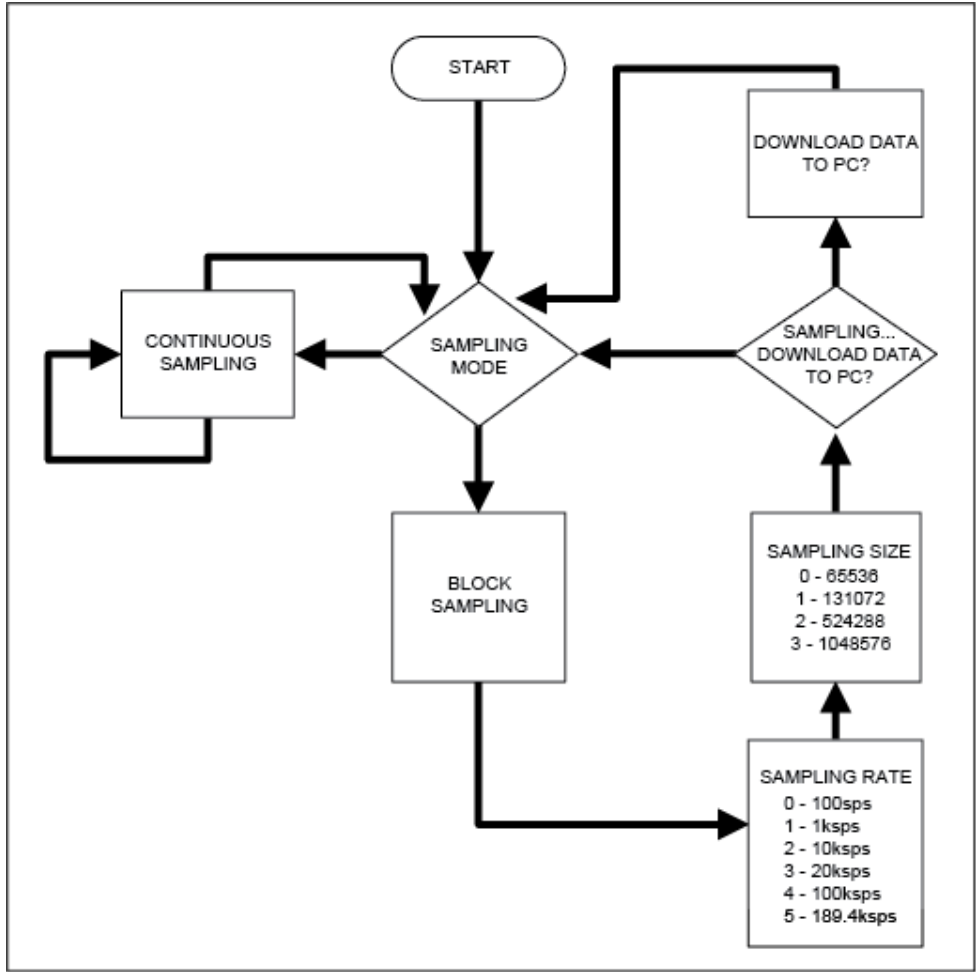
Figure 2b. The Campbell firmware flowchart for ZedBoard platform.

The firmware accepts commands, writes statuses, and is capable of downloading blocks of sampled data to a standard terminal program via a virtual COM port. The complete source code is provided to speed up customer development. Code documentation can be found in the corresponding firmware platform files.

Quick Start

Required equipment:

- Windows® PC with two USB ports
- Campbell (MAXREFDES4#) board
- Campbell-supported platform (i.e., Nexys 3 development kit or ZedBoard kit)
- 4–20mA current loop sensor or other signal source

Download, read, and carefully follow each step in the appropriate Campbell Quick Start Guide:

Campbell (MAXREFDES4#) Nexys 3 Quick Start Guide.

Campbell (MAXREFDES4#) ZedBoard Quick Start Guide.

Lab Measurements

Equipment used:

- Audio Precision® SYS-2722 signal source or equivalent
- Voltage calibrator DVC-8500
- Windows PC with two USB ports
- Campbell (MAXREFDES4#) board
- Nexys 3 development kit
- 12V DC power supply (for external power testing only)

Special care must be taken and the proper equipment must be used when testing the Campbell design. The key to testing any high-accuracy design is to use sources and measurement equipment that are of higher accuracy than the design under test. A low distortion signal source is absolutely required in order to duplicate the results presented below. The input signal was generated using the Audio Precision SYS-2722. The FFTs were created using the FFT control in SignalLab from Mitov Software.

AC and DC performance for on-board isolated power is shown in **Figure 3** and **Figure 4**. AC and DC performance for external power is shown in **Figure 5** and **Figure 6**.
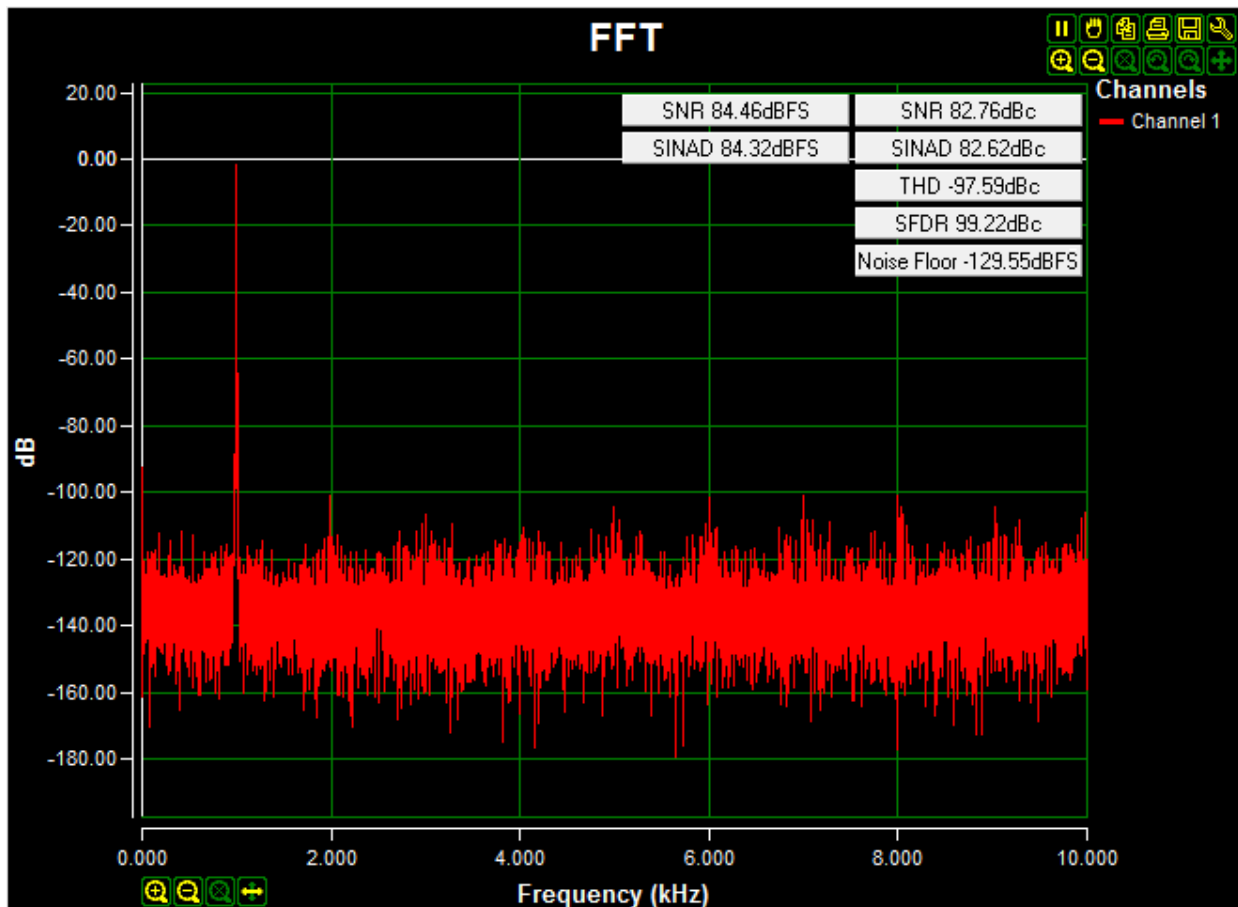

Figure 3. AC FFT using on-board isolated power, a 0.2V to 4.08V 1kHz sine wave input signal, high-impedance input, a 20ksps sample rate, and a Blackman-Harris window.
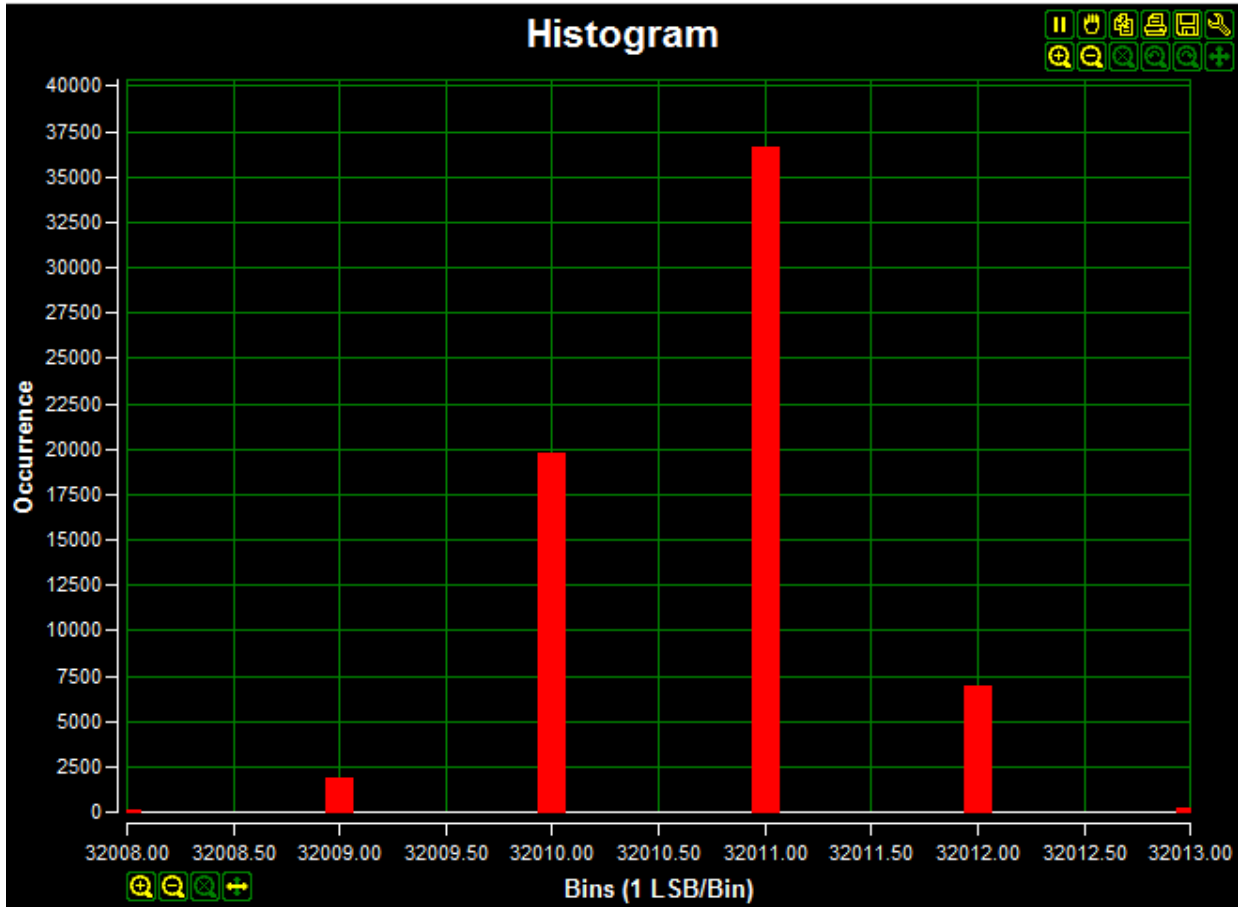
Figure 4. DC histogram using on-board isolated power; a 2.0V input signal; high-impedance input; a 20ksps sample rate; 65,536 samples; a code spread of 6 LSBs with 96.57% of the codes falling within the three center LSBs; and a standard deviation of 0.702.
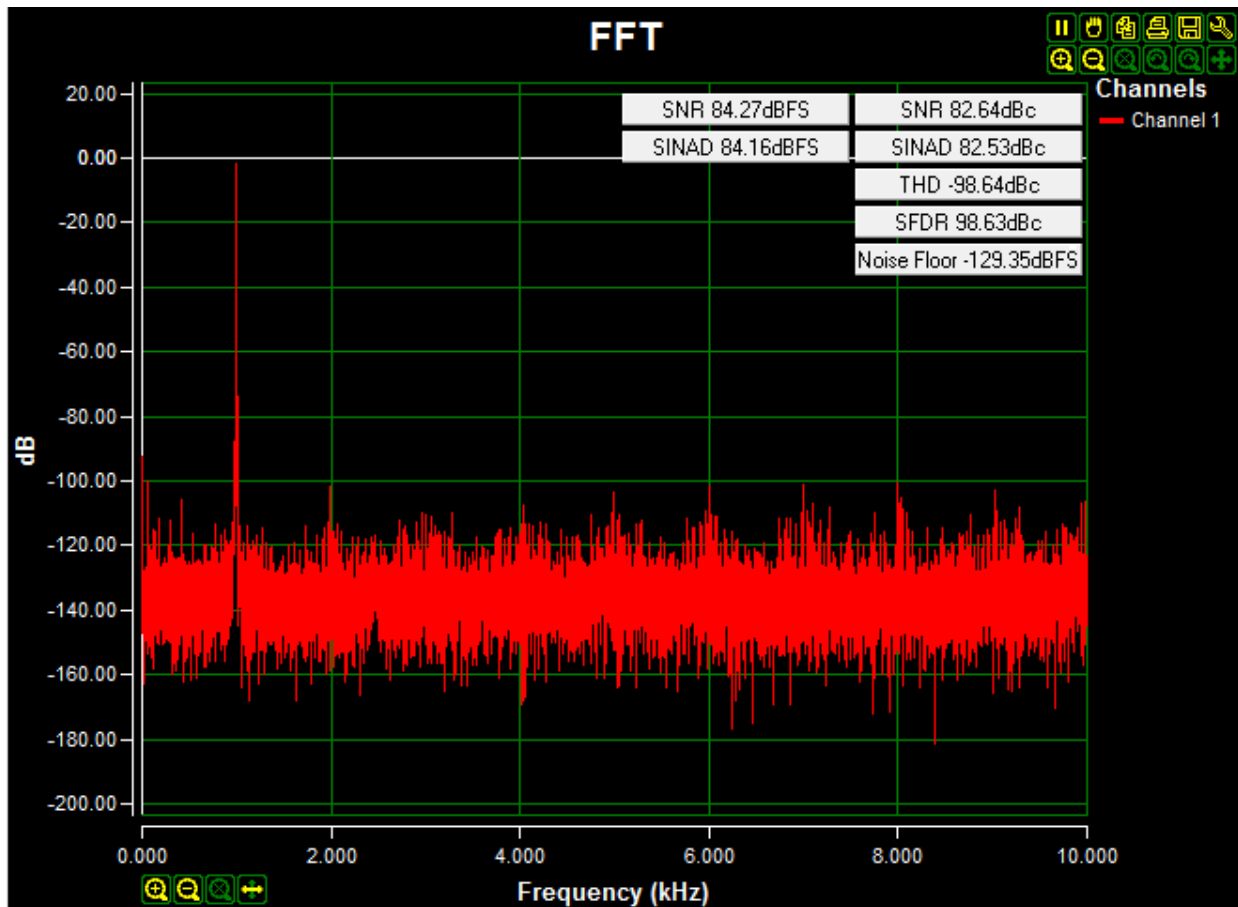
Figure 5. AC FFT using external power, a 0.2V to 4.08V 1kHz sine wave input signal, high-impedance input, a 20ksps sample rate, and a Blackman-Harris window.
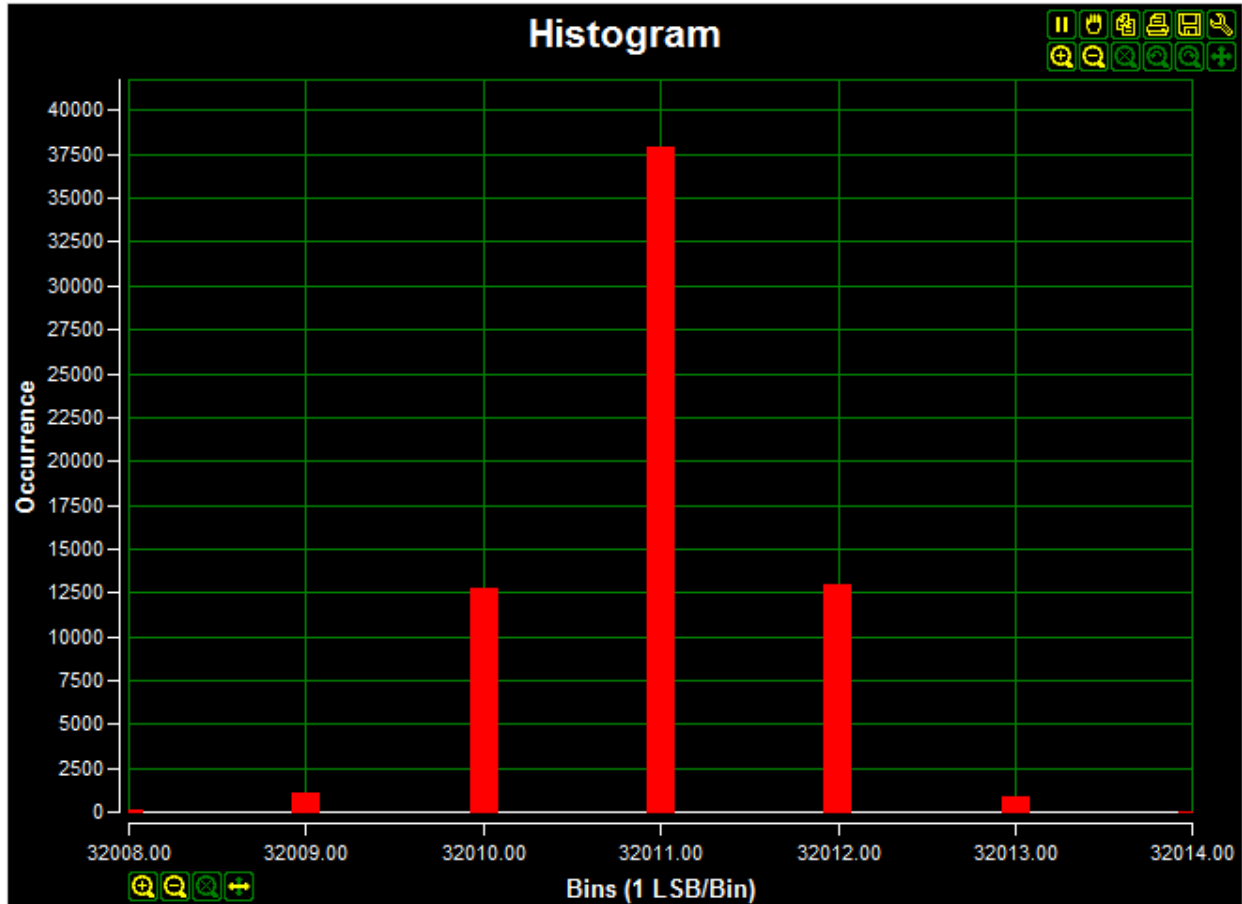
Figure 6. DC histogram using external power; a 2.0V input signal; high-impedance input; a 20ksps sample rate; 65,536 samples; a code spread of 7 LSBs with 96.94% of the codes falling within the three center LSBs; and a standard deviation of 0.721.

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