Data Sheet

ADL8105

GaAs, pHEMT, MMIC, Low Noise Amplifier, 5 GHz to 20 GHz

FEATURES

- Single positive supply (self biased)
- Gain: 27 dB typical at 12 GHz to 17 GHz
- OP1dB: 18 dB typical at 12 GHz to 17 GHz
- OIP3: 30.5 dBm typical at 12 to GHz to 17 GHz
- Noise figure: 1.8 dB typical at 12 GHz to 17 GHz
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Telecommunications
- Satellite communications
- Military radar
- Weather radar
- Electronic warfare
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

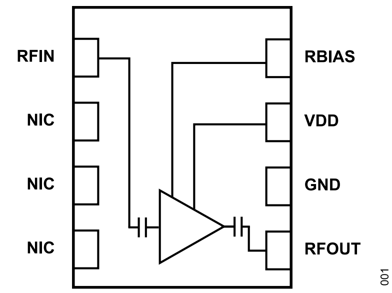

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADL8105 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 5 GHz to 20 GHz.

The ADL8105 provides a typical gain of 27 dB at 12 GHz to 17 GHz, a 1.8 dB typical noise figure from 12 GHz to 17 GHz, a typical output third-order intercept (OIP3) of 30.5 dBm at 12 GHz to 17 GHz, and a saturated output power (P_{SAT}) of up to 20.5 dBm, requiring only 90 mA from a 5 V supply voltage. The power dissipation can be lowered at the expense of OIP3 and output power (P_{OUT}). The ADL8105 also features inputs and outputs that are internally matched to 50 Ω. The RFIN and RFOUT pins are internally ac-coupled, and the bias inductor is also integrated, making it ideal for surface-mounted technology (SMT)-based, high capacity microwave radio applications.

The ADL8105 is housed in an RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP package.

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REVISION HISTORY

7/2023—Rev. 0 to Rev. A

Changes to Figure 69 and Figure 72 17

7/2022—Revision 0: Initial Version

SPECIFICATIONS

5 GHZ TO 12 GHZ

Supply voltage (V_{DD}) = 5 V, quiescent current (I_{DQ}) = 90 mA, bias resistance (R_{BIAS}) = 392 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	5		12	GHz	
GAIN (S21)	27	29		dB	
Gain Variation over Temperature		0.04		dB/°C	
NOISE FIGURE		1.75		dB	
RETURN LOSS					
Input (S11)		13.5		dB	
Output (S22)		13.5		dB	
OUTPUT					
Power for 1 dB Compression (P1dB)	17	19		dBm	
Saturated Output Power (P_{SAT})		20.5		dBm	
IP3		30		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
Second-Order Intercept (IP2)		32		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
POWER ADDED EFFICIENCY (PAE)		21		%	Measured at P_{SAT}

12 GHZ TO 17 GHZ

V_{DD} = 5 V, I_{DQ}= 90 mA, R_{BIAS} = 392 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	12		17	GHz	
S21	24.5	27		dB	
Gain Variation over Temperature		0.033		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
S11		16		dB	
S22		13		dB	
OUTPUT					
P1dB	15.4	18		dBm	
P_{SAT}		20.5		dBm	
IP3		30.5		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
IP2		50		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		19		%	Measured at P_{SAT}

SPECIFICATIONS

17 GHZ TO 20 GHZ

V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	17		20	GHz	
S21	24.5	26.5		dB	
Gain Variation over Temperature		0.037		dB/°C	
NOISE FIGURE		2		dB	
RETURN LOSS					
S11		16.5		dB	
S22		10.5		dB	
OUTPUT					
P1dB	11.5	15		dBm	
P_{SAT}		18		dBm	
IP3		28		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
IP2		62		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		11.5		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		90		mA
Amplifier Current (I_{DQ_AMP})		85		mA
R_{BIAS} Current(I_{RBIAS})		5		mA
SUPPLY VOLTAGE				
V_{DD}	3	5	5.5	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	6 V
RF Input (RFIN) Power	23 dBm
Pulsed RFIN Power (Duty Cycle = 10%, Pulse Width = 100 µs)	25 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 12.6 mW/°C Above 85°C)	1.14 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Nominal Junction (T_{CASE} = 85°C, V_{DD} = 5 V, I_{DQ} = 90 mA, Input Power (P_{IN}) = Off)	120.6°C
Maximum Junction	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	65.6	°C/W
Worst Case[1], T_{CASE} = 85°C	79.1	°C/W

[1] Worst case across all specified operating conditions

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

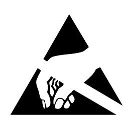
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8105

Table 7. ADL8105, 8-Lead LFCSP

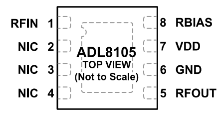
ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. THE NIC PINS ARE NOT CONNECTED INTERNALLY. FOR NORMAL OPERATION, CONNECT THE NIC PINS TO A GROUND PLANE THAT HAS LOW ELECTRICAL AND THERMAL IMPEDANCE.
2. EXPOSED PADDLE. CONNECT THE EXPOSED PADDLE TO A GROUND PLANE THAT HAS LOW ELECTRICAL AND THERMAL IMPEDANCE.

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Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
2, 3, 4	NIC	No Internal Connection. The NIC pins are not connected internally. For normal operation, connect the NIC pins to a ground plane that has low electrical and thermal impedance.
5	RFOUT	RF Output. The RFOUT pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
6	GND	Ground. Connect the GND pin to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
7	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 4 for the interface schematic.
8	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set I_{DQ}. See Table 9 and Figure 74 for more details. See Figure 3 for the interface schematic.
	EXPOSED PADDLE	Exposed Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

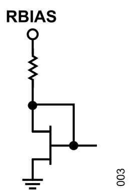

Figure 3. RBIAS Interface Schematic

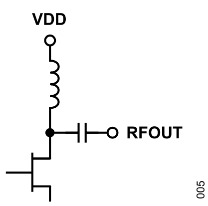

Figure 4. VDD and RFOUT Interface Schematic

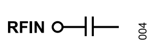

Figure 5. RFIN Interface Schematic

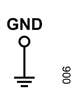

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

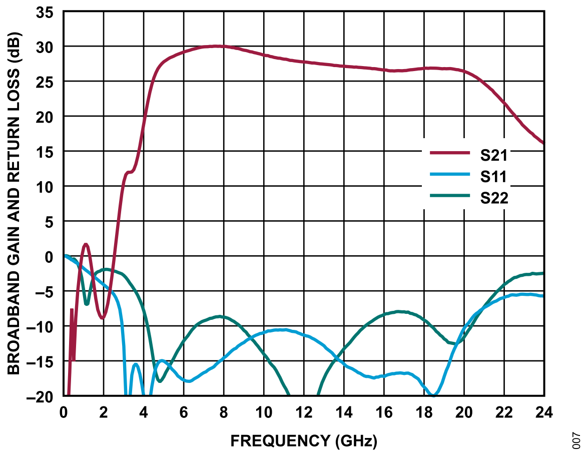

Figure 7. Broadband Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 90 mA

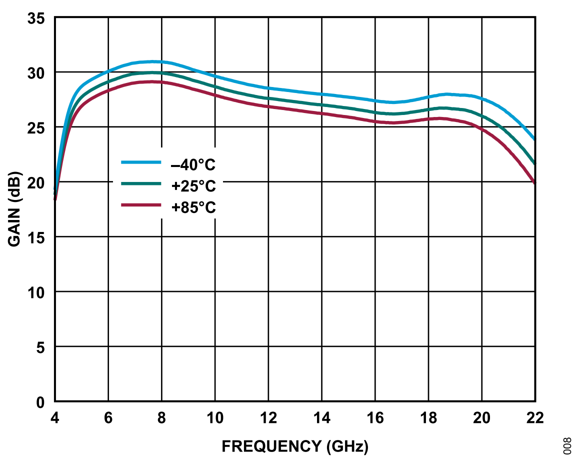

Figure 8. Gain vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

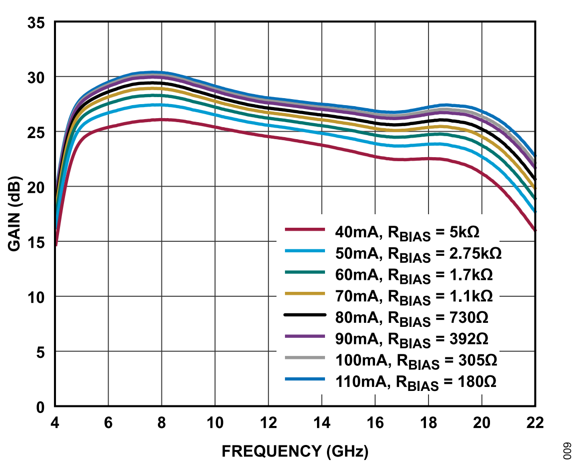

Figure 9. Gain vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

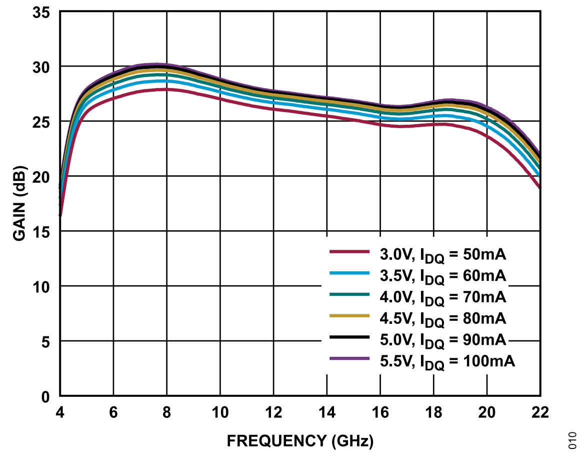

Figure 10. Gain vs. Frequency for Various Supply Voltages and I_{DQ}, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

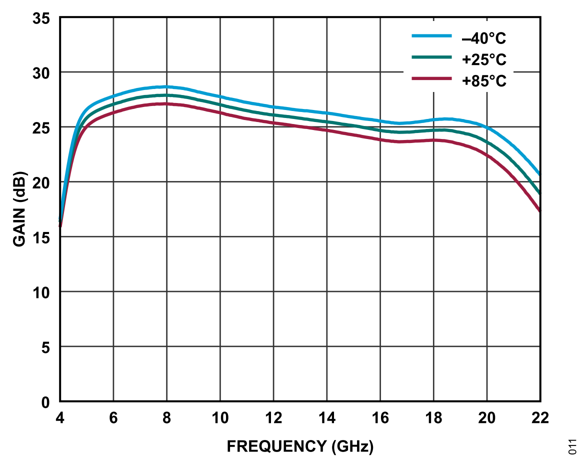

Figure 11. Gain vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

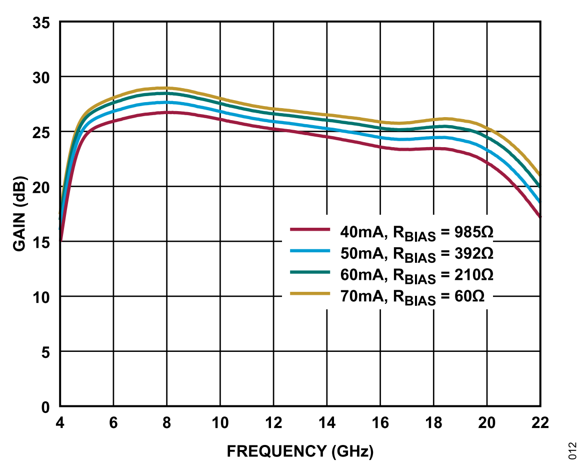

Figure 12. Gain vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

TYPICAL PERFORMANCE CHARACTERISTICS

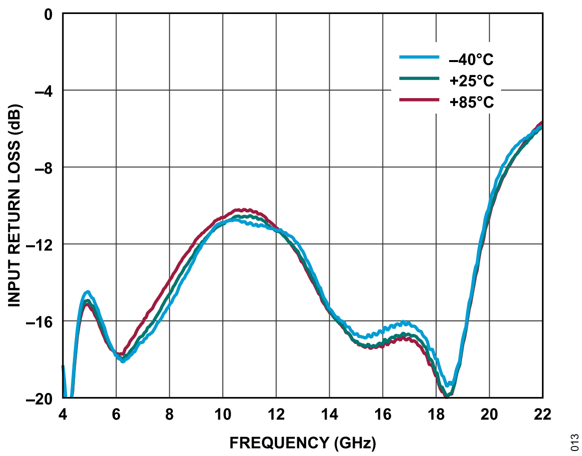

Figure 13. Input Return Loss vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

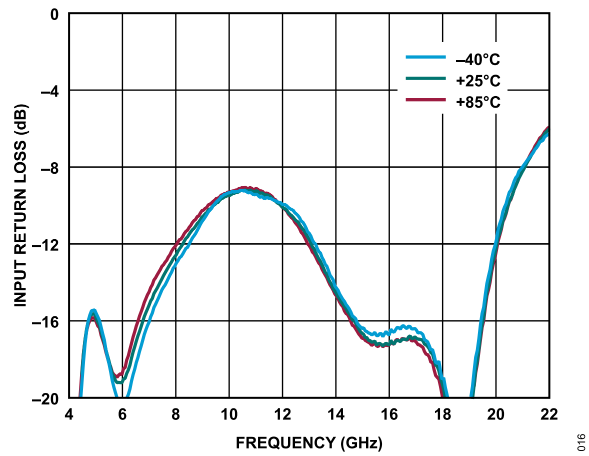

Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

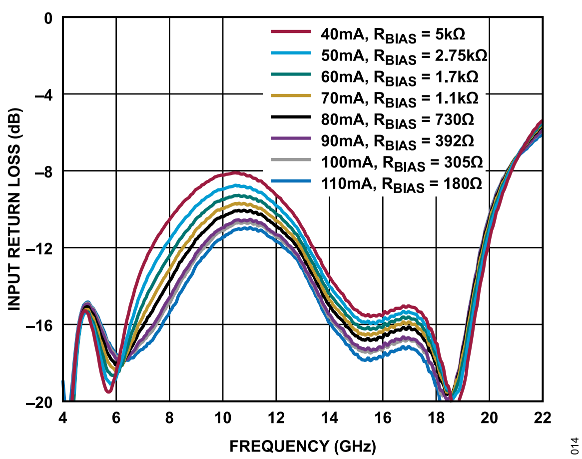

Figure 14. Input Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

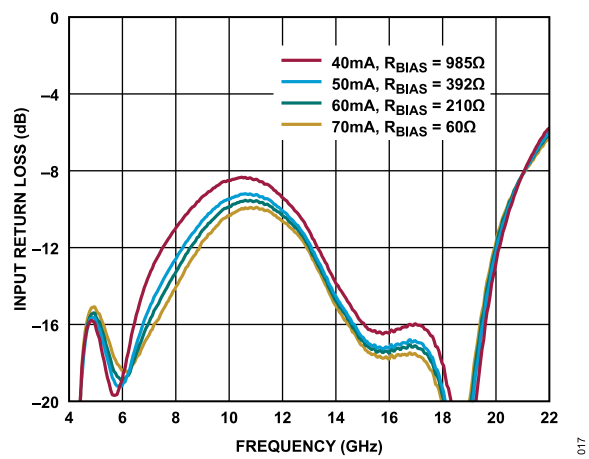

Figure 17. Input Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

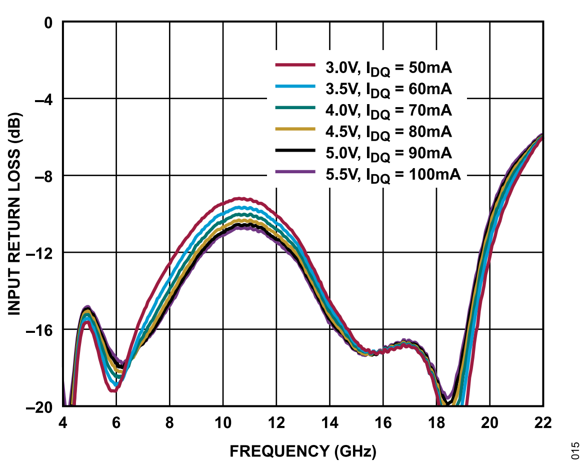

Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

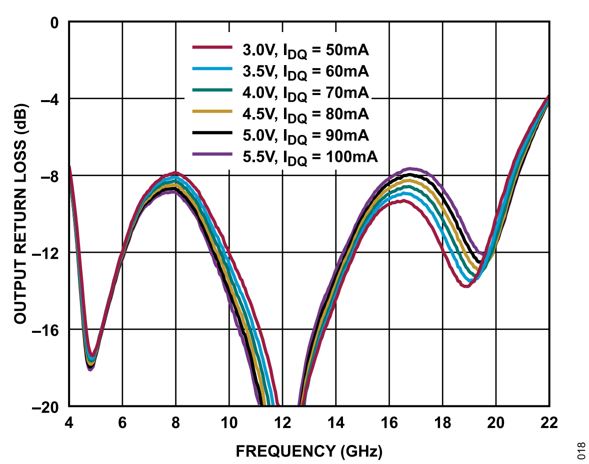

Figure 18. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

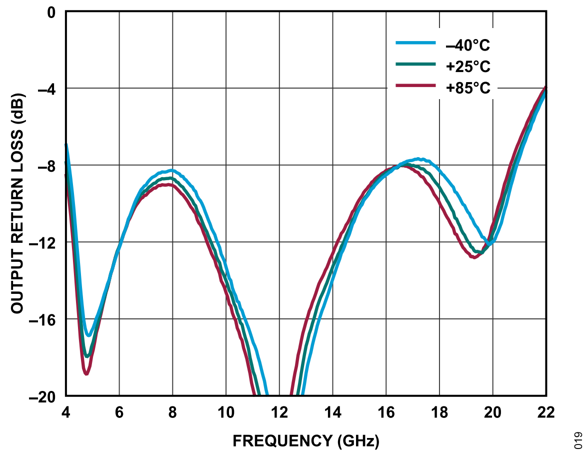

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

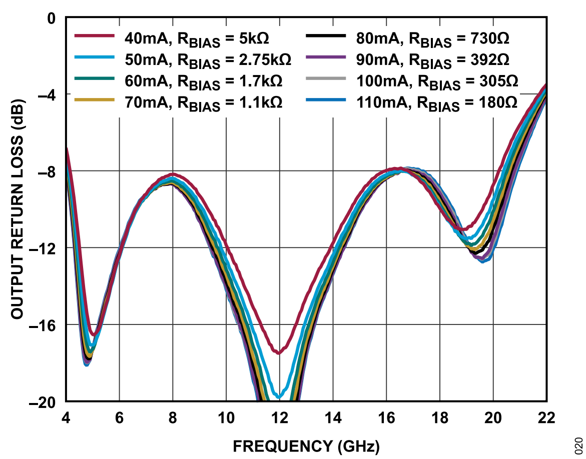

Figure 20. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

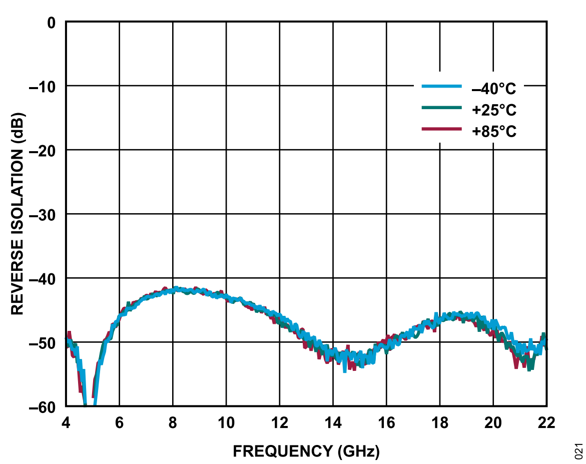

Figure 21. Reverse Isolation vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

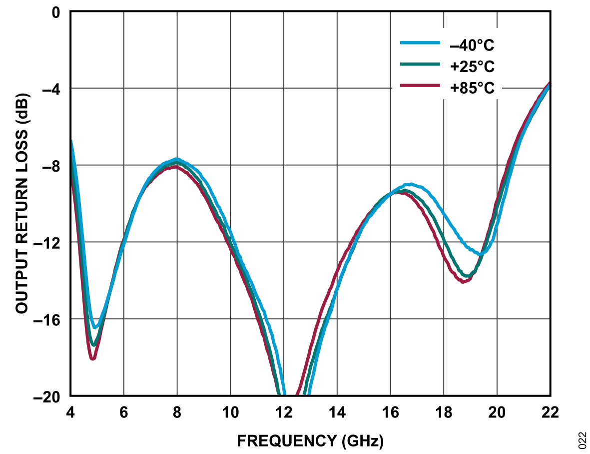

Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

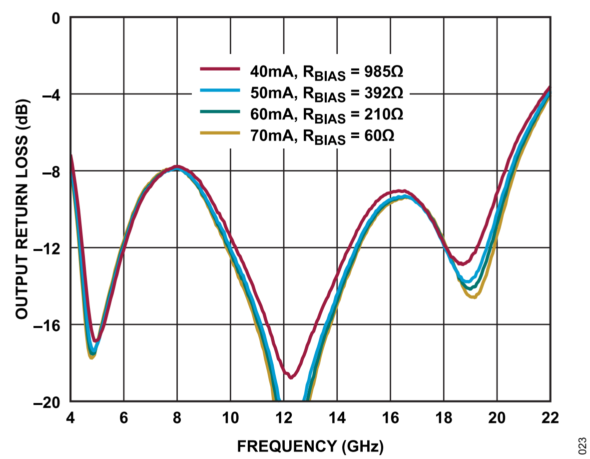

Figure 23. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

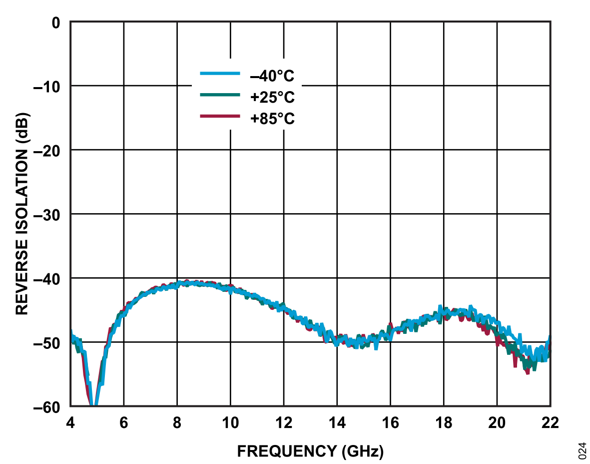

Figure 24. Reverse Isolation vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

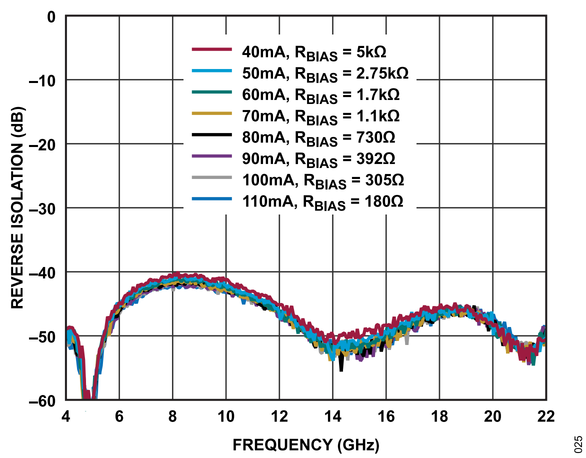

Figure 25. Reverse Isolation vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

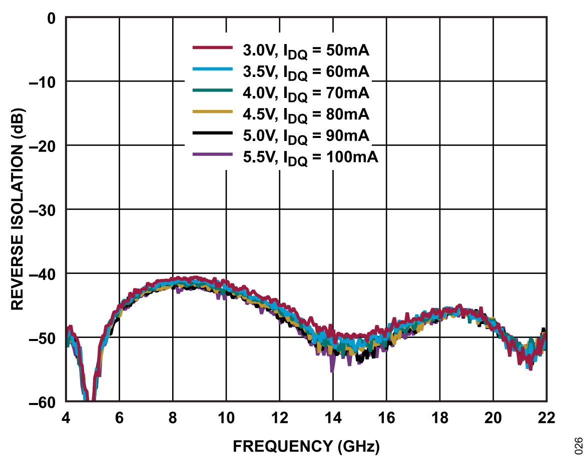

Figure 26. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

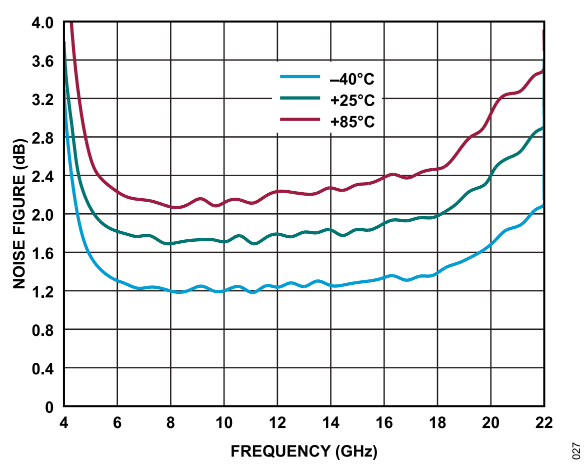

Figure 27. Noise Figure vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

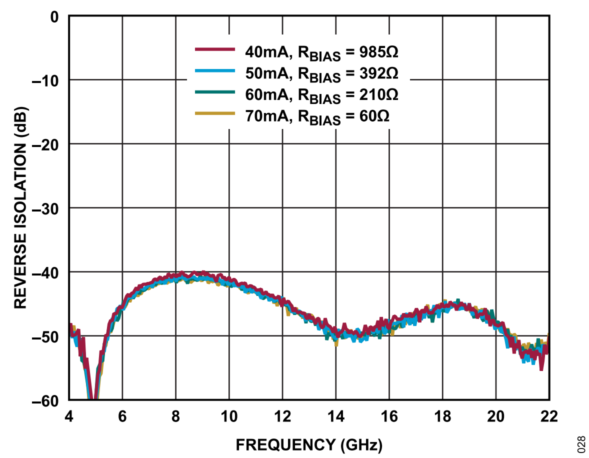

Figure 28. Reverse Isolation vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

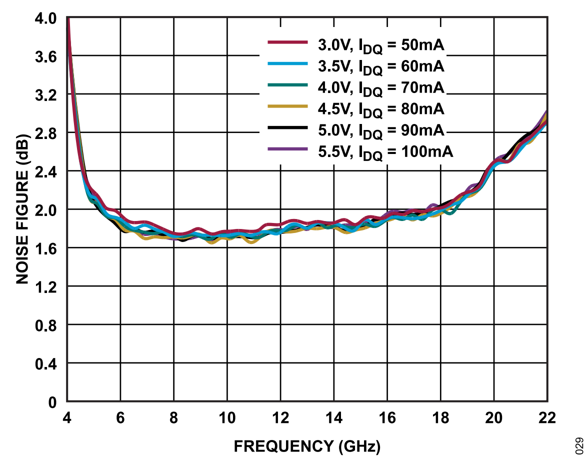

Figure 29. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

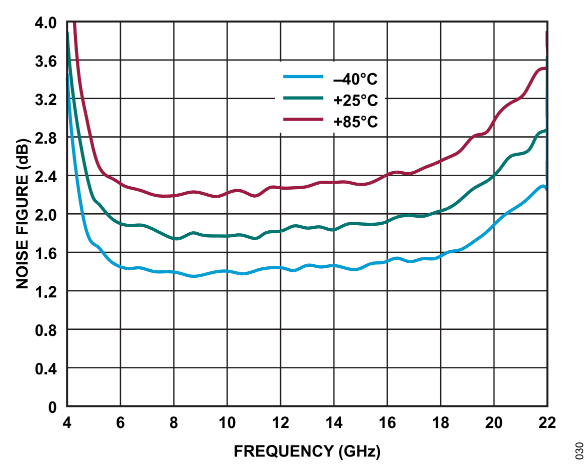

Figure 30. Noise Figure vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

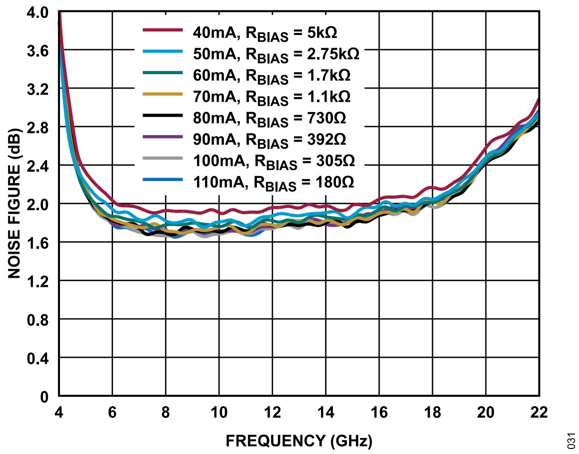

Figure 31. Noise Figure vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

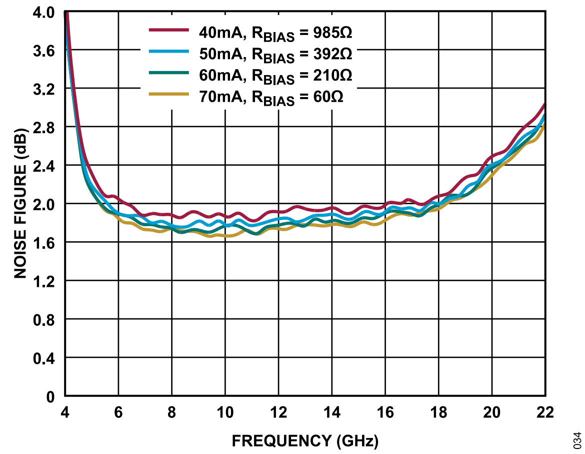

Figure 34. Noise Figure vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

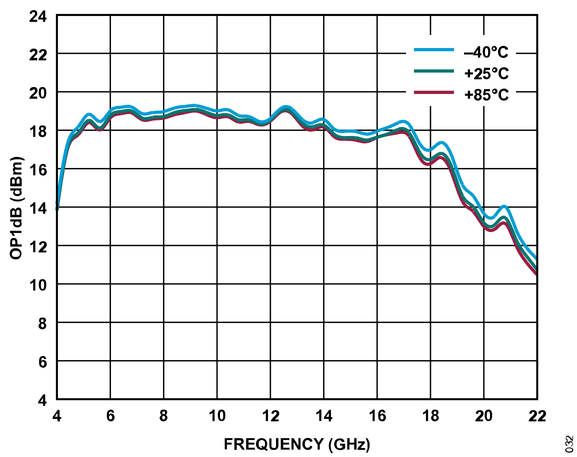

Figure 32. OP1dB vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

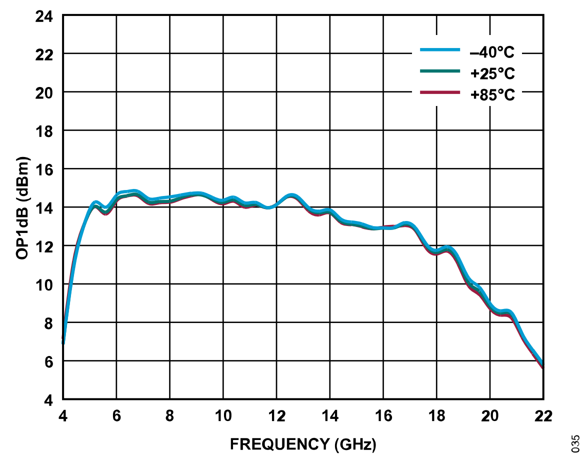

Figure 35. OP1dB vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

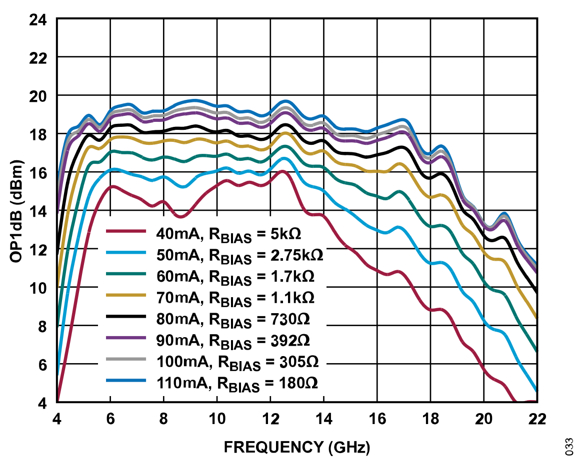

Figure 33. OP1dB vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

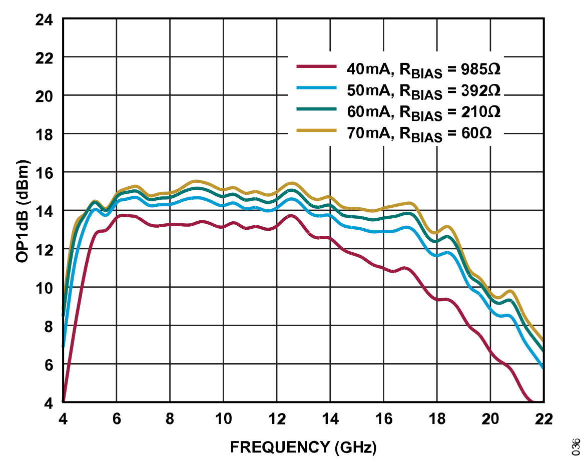

Figure 36. OP1dB vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

TYPICAL PERFORMANCE CHARACTERISTICS

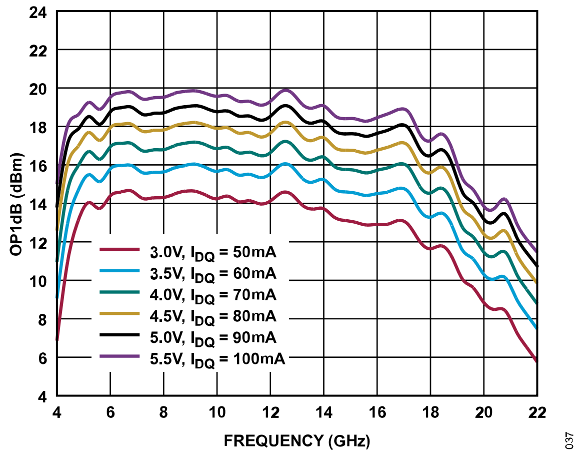

Figure 37. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ}, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

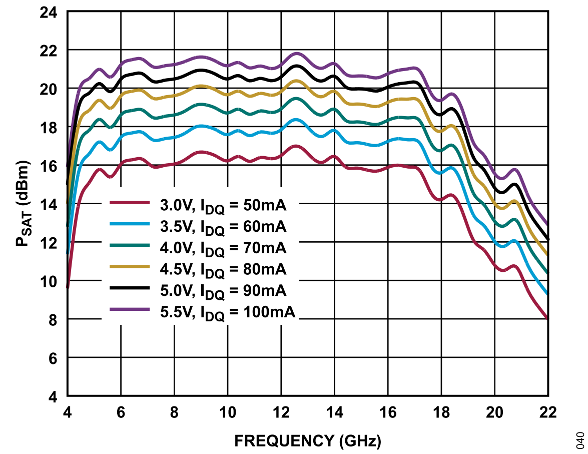

Figure 40. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

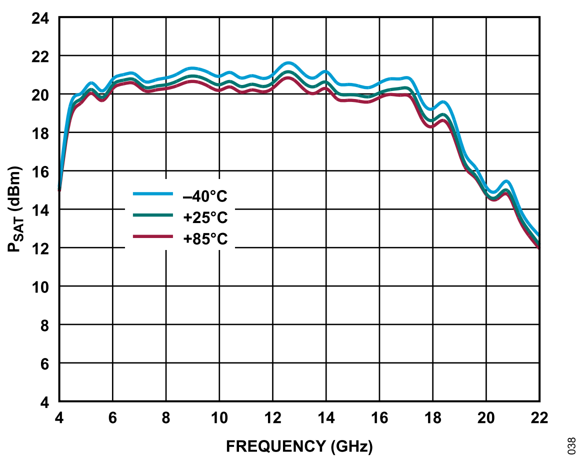

Figure 38. P_{SAT} vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

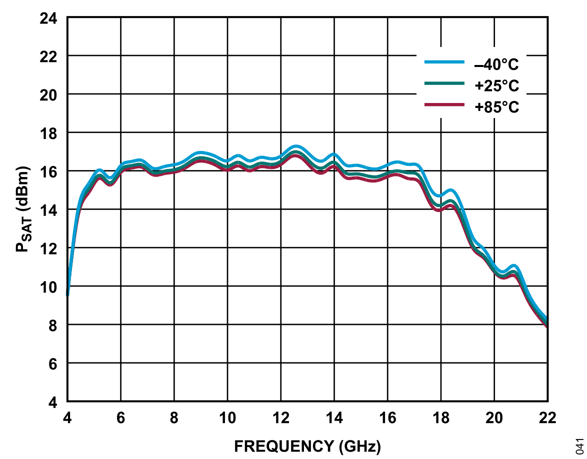

Figure 41. P_{SAT} vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

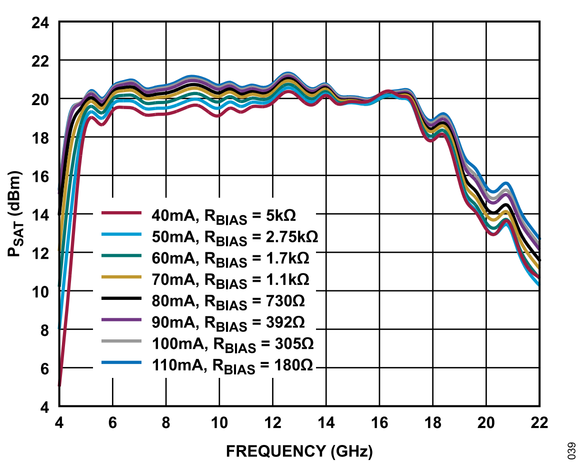

Figure 39. P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

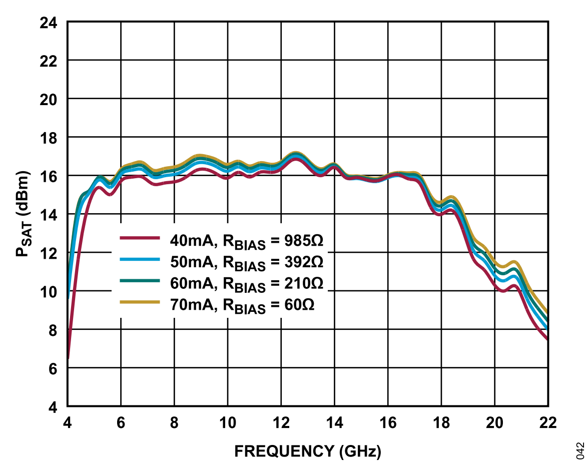

Figure 42. P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

TYPICAL PERFORMANCE CHARACTERISTICS

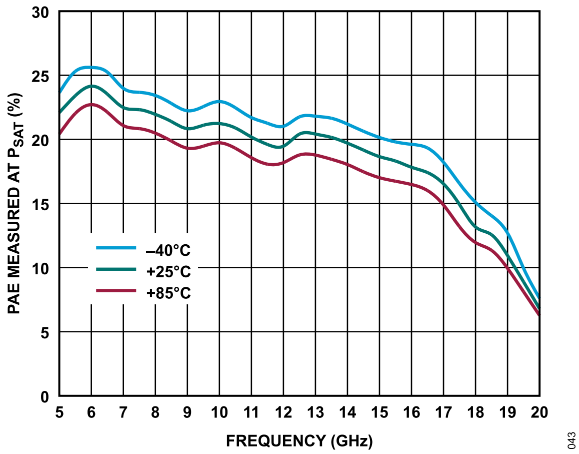

Figure 43. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 5 GHz to 20 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

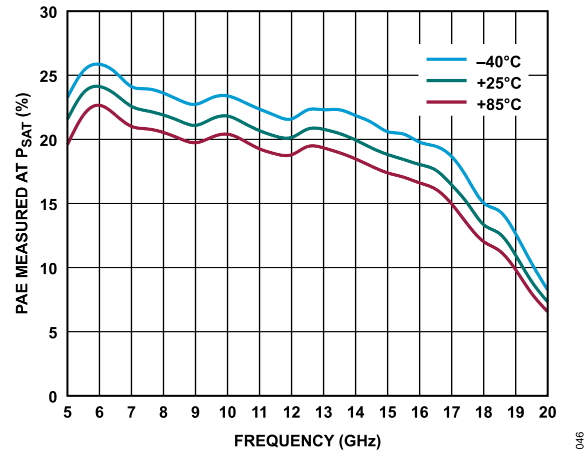

Figure 46. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 5 GHz to 20 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

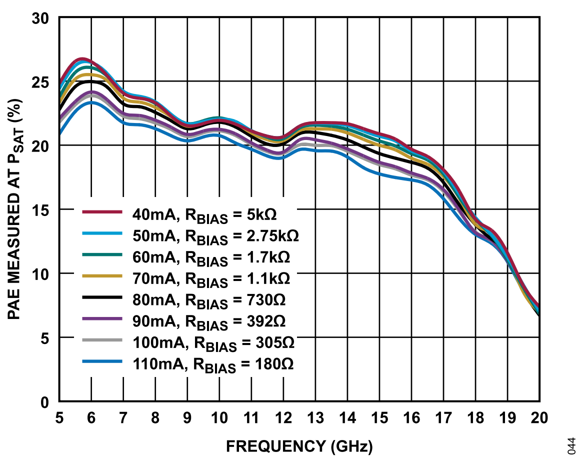

Figure 44. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 5 GHz to 20 GHz, V_{DD} = 5 V

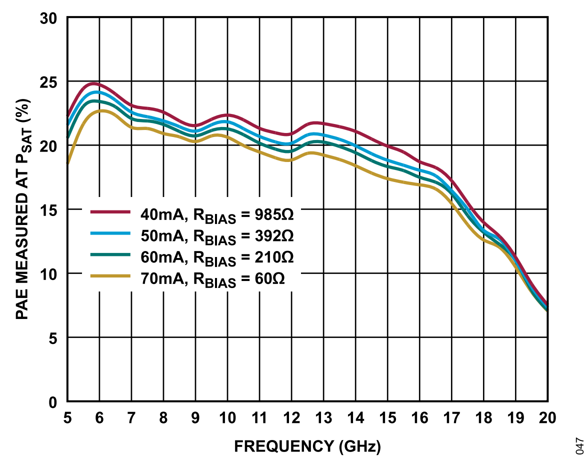

Figure 47. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 5 GHz to 20 GHz, V_{DD} = 3 V

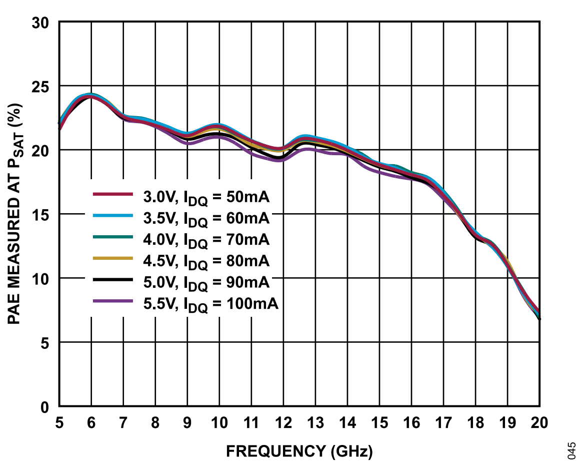

Figure 45. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, 5 GHz to 20 GHz, R_{BIAS} = 392 Ω

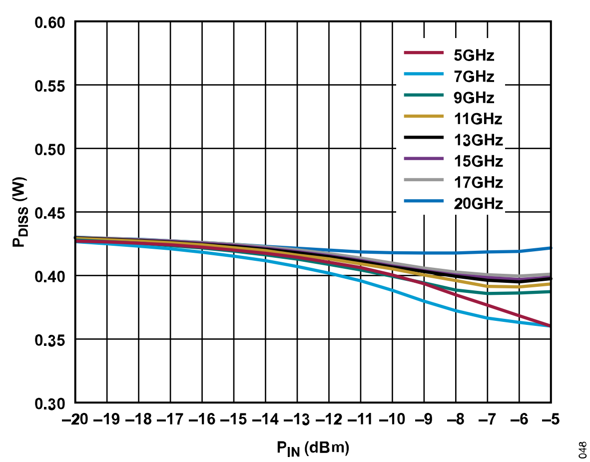

Figure 48. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

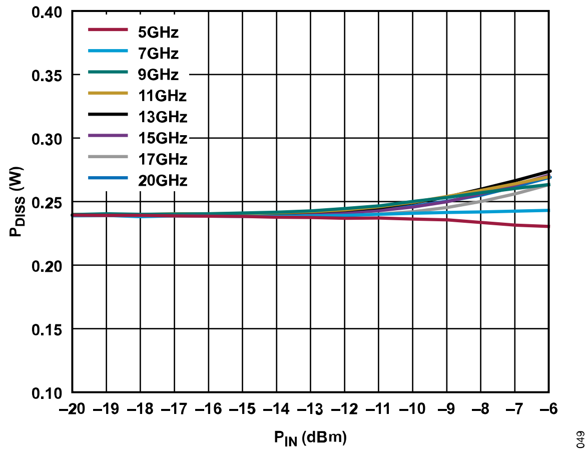

Figure 49. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, V_{DD} = 3 V

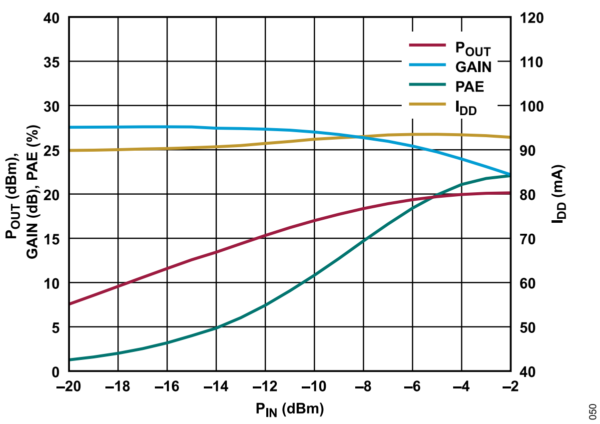

Figure 50. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 5 GHz, V_{DD} = 5 V, R_{BIAS} = 392 Ω

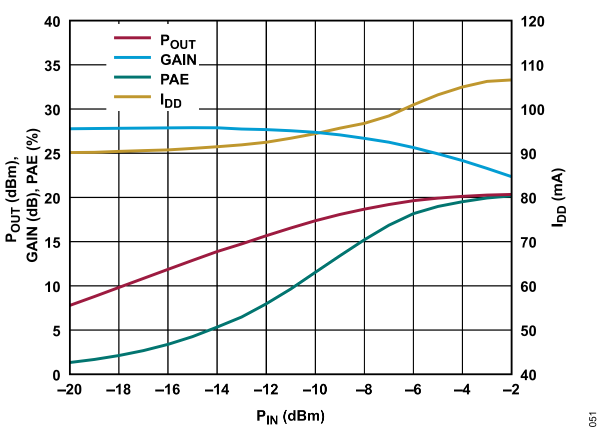

Figure 51. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 11 GHz, V_{DD} = 5 V, R_{BIAS} = 392 Ω

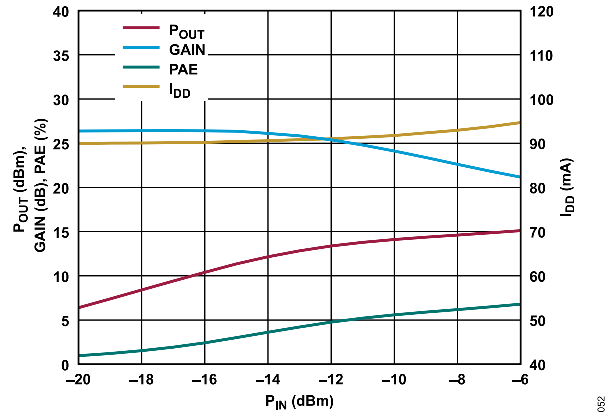

Figure 52. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 20 GHz, V_{DD} = 5 V, R_{BIAS} = 392 Ω

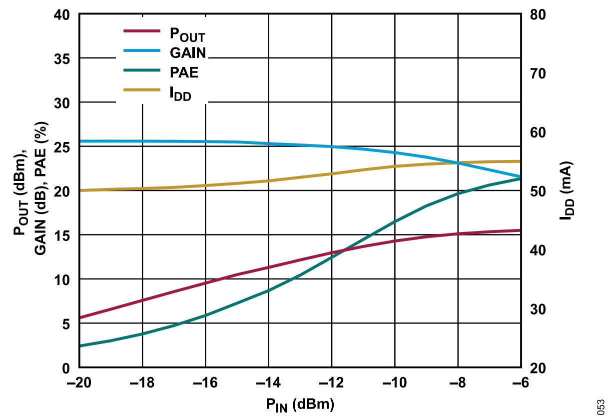

Figure 53. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 5 GHz, V_{DD} = 3 V, R_{BIAS} = 392 Ω

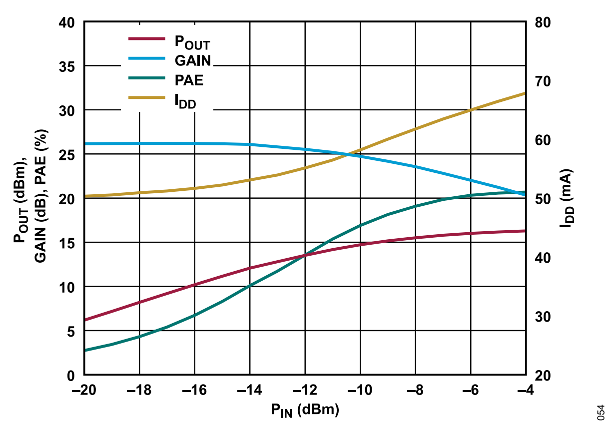

Figure 54. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 11 GHz, V_{DD} = 3 V, R_{BIAS} = 392 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

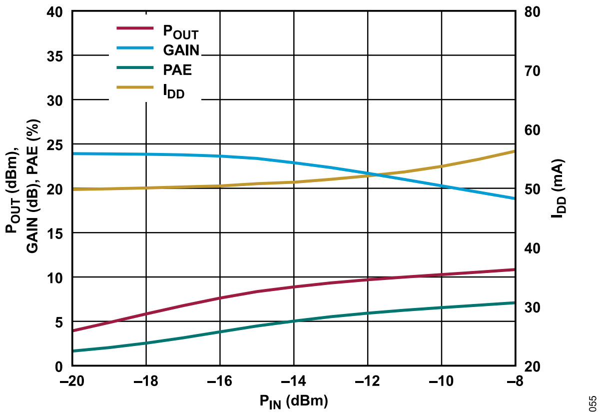

Figure 55. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 20 GHz, V_{DD} = 3 V, R_{BIAS} = 392 Ω

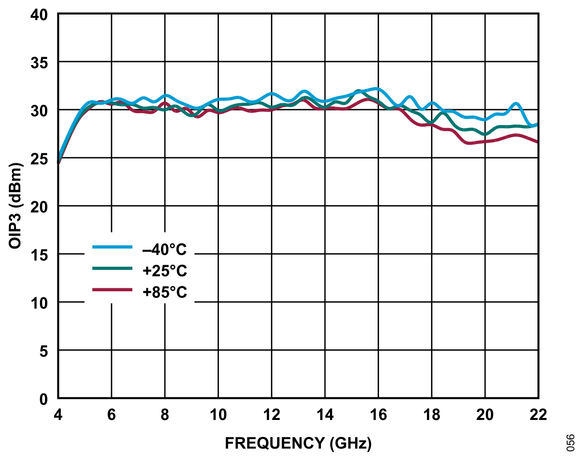

Figure 56. OIP3 vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

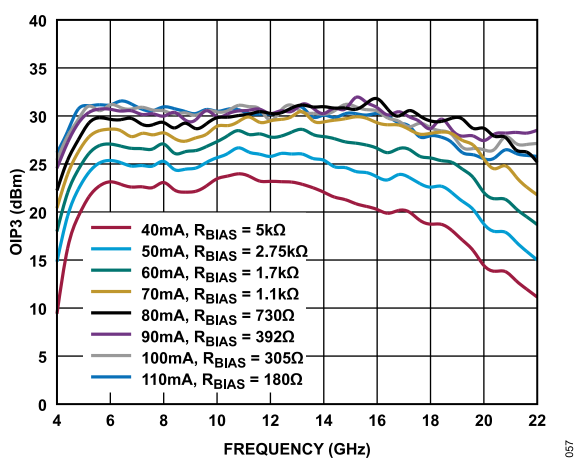

Figure 57. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

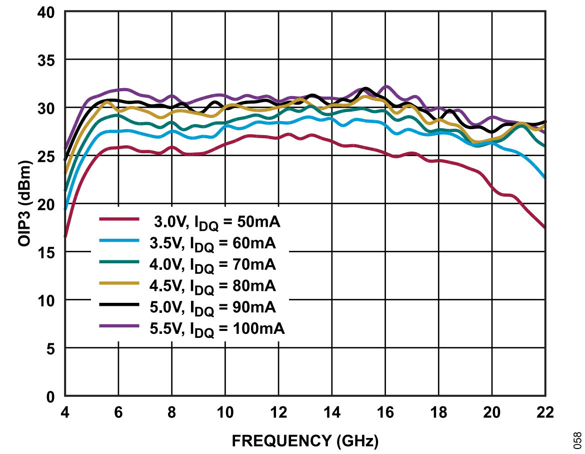

Figure 58. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

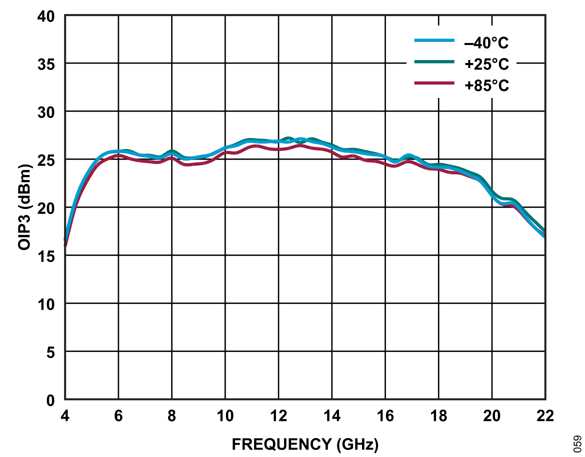

Figure 59. OIP3 vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

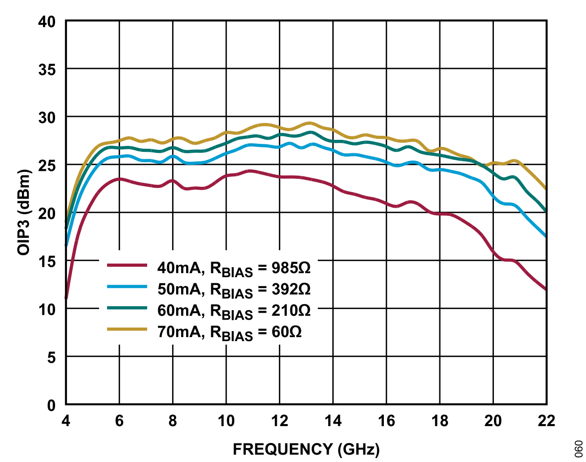

Figure 60. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

TYPICAL PERFORMANCE CHARACTERISTICS

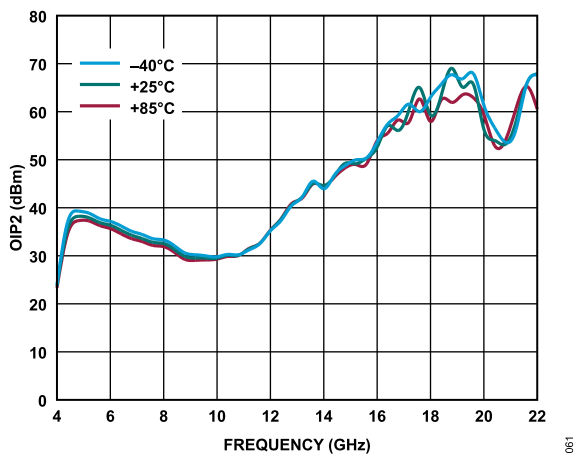

Figure 61. OIP2 vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 392 Ω

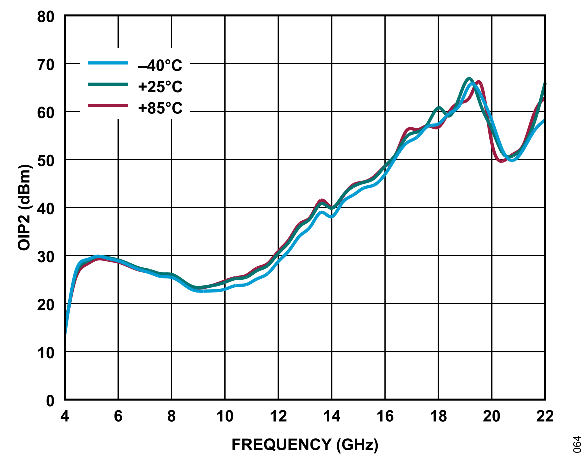

Figure 64. OIP2 vs. Frequency for Various Temperatures, 4 GHz to 22 GHz, V_{DD} = 3 V, I_{DQ} = 50 mA, R_{BIAS} = 392 Ω

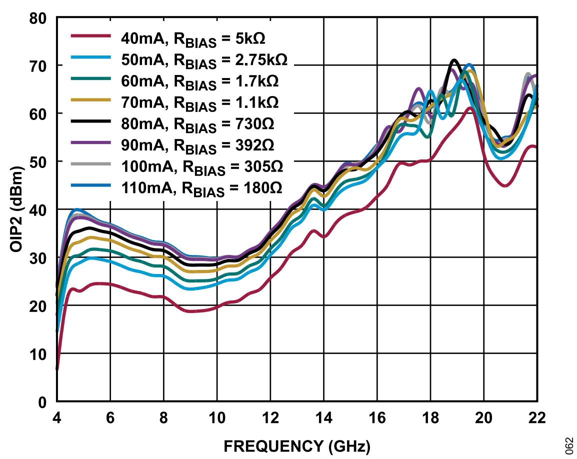

Figure 62. OIP2 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 5 V

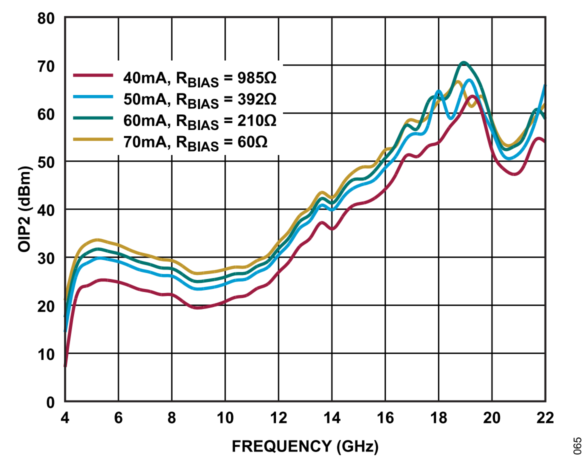

Figure 65. OIP2 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 4 GHz to 22 GHz, V_{DD} = 3 V

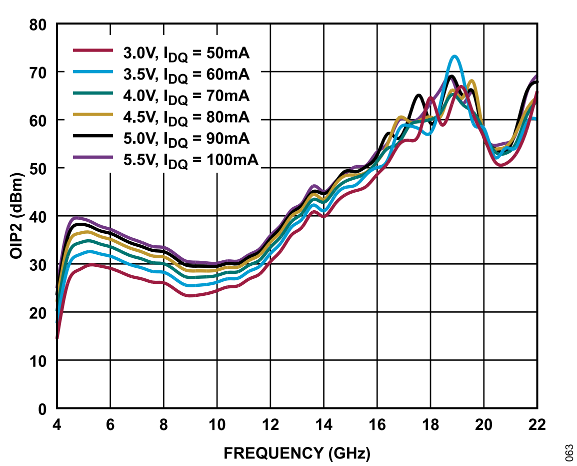

Figure 63. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 4 GHz to 22 GHz, R_{BIAS} = 392 Ω

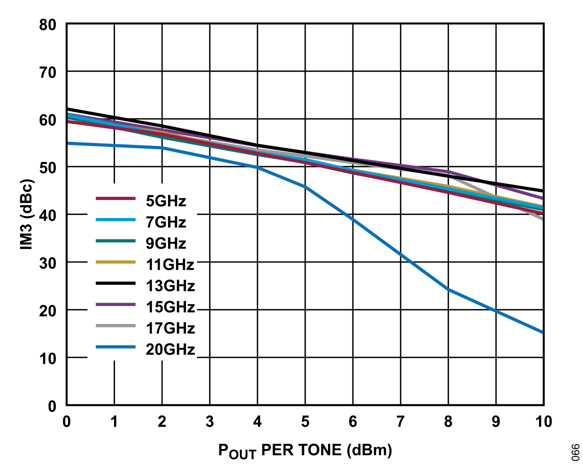

Figure 66. Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, R_{BIAS} = 392 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

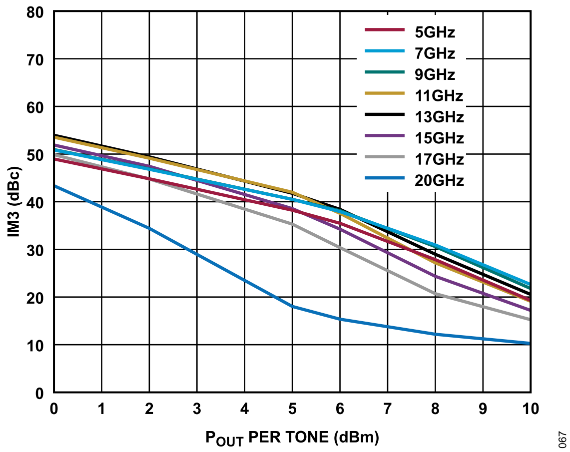

Figure 67. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, R_{BIAS} = 392 Ω

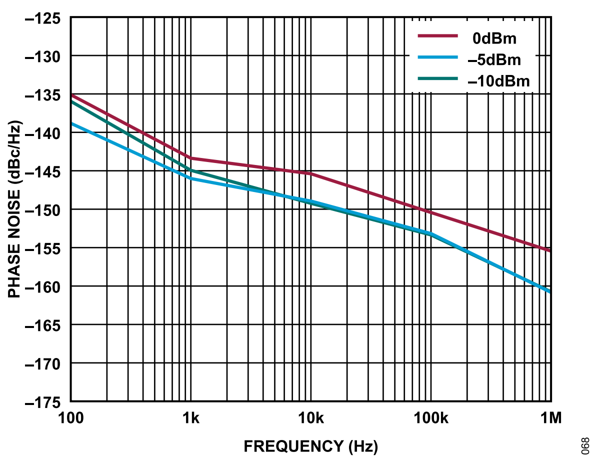

Figure 68. Phase Noise vs. Frequency at 6 GHz for Various P_{IN} Values

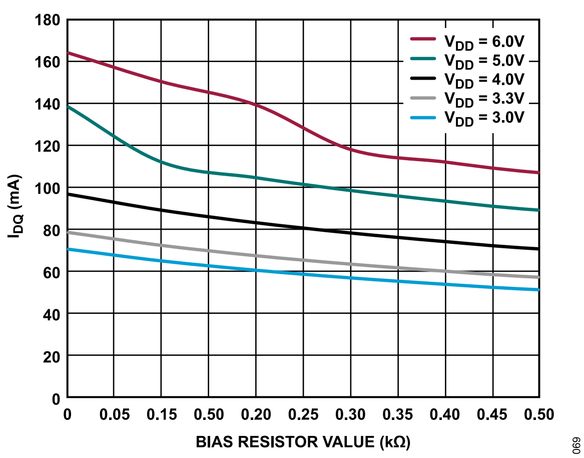

Figure 69. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 500 Ω

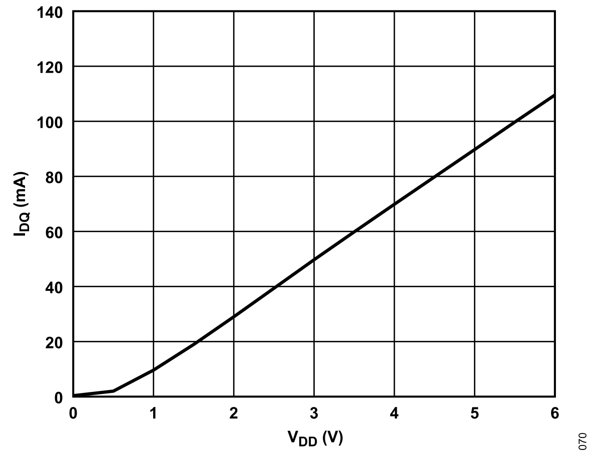

Figure 70. I_{DQ} vs. Supply Voltage, R_{BIAS} = 392 Ω

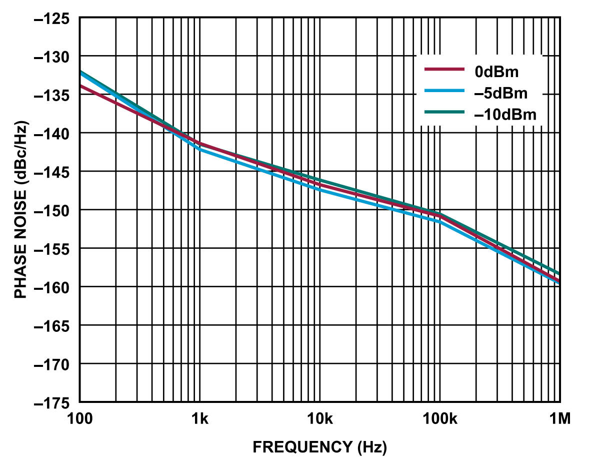

Figure 71. Phase Noise vs. Frequency at 9 GHz for Various P_{IN} Values

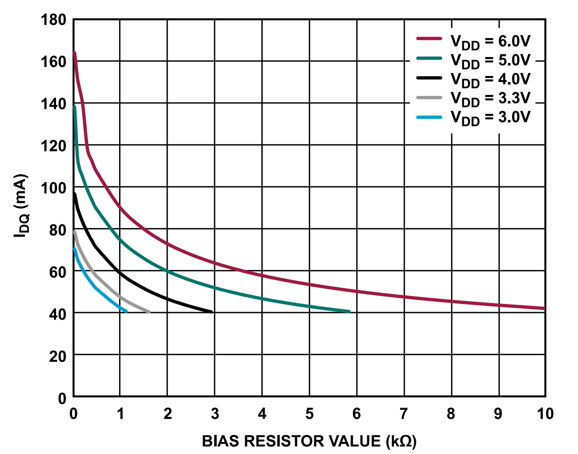

Figure 72. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 10 kΩ

THEORY OF OPERATION

The ADL8105 has ac-coupled, single-ended input and output ports with impedance that are nominally equal to 50 Ω over the 5 GHz to 20 GHz frequency range. No external matching components are required. To adjust I_{DQ}, connect an external resistor between the RBIAS and VDD pins. Figure 73 shows the simplified block diagram.

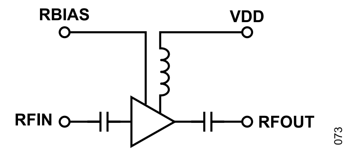

Figure 73. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8105 over the specified frequency range are shown in Figure 74. No external biasing inductor is required, allowing the 5 V supply to be connected to the VDD pin. It is recommended to use 0.01 μF and 100 pF power supply decoupling capacitors. The power supply decoupling capacitors shown in Figure 74 represent the configuration used to characterize and qualify the ADL8105.

To set I_{DQ}, connect a resistor (R2) between the RBIAS and VDD pins. A default value of 392 Ω is recommended, which results in a nominal I_{DQ} of 90 mA. Table 9 shows how I_{DQ} and I_{DQ_AMP} vary vs. R_{BIAS}. The RBIAS pin also draws a current that varies with the value of R_{BIAS} (see Table 9). Do not leave the RBIAS pin open.

Correct sequencing of the dc and RF power is required to safely operate the ADL8105. During power-up, apply V_{DD} before the RF power is applied to RFIN, and during power-off, remove the RF power from RFIN before V_{DD} is powered off.

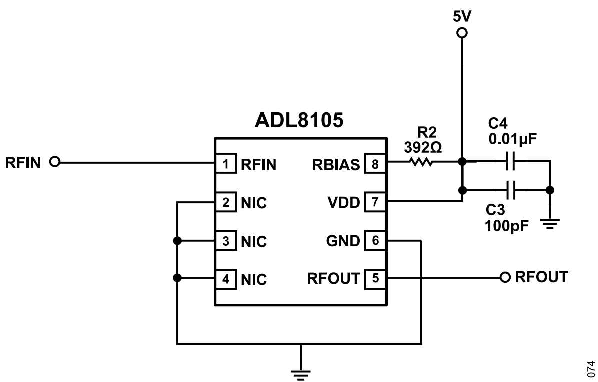

Figure 74. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

See the ADL8105-EVALZ user guide for the recommended bias sequencing information.

Table 9. Recommended R_{BIAS} Values for V_{DD} = 5 V

R_{BIAS} (kΩ)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
5	40	39.18	0.82
2.75	50	48.6	1.4
1.7	60	57.9	2.1
1.1	70	67.2	2.8
0.73	80	76.4	3.6
0.392	90	85	5
0.305	100	94.6	5.4
0.18	110	103.6	6.4

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 75 shows a recommended power management circuit for the ADL8105. The LT8607 step-down regulator is used to step down a 12 V rail to 6.5 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 75 has an input voltage of 12 V, the input range to the LT8607 can be as high as 42 V.

The 6.54 V regulator output of the LT8607 is set by the R2 and R3 resistors according to the following equation:

$R2 = R3((VOUT/0.778\ \text{V}) - 1)$

The switching frequency is set to 2 MHz by the 18.2 kΩ resistor on the RT pin. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.200 MHz.

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin according to the following equation:

$VOUT = 100\ \mu\text{A} \times R4$

The PGFB resistors are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%); therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range. Table 10 provides the recommended resistor values for operation at 5 V, 3.3 V, and 3 V.

Table 10. Recommended Resistor Values for Operating at 5 V, 3.3 V, and 3 V

LDO Output Voltage (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
5	49.9	442	30.1
3.3	33.2	287	30.1
3	30.1	255	30.1

The LT8607 can source a maximum current of 750 mA, and the LT3042 can source a maximum current of 200 mA. If the 5 V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5 A and 3 A, respectively, and these devices are pin-compatible with the LT8607. The LT3045 linear regulator, which is pin-compatible with the LT3042, can source a maximum current to 500 mA.

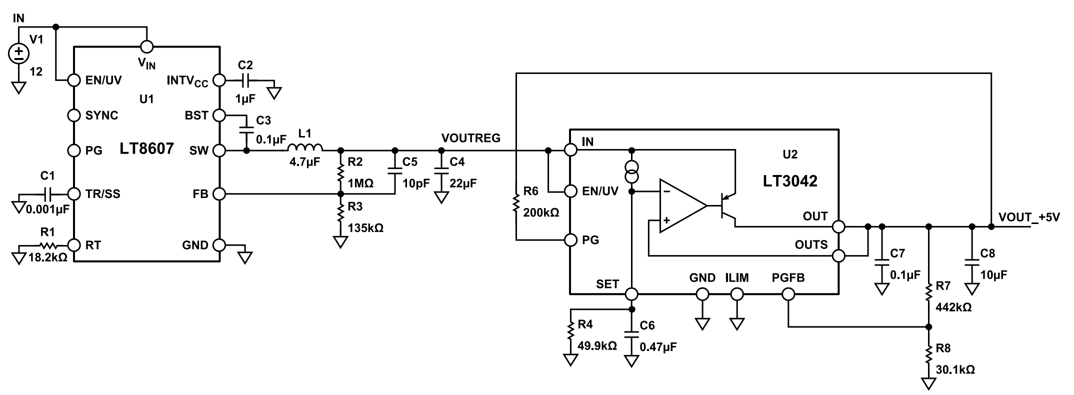

Figure 75. Recommended Power Management Circuit

USING THE RBIAS PIN TO ENABLE AND DISABLE THE ADL8105

By attaching a single-pole, double throw (SPDT) switch to the RBIAS pin, an enable and/or disable circuit can be implemented as shown in Figure 76. The ADG719 CMOS switch is used to connect the R_{BIAS} resistor either to supply or ground. When the R_{BIAS} resistor is connected to ground, the overall current consumption reduces to 4.73 mA with no RF signal present and 4.92 mA when the RF input level is –10 dBm.

Figure 77 shows a plot of the turn on and/or turn off response time of the RF output envelope when the IN pin of the ADG719 is pulsed.

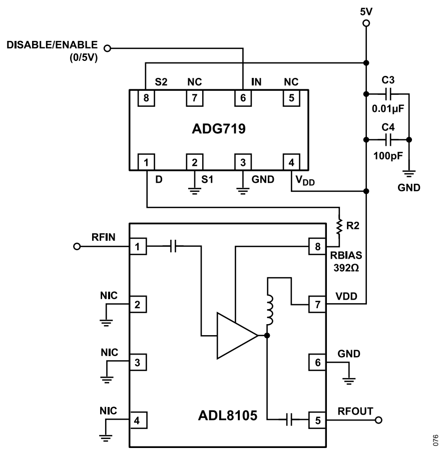

Figure 76. Fast Enable and/or Disable Circuit Using an SPDT

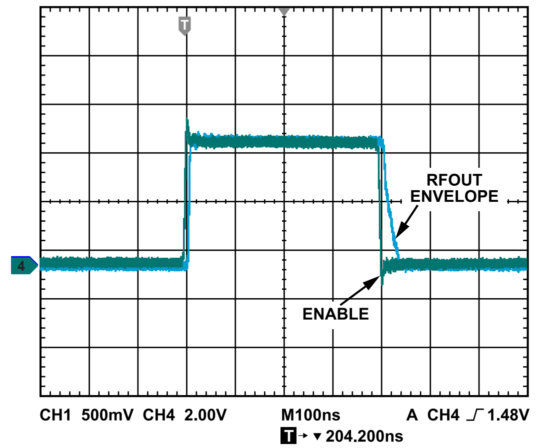

Figure 77. On and/or Off Response of the RF Output Envelope When the IN Pin of the ADG719 Is Pulsed

OUTLINE DIMENSIONS

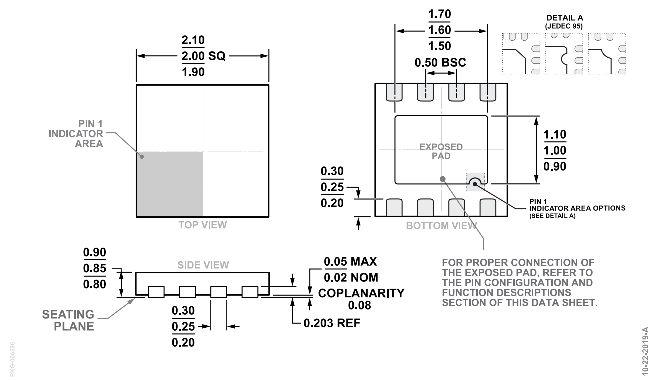

Figure 78. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

Updated: July 07, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADL8105ACPZN	-40°C to +85°C	8-lead LFCSP 2 mm × 2 mm × 0.85		CP-8-30	Y82
ADL8105ACPZN-R7	-40°C to +85°C	8-lead LFCSP 2 mm × 2 mm × 0.85	Reel, 3000	CP-8-30	Y82

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADL8105-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.