4.5 Ω R_{ON}, 1.8 V Logic-Compatible Quad SPDT Switch

FEATURES

- 4.5 Ω typical on resistance for +5 V to −8 V supply at 25°C
- 1.2 Ω on-resistance flatness for +5 V to −8 V supply at 25°C
- Up to 346 mA continuous current
- Fully specified
  - V_{DD} = +5 V ± 10%
  - V_{SS} = −4.5 V to −8.8 V
- No V_L supply required
- 1.8 V logic-compatible inputs
- Rail-to-rail operation
- 20-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- LDMOS power amplifier gate drive
- GaN power amplifier gate drive
- Communication systems
- Automatic test equipment
- Data acquisition systems
- Sample-and-hold systems

GENERAL DESCRIPTION

The ADG1534 contains four independent SPDT switches. An $\overline{EN}$ input on the ADG1534 is used to enable or disable the device. When disabled, all channels are high impedance. The digital inputs, INx, are 1.8 V logic-compatible and suitable for low voltage logic controls.

The ADG1534 is fully specified at V_{DD} = +5 V ± 10% and V_{SS} = −4.5 V to −8.8 V for applications that require asymmetrical supplies. The ultra-low on resistance and on-resistance flatness of the switches makes it an ideal solution for data acquisition and gain switching applications, where low distortion is critical. The construction ensures ultra-low power dissipation, making the device ideally-suited for portable and battery-powered instruments.

The switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All channels exhibit a break-before-make switching action that prevents momentary shorting when switching channels.

FUNCTIONAL BLOCK DIAGRAM

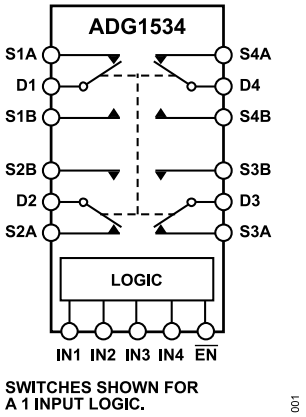


Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. 8 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. 1.8 V logic-compatible digital inputs.
4. No logic power supply (V_L) required.
5. 20-lead, 4 mm × 4 mm LFCSP.

TABLE OF CONTENTS

REVISION HISTORY

10/2023—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −4.5 V to −8.8 V, and GND = 0 V, unless otherwise noted.

Table 1. Dual Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5 V, V_{SS} = −7.2 V
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	4.5			Ω typ	Source voltage (V_S) = V_{SS} to V_{DD}, source current (I_S) = −10 mA, see Figure 17
	5	7	8	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = V_{SS} to V_{DD}, I_S = −10 mA
	0.3	0.35	0.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.2			Ω typ	V_S = V_{SS} to V_{DD}, I_S = −10 mA
	1.4	1.7	2.0	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −8.8 V
Source Off, I_S (Off)	±0.01			nA typ	V_S and drain voltage (V_D) = +4.5 V to −7.8 V, see Figure 18
	±10	±12	±30	nA max	
Drain Off, I_D (Off)	±0.02			nA typ	V_S and V_D = +4.5 V to −7.8 V, see Figure 18
	±10	±12	±30	nA max	
Drain Channel On, I_D (On), Source Channel On, I_S (On)	±0.02			nA typ	V_S and V_D = +4.5 V to −7.8 V, see Figure 19
	±10	±12	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.5	V max	
Input Current, I_{INH} or I_{INL}	0.001			μA typ	V_{INx} = ground voltage (V_{GND}) or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					V_{DD} = +5 V, V_{SS} = −8 V
Transition Time, $t_{TRANSITION}$	179			ns typ	Resistance load (R_L) = 300 Ω, load capacitance (C_L) = 35 pF
	236	264	286	ns max	V_S = 2.5 V, see Figure 20
Enable Delay On Time, t_{ON} ($\overline{EN}$)	164			ns typ	R_L = 300 Ω, C_L = 35 pF
	209	241	265	ns max	V_S = 2.5 V, see Figure 22
Enable Delay Off Time, t_{OFF} ($\overline{EN}$)	192			ns typ	R_L = 300 Ω, C_L = 35 pF
	253	280	300	ns max	V_S = 2.5 V, see Figure 22
Break-Before-Make Time Delay, t_{BBM}	32			ns typ	R_L = 300 Ω, C_L = 35 pF
			21	ns min	V_S = 2.5 V, see Figure 21
Charge Injection, Q_{INJ}	−12.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 23
Off Isolation	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 24
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 26
Total Harmonic Distortion, THD	−102			dB typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 1 kHz to 20 kHz, Figure 15
	−95			dB typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 100 kHz, Figure 15
Total Harmonic Distortion Plus Noise, THD + N	0.002			% typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 100 kHz, see Figure 27

SPECIFICATIONS

Table 1. Dual Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth	77			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 25
Insertion Loss	0.26			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 25
Source Off Capacitance, C_S (Off)	19			pF typ	V_S = 0 V, frequency = 1 MHz
Drain Off Capacitance, C_D (Off)	33			pF typ	V_S = 0 V, frequency = 1 MHz
Drain On Capacitance, C_D (On) and Source On Capacitance, C_S (On)	57			pF typ	V_S = 0 V, frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −8.8 V
Positive Supply Current, I_{DD}	160			µA typ	V_{INx} = 0 V or V_{DD}
			230	µA max	
Negative Supply Current, I_{SS}	0.001			µA typ	V_{INx} = 0 V or V_{DD}
			1	µA max	

CONTINUOUS CURRENT PER CHANNEL, SxA, SxB, OR Dx

Table 2. Four Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, SxA, SxB, or Dx[1] (θ_{JA} = 51.8°C/W)				
V_{DD} = +5 V, V_{SS} = −8 V	191	120	70	mA maximum

[1] SxA and SxB refer to the S1A to S4A pins and the S1B to S4B pins (respectively), and Dx refers to the D1 to D4 pins.

Table 3. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, SxA, SxB, or Dx[1] (θ_{JA} = 51.8°C/W)				
V_{DD} = +5 V, V_{SS} = −8 V	346	187	86	mA maximum

[1] SxA and SxB refer to the S1A to S4A pins and the S1B to S4B pins (respectively), and Dx refers to the D1 to D4 pins.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +16.5 V
V_{SS} to GND	+0.3 V to −16.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[2]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, SxA, SxB, or Dx[3]	513 mA (pulsed at 1 ms, 10% duty-cycle maximum)
Continuous Current, SxA, SxB, or Dx Pins	Data[4] + 15%
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-free	As per JEDEC J-STD-020

1 Overvoltages at the SxA, SxB, and Dx analog input pins are clamped by internal diodes. Limit the current to the maximum ratings given.

2 Overvoltages at the INx digital input pins are clamped by internal diodes.

3 SxA and SxB refers to the S1A to S4A pins and the S1B to S4B (respectively), and Dx refers to the D1 to D4 pins.

4 See Table 1 and Table 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction-to-case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-20-10[1]	51.8	9.4	°C/W

1 Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADG1534

Table 6. ADG1534, 20-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±3500	2
FICDM	±1250	C3

1 For the input and output port to the supplies, the input and output port to the input and output port, and all other inputs.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

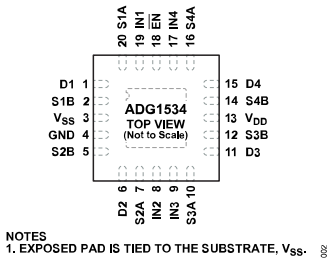


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal 1. The D1 pin can be an input or an output.
2	S1B	Source Terminal 1B. The S1B pin can be an input or an output.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, the V_{SS} pin can be connected to ground.
4	GND	Ground (0 V) Reference.
5	S2B	Source Terminal 2B. The S2B pin can be an input or an output.
6	D2	Drain Terminal 2. The D2 pin can be an input or an output.
7	S2A	Source Terminal 2A. The S2A pin can be an input or an output.
8	IN2	Logic Control Input 2.
9	IN3	Logic Control Input 3.
10	S3A	Source Terminal 3A. The S3A pin can be an input or an output.
11	D3	Drain Terminal 3. The D3 pin can be an input or an output.
12	S3B	Source Terminal 3B. The S3B pin can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	S4B	Source Terminal 4B. The S4B pin can be an input or an output.
15	D4	Drain Terminal 4. The D4 pin can be an input or an output.
16	S4A	Source Terminal 4A. The S4A pin can be an input or an output.
17	IN4	Logic Control Input 4.
18	$\overline{EN}$	Active Low Digital Input. When the $\overline{EN}$ pin is high, the device is disabled, and all switches are off. Also, when the $\overline{EN}$ pin is low, the INx logic inputs determine the on switches.
19	IN1	Logic Control Input 1.
20	S1A	Source Terminal 1A. The S1A pin can be an input or an output.
Not applicable	EPAD	Exposed Pad. The exposed pad is tied to the substrate, V_{SS}.

Table 8. Truth Table

$\overline{EN}$	INx	SxA	SxB
1	Don't care	Off	Off
0	0	Off	On
0	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

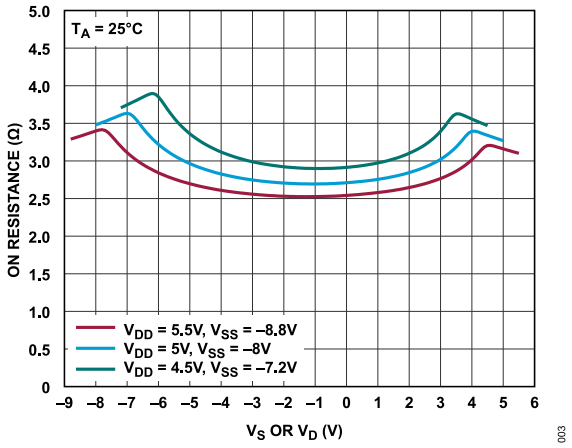


Figure 3. On Resistance vs. V_S or V_D

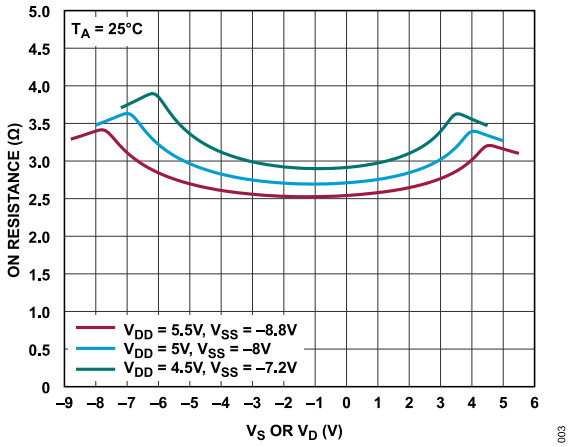


Figure 4. On Resistance vs. V_S or V_D for Different Temperatures

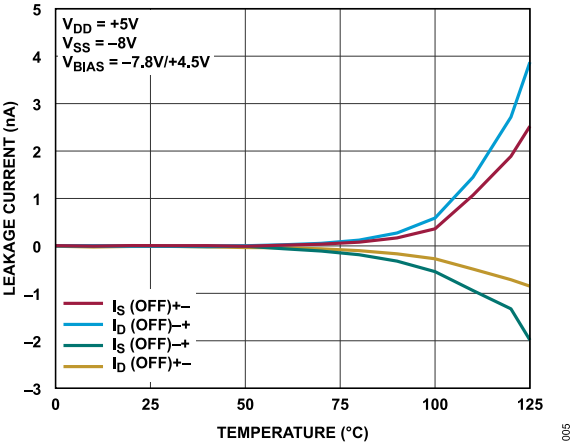


Figure 5. Off Leakage Current vs. Temperature

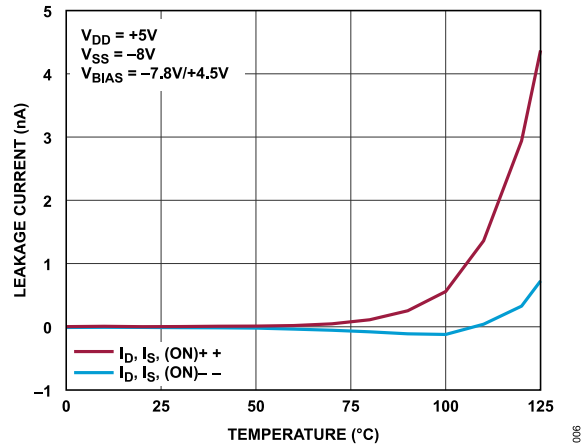


Figure 6. On Leakage Current vs. Temperature (V_{BIAS} is Bias Voltage)

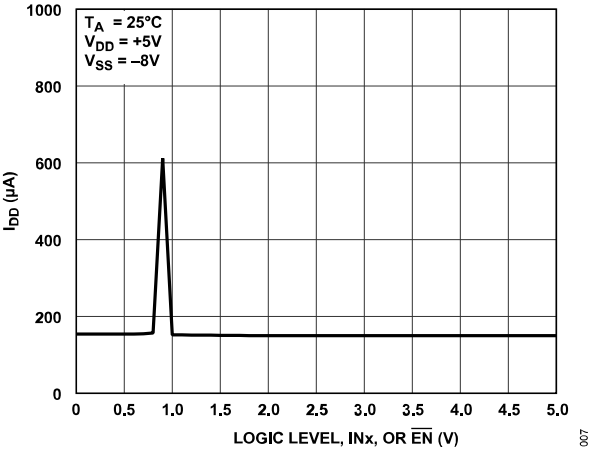


Figure 7. I_{DD} vs. Logic Level, INx, or $\overline{EN}$

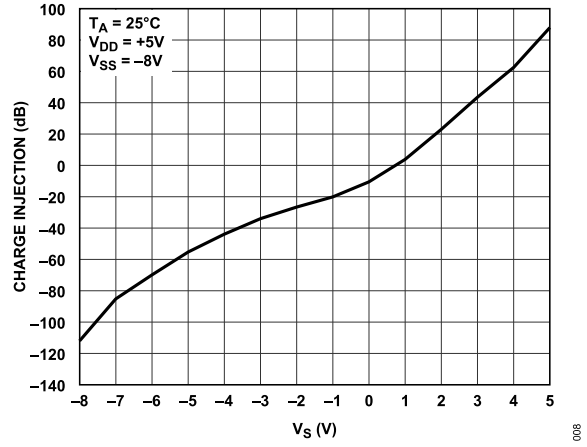


Figure 8. Charge Injection vs. V_S

TYPICAL PERFORMANCE CHARACTERISTICS

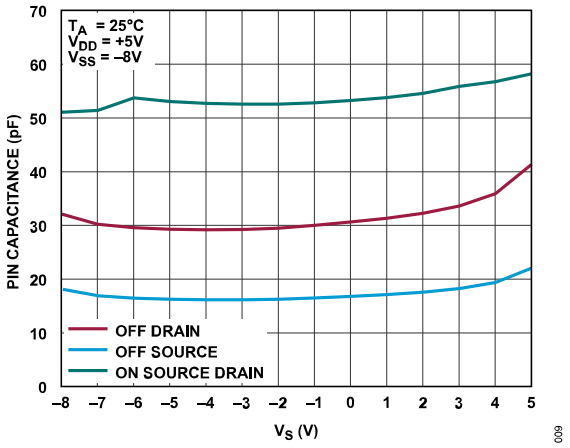


Figure 9. Pin Capacitance vs. V_S

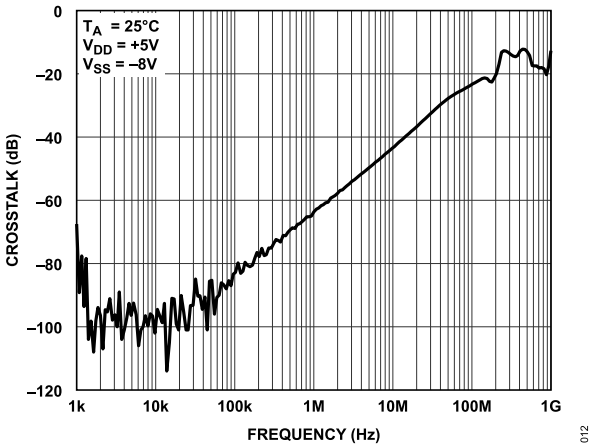


Figure 12. Crosstalk vs. Frequency

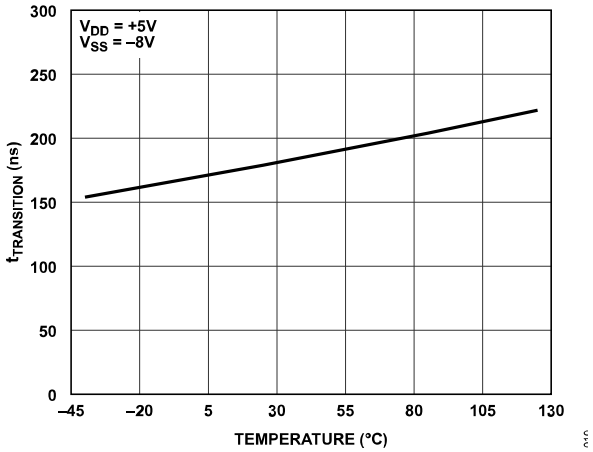


Figure 10. $t_{TRANSITION}$ vs. Temperature

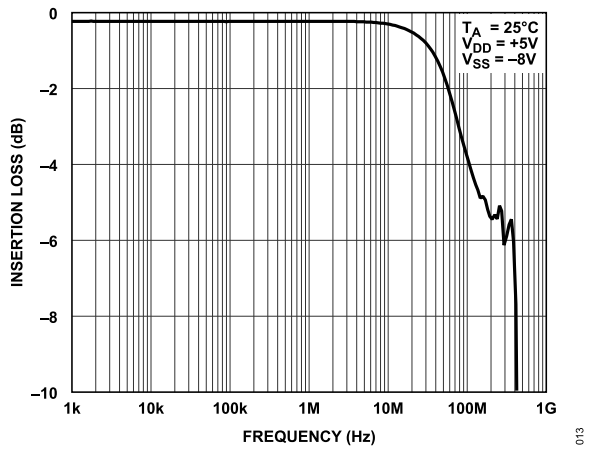


Figure 13. Insertion Loss vs. Frequency

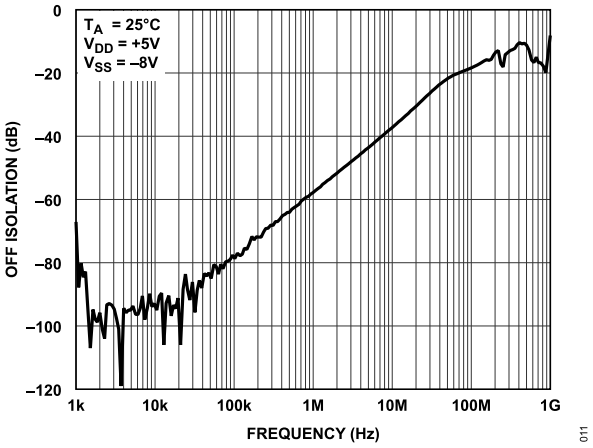


Figure 11. Off Isolation vs. Frequency

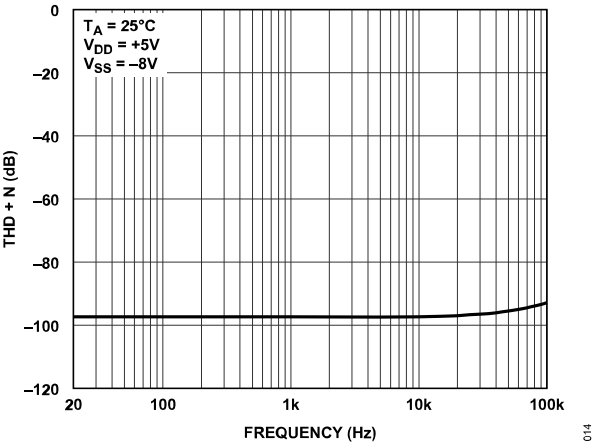


Figure 14. THD + N vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

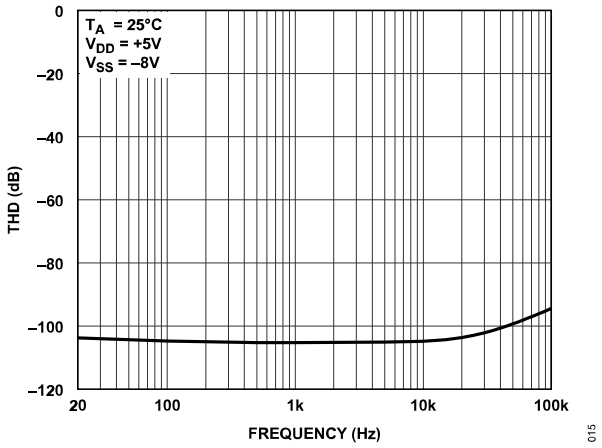


Figure 15. THD vs. Frequency

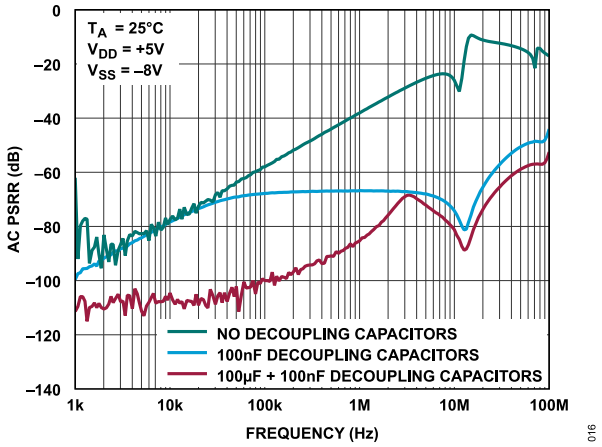


Figure 16. AC Power Supply Rejection Ratio (PSRR) vs. Frequency

TEST CIRCUITS

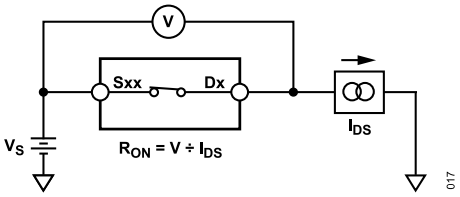


Figure 17. On Resistance

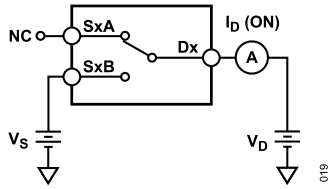


Figure 19. On Leakage (NC = No Connect)

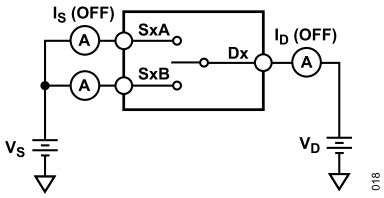


Figure 18. Off Leakage

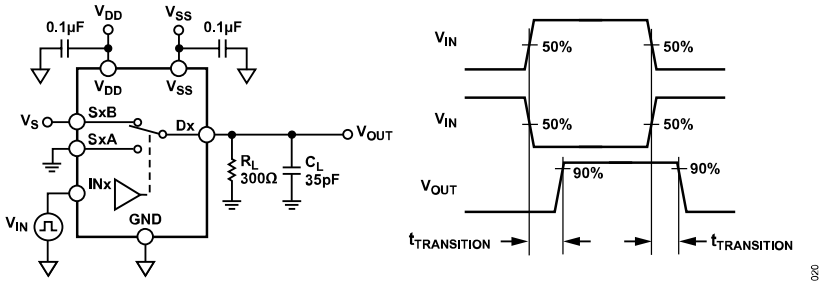


Figure 20. $t_{TRANSITION}$ (Input Voltage (V_{IN}) and Output Voltage (V_{OUT}))

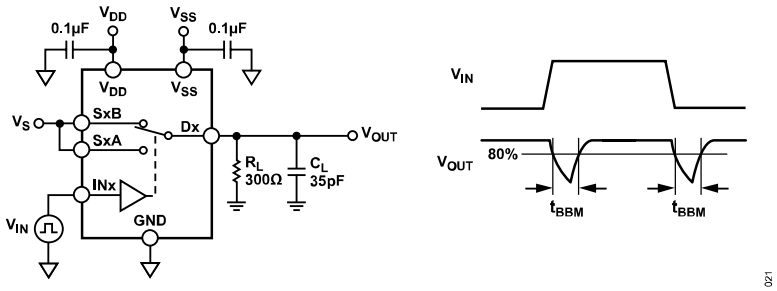


Figure 21. t_{BBM} Delay

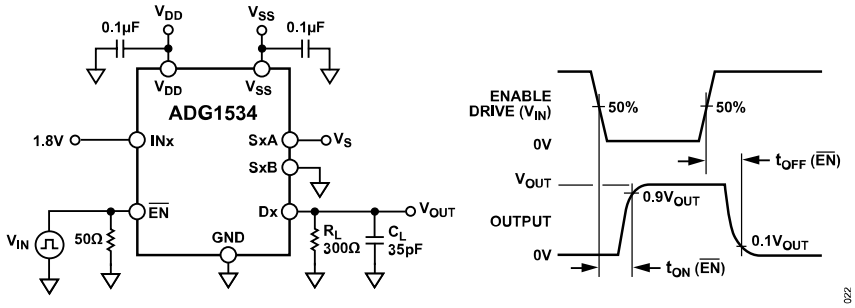


Figure 22. Enable Delay On Time, t_{ON} ($\overline{EN}$) and Enable Delay Off Time, t_{OFF} ($\overline{EN}$)

TEST CIRCUITS

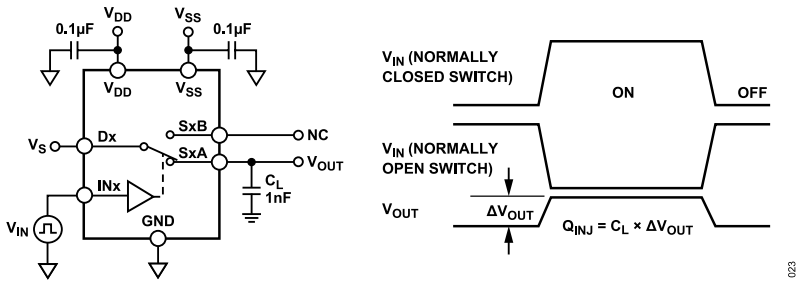


Figure 23. Charge Injection

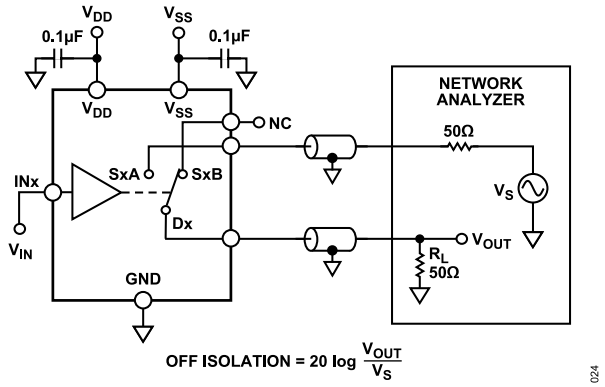


Figure 24. Off Isolation

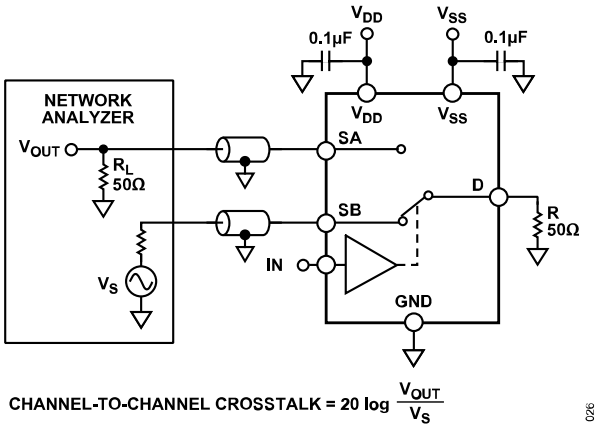


Figure 26. Channel-to-Channel Crosstalk

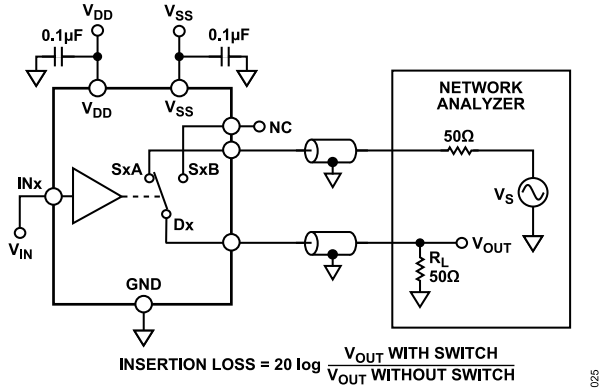


Figure 25. Bandwidth

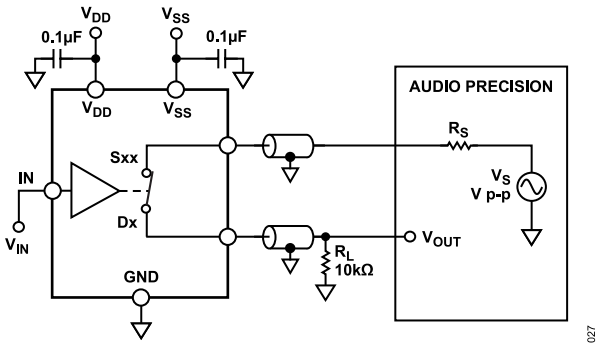
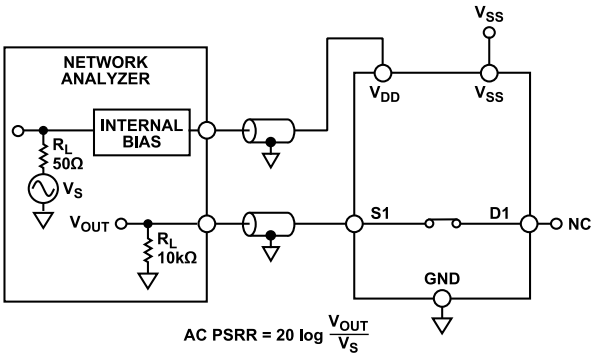


Figure 27. THD + Noise

TEST CIRCUITS



NOTES
1. BOARD AND COMPONENT EFFECTS ARE NOT DE-EMBEDDED FROM THE AC PSRR MEASUREMENT.

030

Figure 28. AC PSRR

TERMINOLOGY

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of the on resistance measured.

I_S Off

Source leakage current when the switch is off.

I_D Off

Drain leakage current when the switch is off.

I_D (On) and I_S (On)

Channel drain and source leakage currents when the switch is on.

V_D and V_S

Analog voltages on Terminal D and Terminal S.

C_S (Off) and C_D (Off)

Channel source and drain capacitance for off condition.

C_D (On) and C_S (On)

On switch drain and source capacitance.

C_{IN}

Digital input capacitance.

t_{ON} ($\overline{EN}$)

Enable delay on time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)

Enable delay off time between the 50% and 10% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INH}

Input high current of the digital input.

I_{INL}

Input low current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Channel-to-Channel Crosstalk

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion (THD)

THD is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

Total Harmonic Distortion Plus Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

A measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.115 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the AC PSRR.

APPLICATIONS INFORMATION

POWER AMPLIFIER GATE DRIVE

Figure 29 shows a typical application where the ADG1534 is used to set the gate bias voltage for an RF power amplifier for communications applications. The asymmetrical dual supply and rail-to-rail operation of the ADG1534 allows for negative voltages of up to –8 V for biasing gallium nitride (GaN) power amplifiers, and the positive +5 V rail is ideal for laterally diffused metal-oxide semiconductor (LDMOS) power amplifiers.

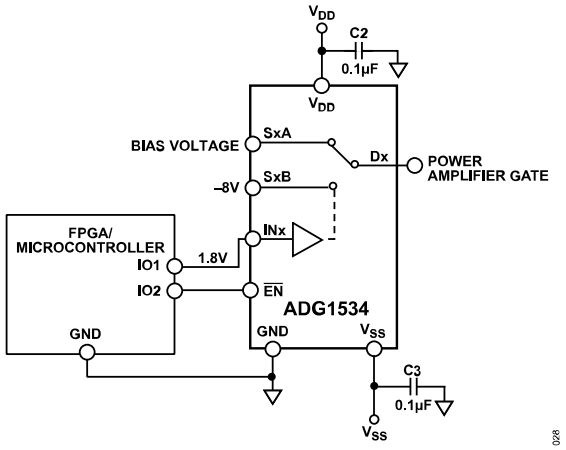


Figure 29. GaN Power Amplifier Gate Drive

POWER SUPPLY RAILS

To guarantee correct operation of the ADG1534, 0.1 µF decoupling capacitors are required on the V_{DD} and V_{SS} pins.

The ADG1534 can operate with asymmetrical bipolar supplies between of V_{DD} = +5 V ± 10% and V_{SS} = −4.5 V to −8.8 V. The supplies on V_{DD} and V_{SS} do not have to be asymmetrical. However, the V_{DD} to V_{SS} range must not exceed 18 V, as stated in the Absolute Maximum Ratings section.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of an asymmetrical bipolar power solution is shown in Figure 30. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADG1534. Two optional positive and negative low dropout regulators (LDO) are shown in Figure 30). The ADP7118 and ADP7182 can reduce the output ripple of the ADP5070 in ultra-low noise sensitive applications.

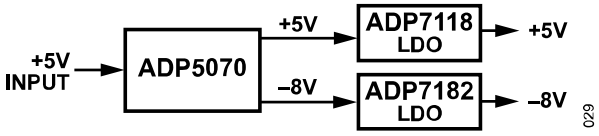


Figure 30. Bipolar Power Solution

Table 9. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, DC-to-DC switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS, LDO linear regulator
ADP7182	−28 V, −200 mA, low noise, LDO linear regulator

OUTLINE DIMENSIONS

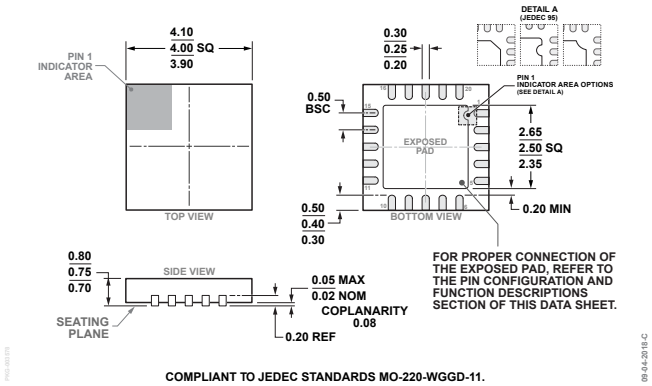


Figure 31. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-10)
Dimensions shown in millimeters

Updated: October 13, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADG1534BCPZ-REEL7	−40°C to +125°C	20-Lead LFCSP (4 mm x 4 mm w/ EP)	Reel, 1500	CP-20-10

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADG1534EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.