Data Sheet

LTC2323-12

Dual, 12-Bit + Sign, 5 Msps Differential Input ADC with Wide Input Common Mode Range

FEATURES

- 5 Msps Throughput Rate
- ±0.5 LSB INL (Typ)
- Guaranteed 12-Bit, No Missing Codes
- 8 V_{P-P} Differential Inputs with Wide Input Common Mode Range
- 73 dB SNR (Typ) at f_{IN} = 2 MHz
- –85 dB THD (Typ) at f_{IN} = 2 MHz
- Guaranteed Operation to 125°C
- Single 3.3 V or 5 V Supply
- Low Drift (20 ppm/°C Max) 2.048 V or 4.096 V Internal Reference
- 1.8 V to 2.5 V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 38 mW/Ch (Typ)
- Small 28-Lead (4 mm × 5 mm) QFN Package

APPLICATIONS

- High Speed Data Acquisition Systems
- Communications
- Remote Data Acquisition
- Imaging
- Optical Networking
- Multiphase Motor Control

GENERAL DESCRIPTION

The LTC2323-12 is a low noise, high speed dual 12-bit + sign successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3 V or 5 V supply, the LTC2323-12 has an 8 V_{P-P} differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2323-12 achieves ±0.5 LSB INL typical, no missing codes at 12 bits and 73 dB SNR.

The LTC2323-12 has an onboard low drift (20 ppm/°C max) 2.048 V or 4.096 V temperature-compensated reference. The LTC2323-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 5 Msps per channel throughput with one-cycle latency makes the LTC2323-12 ideally suited for a wide variety of high speed applications. The LTC2323-12 dissipates only 38 mW per channel and offers nap and sleep modes to reduce the power consumption to 5 µW for further power savings during inactive periods.

TYPICAL APPLICATION

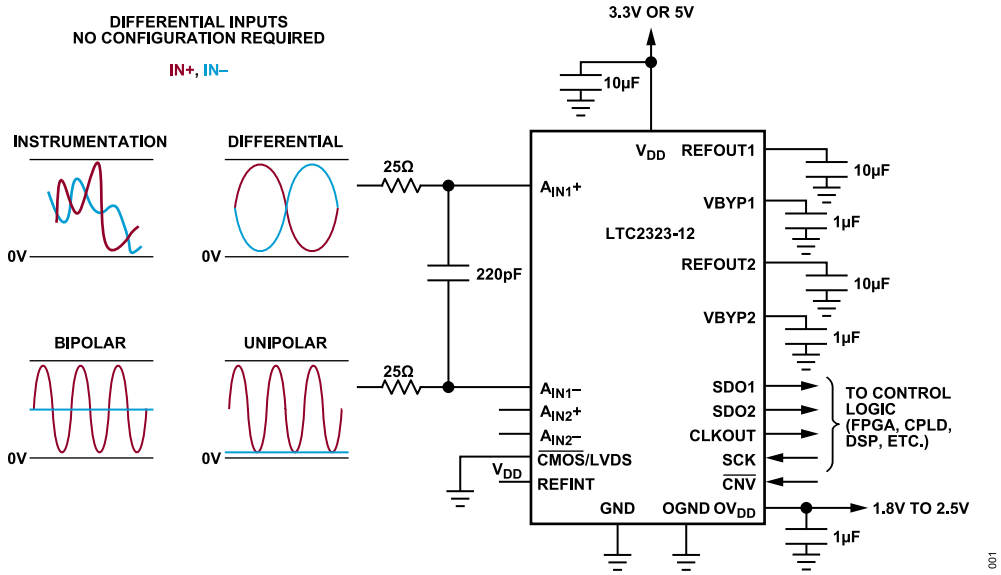

Figure 1. Typical Application of LTC2323-12

Rev. C

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4/2024—Rev. B to Rev. C

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FUNCTIONAL BLOCK DIAGRAM

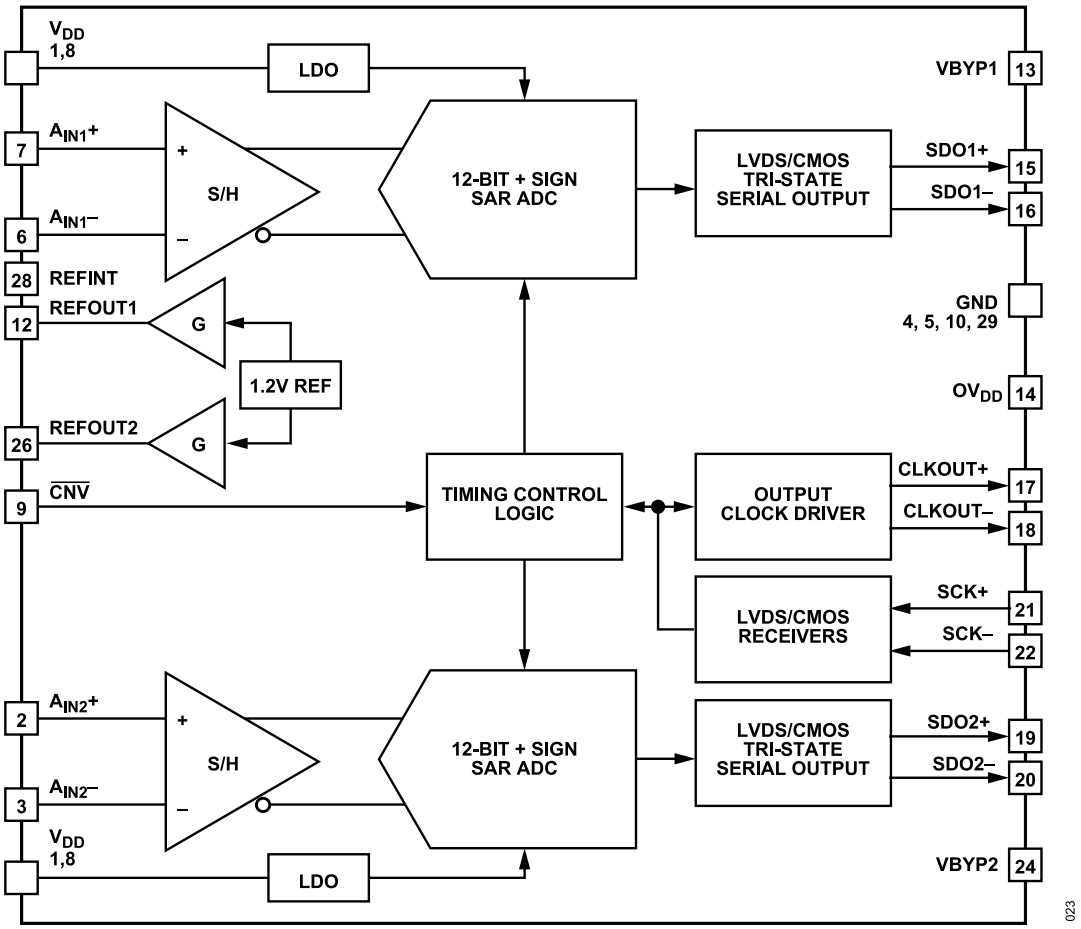


Figure 2. Functional Block Diagram of LTC2323-12

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS						
Absolute Input Range (A_{IN1^+}, A_{IN2^+})[1]	V_{IN+}		0		V_{DD}	V
Absolute Input Range (A_{IN1^-}, A_{IN2^-})[1]	V_{IN-}		0		V_{DD}	V
Input Differential Voltage Range	$V_{IN+} - V_{IN-}$	$V_{IN} = V_{IN^+} - V_{IN^-}$	–REFOUT1,2		REFOUT1,2	V
Common Mode Input Range	V_{CM}	$V_{IN} = (V_{IN^+} + V_{IN^-})/2$	0		V_{DD}	V
Analog Input DC Leakage Current	I_{IN}		–1		1	µA
Analog Input Capacitance	C_{IN}	T_A = 25°C		10		pF
Input Common Mode Rejection Ratio	CMRR	f_{IN} = 2.2 MHz T_A = 25°C		85		dB
External Reference Current[2, 3]	I_{REFOUT}	REFINT = 0 V, REFOUT = 4.096 V T_A = 25°C		675		µA

1 Recommended operating conditions.

2 When REFOUT1,2 is overdriven, the internal reference buffer must be turned off by setting REFINT = 0 V.

3 f_{SMPL} = 5 MHz, I_{REFOUT} varies proportionally with sample rate.

CONVERTER CHARACTERISTICS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz, 1 LSB = 2 • REFOUT1,2/2^{12}.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CONVERTER CHARACTERISTICS						
Resolution			12			Bits
No Missing Codes			12			Bits
Transition Noise		T_A = 25°C		0.2		LSB_{RMS}
Integral Linearity Error[1]	INL		–1	±0.5	1	LSB
Differential Linearity Error	DNL		–0.99	±0.4	0.99	LSB
Bipolar Zero-Scale Error[2]	BZE		–3	0	3	LSB
Bipolar Zero-Scale Error Drift		T_A = 25°C		0.0015		LSB/°C
Bipolar Full-Scale Error[2]	FSE	$V_{REFOUT1,2}$ = 4.096 V (REFINT Grounded)	–20	±3	20	LSB
Bipolar Full-Scale Error Drift		$V_{REFOUT1,2}$ = 4.096 V (REFINT Grounded) T_A = 25°C		15		ppm/°C

1 Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

2 Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0 0000 0000 0000 and 1 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS un-trimmed deviation from ideal first and last code transitions and includes the effect of offset error.

SPECIFICATIONS

DYNAMIC ACCURACY

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C and A_{IN} = –1dBFS. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC ACCURACY						
Signal-to-(Noise + Distortion) Ratio[1]	SINAD	f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 4.096 V, Internal Reference	69.8	72.9		dB
		f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1dBFS		73.2		dB
Signal-to-Noise Ratio[1]	SNR	f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 4.096 V, Internal Reference	70	73		dB
		f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1dBFS		73.5		dB
Total Harmonic Distortion[1]	THD	f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 4.096 V, Internal Reference		–85	–80	dB
		f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1dBFS		–84		dB
Spurious Free Dynamic Range[1]	SFDR	f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 4.096 V, Internal Reference	78	88		dB
		f_{IN} = 2.2 MHz, $V_{REFOUT1,2}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1dBFS		88		dB
–3 dB Input Linear Bandwidth		T_A = 25°C and A_{IN} = –1dBFS		10		MHz
Aperture Delay		T_A = 25°C and A_{IN} = –1dBFS		500		ps
Aperture Delay Matching		T_A = 25°C and A_{IN} = –1dBFS		500		ps
Aperture Jitter		T_A = 25°C and A_{IN} = –1dBFS		1		ps_{RMS}
Transient Response		Full-Scale Step T_A = 25°C and A_{IN} = –1dBFS		3		ns

[1] All specifications in dB are referred to a full-scale ±4.096 V input with REFIN = 4.096 V.

INTERNAL REFERENCE CHARACTERISTICS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE CHARACTERISTICS						
Internal Reference Output Voltage	$V_{REFOUT1,2}$	4.75 V < V_{DD} < 5.25 V	4.088	4.096	4.106	V
		3.13 V < V_{DD} < 3.47 V	2.044	2.048	2.053	
$V_{REFOUT1,2}$ Temperature Coefficient[1]				3	20	ppm/°C
REFOUT1,2 Output Impedance		T_A = 25°C		0.25		Ω
$V_{REFOUT1,2}$ Line Regulation		V_{DD} = 4.75 V to 5.25 V T_A = 25°C		0.3		mV/V

[1] Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

SPECIFICATIONS

DIGITAL INPUTS AND DIGITAL OUTPUTS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS AND DIGITAL OUTPUTS						
High Level Input Voltage	V_{IH}		0.8 • OV_{DD}			V
Low Level Input Voltage	V_{IL}				0.2 • OV_{DD}	V
Digital Input Current	I_{IN}	V_{IN} = 0 V to OV_{DD}	–10		10	µA
Digital Input Capacitance	C_{IN}	T_A = 25°C		5		pF
High Level Output Voltage	V_{OH}	I_O = –500 µA	OV_{DD} – 0.2			V
Low Level Output Voltage	V_{OL}	I_O = 500 µA			0.2	V
Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0 V to OV_{DD}	–10		10	µA
Output Source Current	I_{SOURCE}	V_{OUT} = 0 V T_A = 25°C		–10		mA
Output Sink Current	I_{SINK}	V_{OUT} = OV_{DD} T_A = 25°C		10		mA
LVDS Differential Input Voltage	V_{ID}	100 Ω Differential Termination, OV_{DD} = 2.5 V	240		600	mV
LVDS Common Mode Input Voltage	V_{IS}	100 Ω Differential Termination, OV_{DD} = 2.5 V	1		1.45	V
LVDS Differential Output Voltage	V_{OD}	100 Ω Differential Load, LVDS Mode, OV_{DD} = 2.5 V	100	150	300	mV
LVDS Common Mode Output Voltage	V_{OS}	100 Ω Differential Load, LVDS Mode, OV_{DD} = 2.5 V	0.85	1.2	1.4	V
Low Power LVDS Differential Output Voltage	V_{OD_LP}	100 Ω Differential Load, Low Power, LVDS Mode, OV_{DD} = 2.5 V	75	100	200	mV
Low Power LVDS Common Mode Output Voltage	V_{OS_LP}	100 Ω Differential Load, Low Power, LVDS Mode, OV_{DD} = 2.5 V	0.9	1.2	1.4	V

POWER REQUIREMENTS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY VOLTAGE	V_{DD}	5 V Operation	4.75		5.25	V
		3.3 V Operation	3.13		3.47	V
	OV_{DD}		1.71		2.63	V
SUPPLY CURRENT	I_{VDD}	5 Msps Sample Rate (IN^+ = IN^- = 0 V)		14	18	mA
NAP MODE CURRENT	I_{NAP}	Conversion Done (I_{VDD})		2.85	5	mA
CMOS MODE						
Supply Current	I_{OVDD}	5 Msps Sample Rate (C_L = 5 pF)		2.8	5	mA
Sleep Mode Current	I_{SLEEP}	Sleep Mode (I_{VDD} + I_{OVDD})		1	5	µA
3.3 V Operation						
Power Dissipation	$P_{D\_3.3V}$	V_{DD} = 3.3 V 5 Msps Sample Rate (IN^+ = IN^- = 0 V)		55	58	mW
Nap Mode		V_{DD} = 3.3 V Conversion Done (I_{VDD} + I_{OVDD})		9	13	mW
Sleep Mode		V_{DD} = 3.3 V Sleep Mode (I_{VDD} + I_{OVDD})		5	16.5	µW
5 V Operation						
Power Dissipation	P_{D_5V}	V_{DD} = 5 V 5 Msps Sample Rate (IN^+ = IN^- = 0V)		76	100	mW
Nap Mode		V_{DD} = 5 V Conversion Done (I_{VDD} + I_{OVDD})		15	25	mW
Sleep Mode		V_{DD} = 5 V Sleep Mode (I_{VDD} + I_{OVDD})		5	25	µW
LVDS MODE						
Supply Current		5 Msps Sample Rate (R_L = 100 Ω)		9.5	12	mA
Sleep Mode Current		Sleep Mode (I_{VDD} + I_{OVDD})		1	5	µA

SPECIFICATIONS

Table 6. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
3.3 V Operation						
Power Dissipation	$P_{D\_3.3V}$	V_{DD} = 3.3 V 5 Msps Sample Rate ($IN^+ = IN^- = 0V$)		72	86	mW
Nap Mode		V_{DD} = 3.3 V Conversion Done ($I_{VDD} + I_{OVDD}$)		32	41	mW
Sleep Mode		V_{DD} = 3.3 V Sleep Mode ($I_{VDD} + I_{OVDD}$)		5	16.5	µW
5 V Operation						
Power Dissipation	P_{D_5V}	V_{DD} = 5 V 5 Msps Sample Rate ($IN^+ = IN^- = 0$ V)		105	110	mW
Nap Mode		V_{DD} = 5 V Conversion Done ($I_{VDD} + I_{OVDD}$)		38	40	mW
Sleep Mode		V_{DD} = 5 V Sleep Mode ($I_{VDD} + I_{OVDD}$)		5	25	µW

ADC TIMING SPECIFICATIONS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 MHz.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Maximum Sampling Frequency	f_{SMPL}				5	Msps
Time Between Conversions[1]	t_{CYC}		200		1000000	ns
Conversion Time	t_{CONV}		161.9			ns
$\overline{CNV}$ High Time	t_{CNVH}		35			ns
SCK Quiet Time from $\overline{CNV}\downarrow$[1]	$t_{DCNVSCKL}$		10			ns
SCK Delay Time to $\overline{CNV}\uparrow$ [1]	$t_{DSCKLCNVH}$		20			ns
SCK Period[2, 3]	t_{SCK}	,	9.4			ns
SCK High Time	t_{SCKH}		4			ns
SCK Low Time	t_{SCKL}		4			ns
SCK to CLKOUT Delay[2]	$t_{DSCKCLKOUT}$		2.5			ns
SDO Data Valid Delay from CLKOUT↓[2]	$t_{DCLKOUTSDOV}$	CL = 5 pF			2	ns
SDO Data Remains Valid Delay from CLKOUT↓[1]	t_{HSDO}	CL = 5 pF			2	ns
SDO Data Valid Delay from $\overline{CNV}\downarrow$[1]	$t_{DCNVSDOV}$	CL = 5 pF		2.5	3	ns
Bus Relinquish Time After $\overline{CNV}\uparrow$[1]	$t_{DCNVSDOZ}$				3	ns
REFOUT1,2 Wakeup Time	t_{WAKE}	$C_{REFOUT1,2}$ = 10 µF T_A = 25°C		10		ms

1 Guaranteed by design, not subject to test.

2 Parameter tested and guaranteed at OV_{DD} = 1.71 V and OV_{DD} = 2.5 V.

3 t_{SCK} of 9.4 ns maximum allows a shift clock frequency up to 105 MHz for rising edge capture.

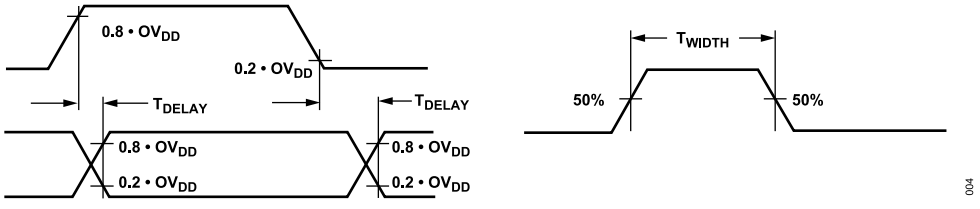


Figure 3. Voltage Levels for Timing Specifications

SPECIFICATIONS

Timing Diagram

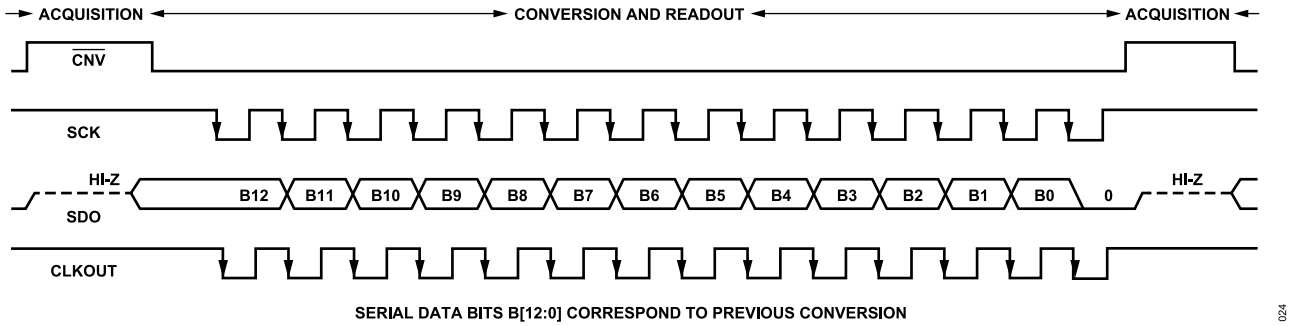


Figure 4. Timing Diagram of LTC2323-12

ABSOLUTE MAXIMUM RATINGS

All voltage values are with respect to ground.

Table 8. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	6 V
Supply Voltage (OV_{DD})	3 V
Supply Bypass Voltage (V_{BYP1}, V_{BYP2})	3 V
Analog Input Voltage	
A_{IN+}, A_{IN-}[1]	–0.3 V to (V_{DD} + 0.3 V)
REFOUT1,2	–0.3 V to (V_{DD} + 0.3 V)
$\overline{CNV}$[2]	–0.3 V to (V_{DD} + 0.3 V)
Digital Input Voltage[1]	(GND – 0.3 V) to (OV_{DD} + 0.3 V)
Digital Output Voltage[1]	(GND – 0.3 V) to (OV_{DD} + 0.3 V)
Power Dissipation	200 mW
Operating Temperature Range	
LTC2323C	0°C to 70°C
LTC2323I	–40°C to 85°C
LTC2323H	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

[1] When these pin voltages are taken below ground, or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100 mA below ground, or above V_{DD} or OV_{DD}, without latch-up.

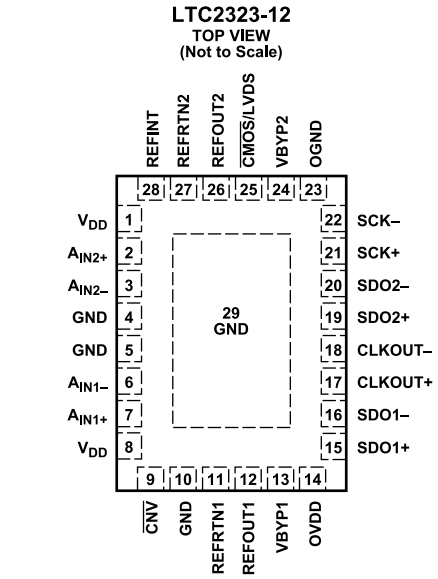
[2] $\overline{CNV}$ is driven from a low jitter digital source, typically at OV_{DD} logic levels. This input pin has a TTL style input that will draw a small amount of current.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. T_{JMAX} = 125°C, θ_{JA} = 43°C/W.
2. EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB.

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Figure 5. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	V_{DD}	Power Supply. Bypass V_{DD} to GND with a 10 µF ceramic and a 0.1 µF ceramic close to the part. The V_{DD} pins should be shorted together and driven from the same supply.
2, 3	A_{IN2^+}, A_{IN2^-}	Analog Differential Input Pins. Full-scale range (A_{IN2^+} – A_{IN2^-}) is ±REFOUT2 voltage. These pins can be driven from V_{DD} to GND.
4, 5, 10, 29	GND	Ground. These pins and exposed pad (Pin 29) must be tied directly to a solid ground plane.
6, 7	A_{IN1^-}, A_{IN1^+}	Analog Differential Input Pins. Full-scale range (A_{IN1^+} – A_{IN1^-}) is ±REFOUT1 voltage. These pins can be driven from V_{DD} to GND.
9	$\overline{CNV}$	Conversion Start Input. A falling edge on $\overline{CNV}$ puts the internal sample-and-hold into the hold mode and starts a conversion cycle. $\overline{CNV}$ must be driven by a low jitter clock as shown in the Typical Application on the back page. The $\overline{CNV}$ pin is unaffected by the CMOS/LVDS pin.
11	REFRTN1	Reference Buffer 1 Output Return. Bypass REFRTN1 to REFOUT1. Do not tie the REFRTN1 pin to the ground plane.
12	REFOUT1	Reference Buffer 1 Output. An onboard buffer nominally outputs 4.096 V to this pin. This pin is referred to REFRTN1 and should be decoupled closely to the pin (no vias) with a 0.1 µF (X7R, 0402 size) capacitor and a 10 µF (X5R, 0805 size) ceramic capacitor in parallel. The internal buffer driving this pin may be disabled by grounding the REFINT pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25 V to V_{DD}.
13	VBYP1	Bypass this internally supplied pin to ground with a 1 µF ceramic capacitor. The nominal output voltage on this pin is 1.6 V.
14	OV_{DD}	I/O Interface Digital Power. The range of OV_{DD} is 1.71 V to 2.5 V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8 V or 2.5 V, LVDS: 2.5 V). Bypass OV_{DD} to OGND with a 0.1 µF capacitor.
15, 16	$SDO1^+$, $SDO1^-$	Channel 1 Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. In CMOS mode, the result is output on $SDO1^+$. The logic level is determined by OV_{DD}. Do not connect $SDO1^-$. In LVDS mode, the result is output differentially on $SDO1^+$ and $SDO1^-$. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA).
17, 18	$CLKOUT^+$, $CLKOUT^-$	Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. In CMOS mode, the skew-matched clock is output on $CLKOUT^+$. The logic level is determined by OV_{DD}. Do not connect $CLKOUT^-$. For low throughput applications using SCK to latch the SDO output, $CLKOUT^+$ can be disabled by tying $CLKOUT^-$ to OV_{DD}. In LVDS mode, the skew-matched clock is output differentially on $CLKOUT^+$ and $CLKOUT^-$. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
19, 20	$SDO2^+$, $SDO2^-$	Channel 2 Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. In CMOS mode, the result is output on $SDO2^+$. The logic level is determined by OV_{DD}. Do not connect $SDO2^-$. In LVDS mode, the result is output differentially on $SDO2^+$ and $SDO2^-$. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA).
21, 22	SCK^+, SCK^-	Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. In CMOS mode, drive SCK^+ with a single-ended clock. The logic level is determined by OV_{DD}. Do not connect SCK^-. In LVDS mode, drive SCK^+ and SCK^-. with a differential clock. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (ADC).
23	OGND	I/O Ground. This ground must be tied to the ground plane at a single point. OV_{DD} is bypassed to this pin.
24	VBYP2	Bypass this internally supplied pin to ground with a 1 µF ceramic capacitor. The nominal output voltage on this pin is 1.6 V
25	$\overline{CMOS}$/LVDS	I/O Mode Select. Ground this pin to enable CMOS mode, tie to OV_{DD} to enable LVDS mode. Float this pin to enable low power LVDS mode.
26	REFOUT2	Reference Buffer 2 Output. An onboard buffer nominally outputs 4.096 V to this pin. This pin is referred to REFRTN2 and should be decoupled closely to the pin (no vias) with a 0.1 µF (X7R, 0402 size) capacitor and a 10 µF (X5R, 0805 size) ceramic capacitor in parallel. The internal buffer driving this pin may be disabled by grounding the REFINT pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25 V to V_{DD}.
27	REFRTN2	Reference Buffer 2 Output Return. Bypass REFRTN2 to REFOUT2. Do not tie the REFRTN2 pin to the ground plane.
28	REFINT	Reference Buffer Output Enable. Tie to V_{DD} when using the internal reference. Tie to ground to disable the internal REFOUT1 and REFOUT2 buffers for use with external voltage references. This pin has a 500 k internal pull-up to V_{DD}.
29	Exposed Pad	Ground. Solder this pad to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2 = 4.096 V, f_{SMPL} = 5 Msps, unless otherwise noted. 1 LSB = 2 • REFOUT1,2/2^{12}.

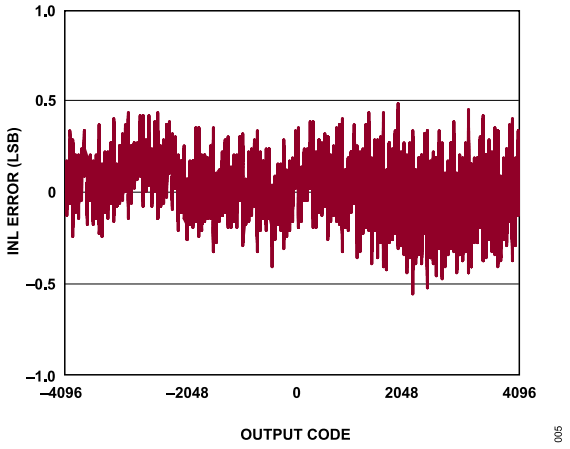


Figure 6. Integral Nonlinearity vs. Output Code

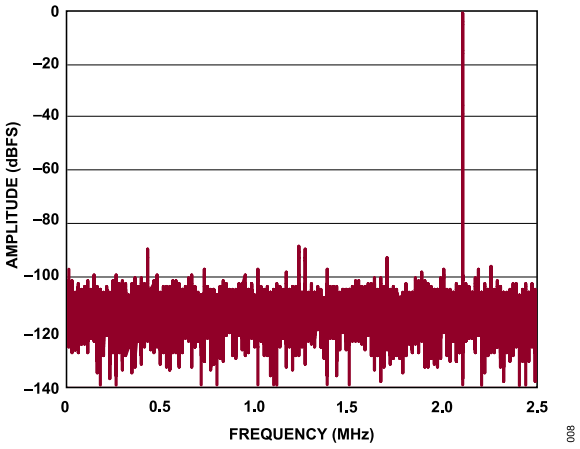


Figure 9. 16 k Point FFT, f_S = 5 Msps, f_{IN} = 2.2 MHz

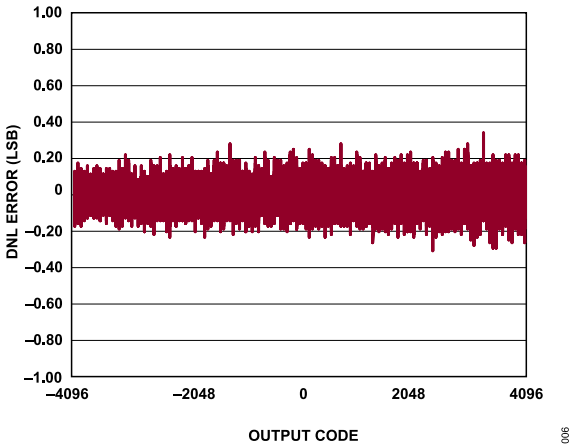


Figure 7. Differential Nonlinearity vs. Output Code

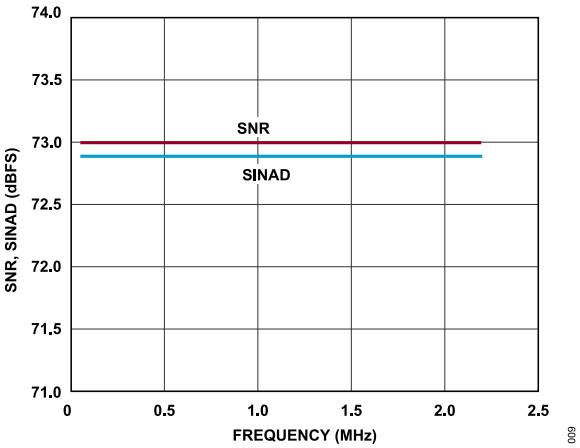


Figure 10. SNR, SINAD vs. Input Frequency (50 kHz to 2.2 MHz)

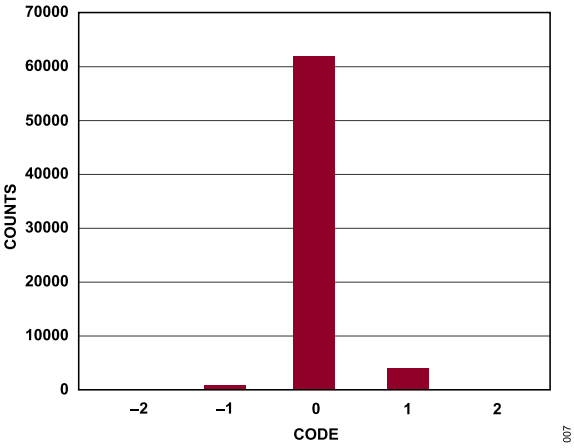


Figure 8. DC Histogram

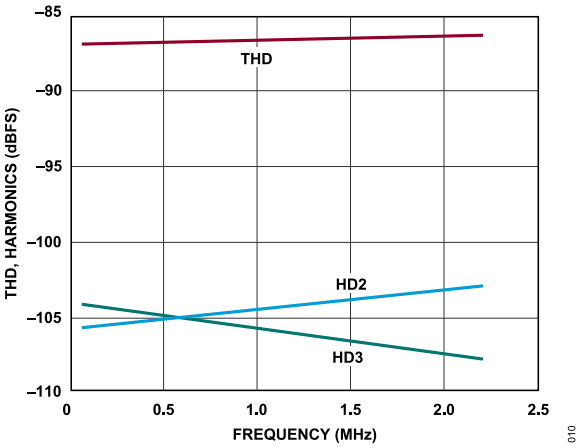


Figure 11. THD, Harmonics vs. Input Frequency (50 kHz to 2.2 MHz)

TYPICAL PERFORMANCE CHARACTERISTICS

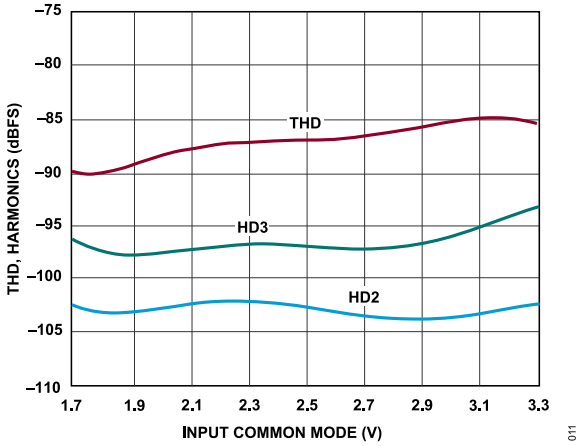


Figure 12. THD, Harmonics vs. Input Common Mode (100 kHz to 2.2 MHz)

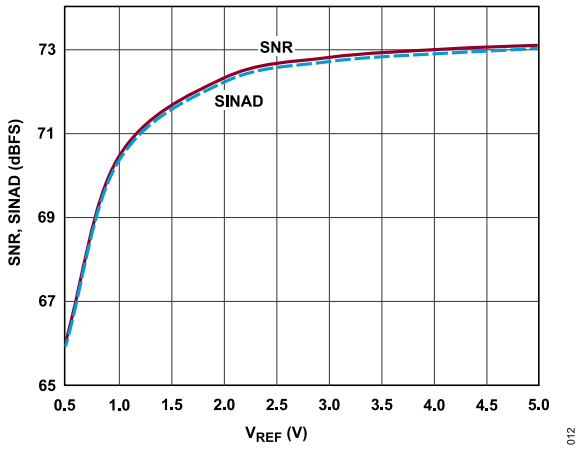


Figure 13. NR, SINAD vs. Reference Voltage, f_{IN} = 500 kHz

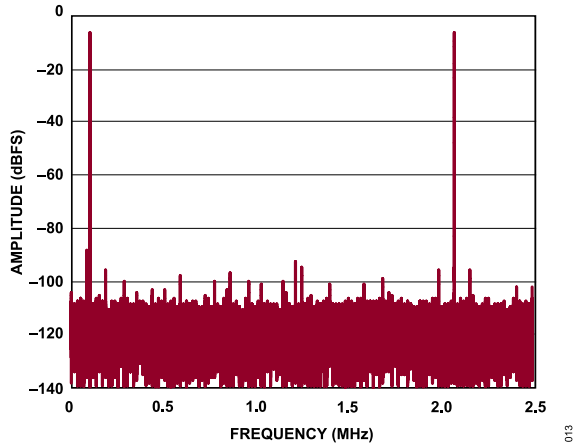


Figure 14. 32 k Point FFT, IMD, f_S = 5 Msps, V_{IN}^+ = 100 kHz, V_{IN}– = 2.2 MHz

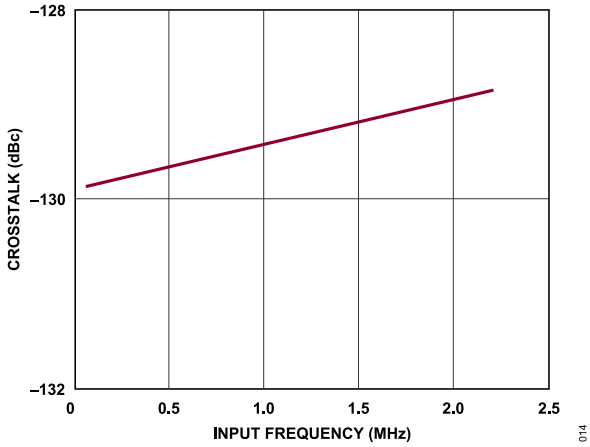


Figure 15. Crosstalk vs. Input Frequency

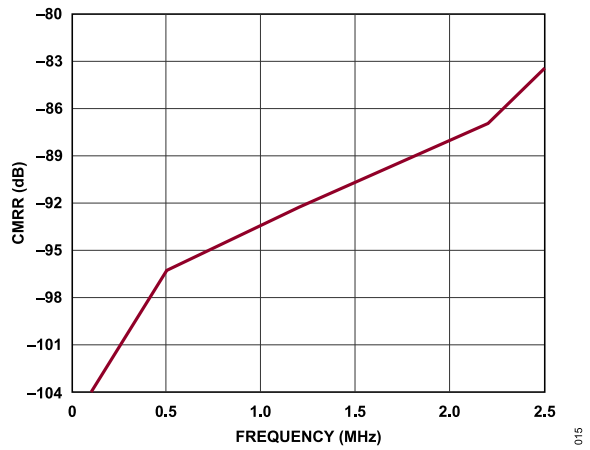


Figure 16. CMRR vs. Input Frequency

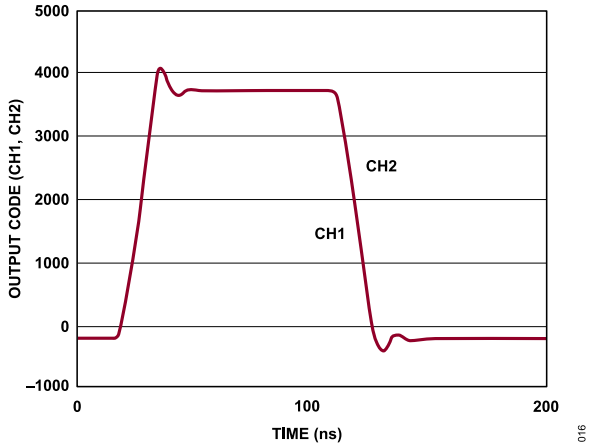


Figure 17. Output Match with Simultaneous Input Steps at CH1, CH2

TYPICAL PERFORMANCE CHARACTERISTICS

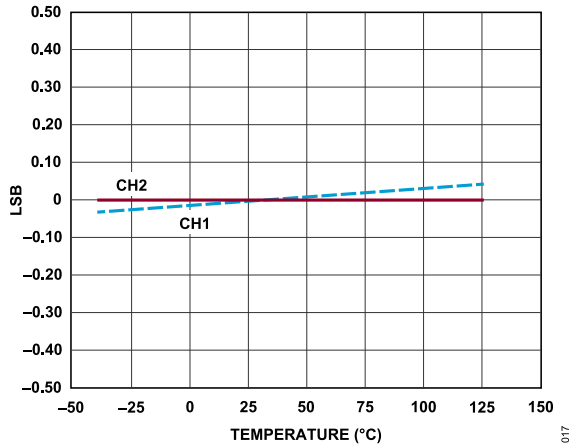


Figure 18. Offset Error vs. Temperature

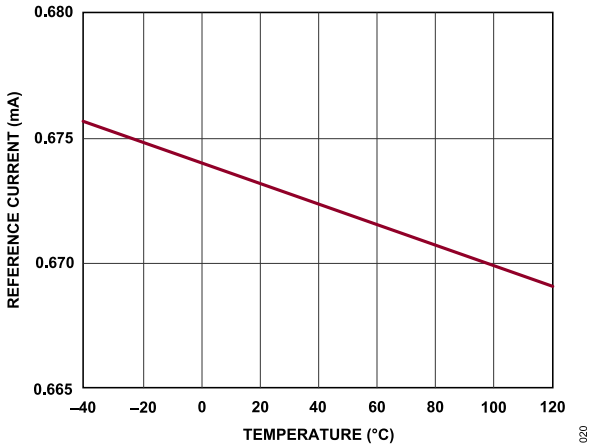


Figure 21. Reference Current vs. Temperature, V_{REF} = 4.096 V

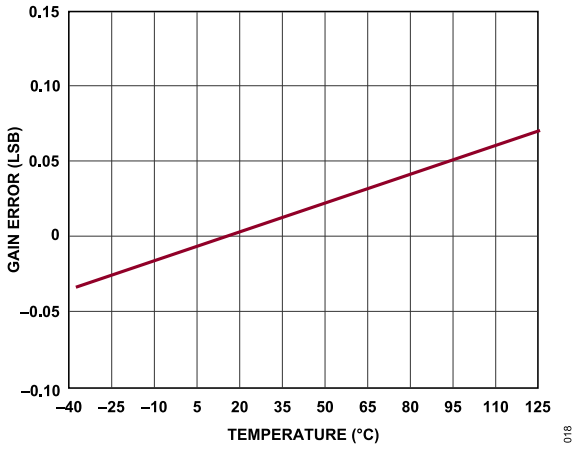


Figure 19. Gain Error vs. Temperature

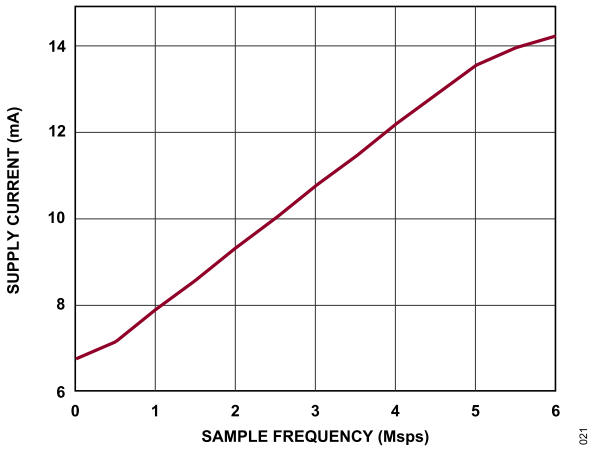


Figure 22. Supply Current vs. Sample Frequency

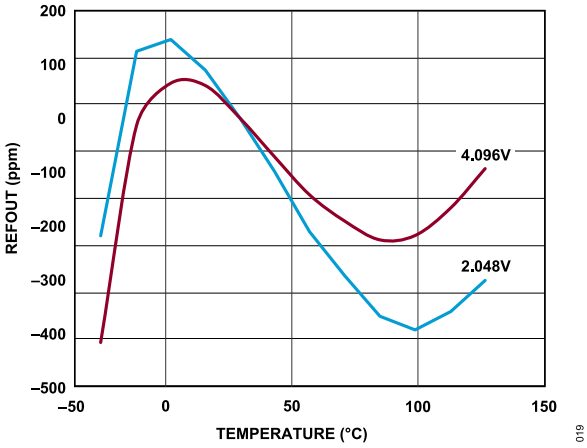


Figure 20. REFOUT1,2 Output vs. Temperature

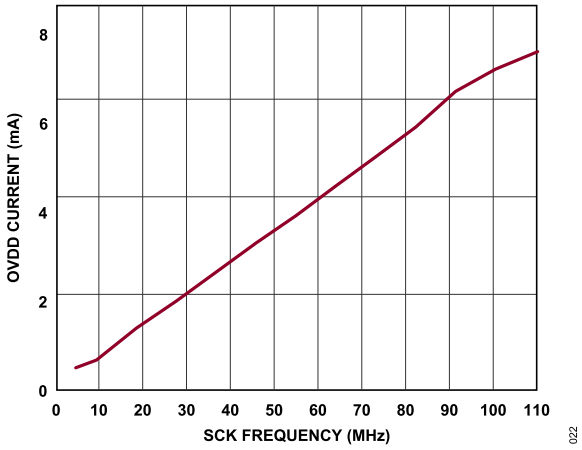


Figure 23. OV_{DD} Current vs. SCK Frequency, C_{LOAD} = 10 pF

APPLICATIONS INFORMATION

OVERVIEW

The LTC2323-12 is a low noise, high speed 12-bit + sign dual successive approximation register (SAR) ADC with differential inputs and wide input common mode range. The flexible analog inputs support fully differential, pseudo-differential bipolar and pseudo-differential unipolar drive without requiring any hardware configuration. The MSB of the 12-bit + sign two's complement output indicates the sign of the differential analog input voltage.

The ADC's transfer function provides 13-bits of resolution across the full-scale span of 2 • REFOUT, as shown in Figure 24. If the analog input spans less than this full-scale, such as in the case of pseudo-differential drive, the ADC provides 12-bits of resolution across this reduced span, with the additional benefit of digitizing over- and underrange conditions, as shown in Table 10. This unique feature is particularly useful in control loop applications.

CONVERTER OPERATION

The LTC2323-12 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A_{IN+} and A_{IN}– to sample the differential analog input voltage, as shown in Figure 25. A falling edge on the $\overline{CNV}$ pin initiates a conversion. During the conversion phase, the 13-bit CDAC is sequenced through a successive approximation algorithm for each input SCK pulse, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REFOUT}/2$, $V_{REFOUT}/4$ … $V_{REFOUT}/4096$) using a differential comparator. At the end of conversion, a CDAC output approximates the sampled analog input. The ADC control logic then prepares the 13-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2323-12 digitizes the full-scale voltage of 2 • REFOUT into 2^{13} levels, resulting in an LSB size of 1mV with REFBUF = 4.096 V. The ideal transfer function is shown in Figure 24. The output data is in 2's complement format. When driven by fully differential inputs, the transfer function spans 2^{13} codes. When driven by pseudo-differential inputs, the transfer function spans 2^{12} codes.

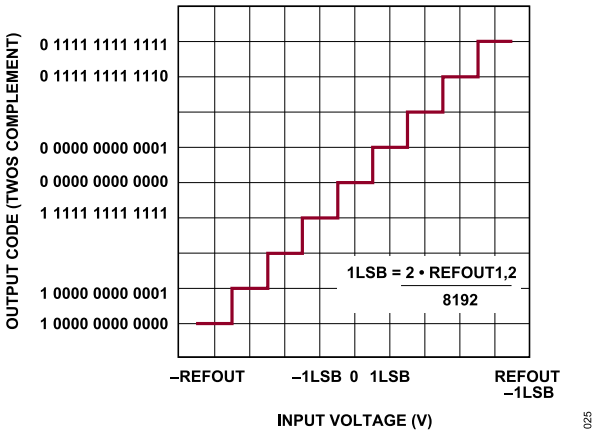


Figure 24. LTC2323-12 Transfer Function

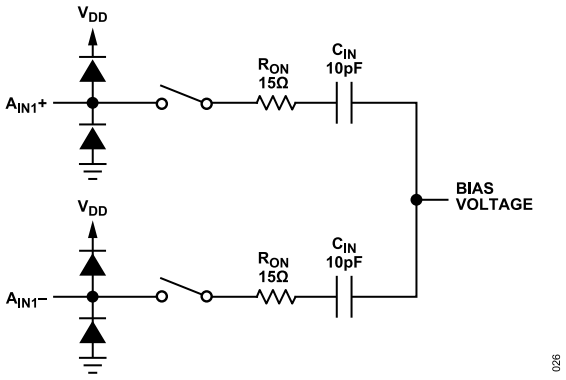


Figure 25. The Equivalent Circuit for the Differential Analog Input of the LTC2323-12

APPLICATIONS INFORMATION

Table 10. Code Ranges for the Analog Input Operational Modes

Mode	Span (V_{IN+} – V_{IN-})	Min Code	Max Code
Fully Differential	–REFOUT to +REFOUT	1 0000 0000 0000	0 1111 1111 1111
Pseudo-Differential Bipolar	–REFOUT/2 to +REFOUT/2	1 1000 0000 0000	0 0111 1111 1111
Pseudo-Differential Unipolar	0 to REFOUT	0 0000 0000 0000	0 1111 1111 1111

Analog Input

The differential inputs of the LTC2323-12 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2323-12 digitizes the difference voltage between the A_{IN+} and A_{IN}– pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between V_{DD} and GND. The LTC2323-12 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2323-12 can be modeled by the equivalent circuit shown in Figure 25. The back-to-back diodes at the inputs form clamps that provide ESD protection. In the acquisition phase, 10 pF (C_{IN}) from the sampling capacitor in series with approximately 15 Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the C_{IN} capacitors during acquisition.

Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2323-12. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other A_{IN} pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2323-12 flexibility handles both pseudo-differential unipolar and bipolar signals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically $V_{REF}/2$, and applying a signal to the other A_{IN} pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 26, and the corresponding transfer function in Figure 27. The fixed analog input pin need not be set at $V_{REF}/2$, but at some point within the V_{DD} rails allowing the alternate input to swing symmetrically around this voltage. If the input signal (A_{IN+} – A_{IN-}) swings beyond ±REFOUT/2, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other A_{IN} pin. In this case, the analog input swings between ground and V_{REF} yielding unipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 28, and the corresponding transfer function in Figure 29. If the input signal (A_{IN+} – A_{IN-}) swings negative, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

APPLICATIONS INFORMATION

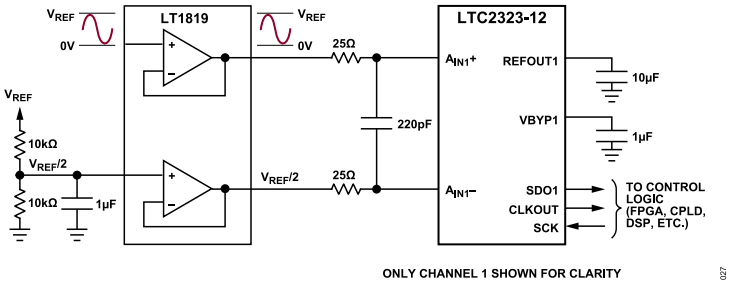


Figure 26. Pseudo-Differential Bipolar Application Circuit

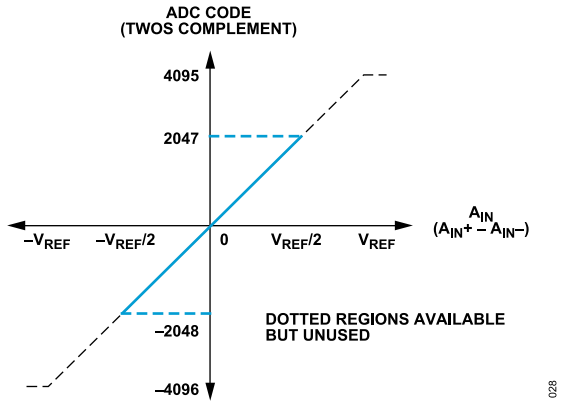


Figure 27. Pseudo-Differential Bipolar Transfer Function

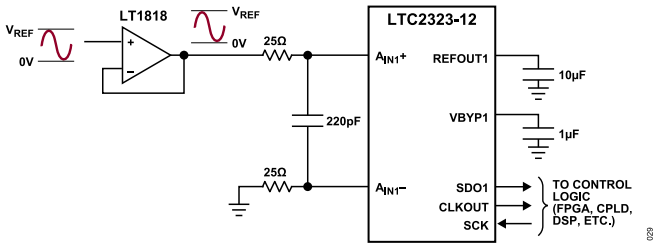


Figure 28. Pseudo-Differential Unipolar Application Circuit

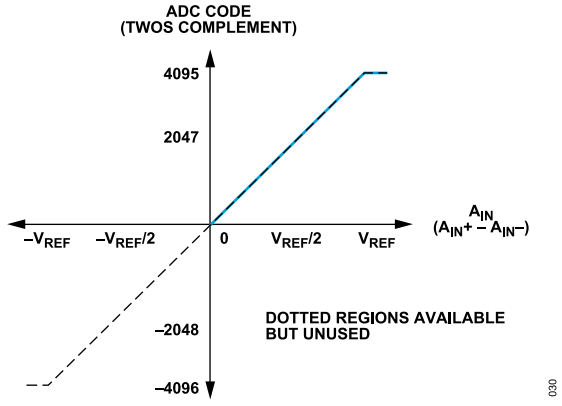


Figure 29. Pseudo-Differential Unipolar Transfer Function

APPLICATIONS INFORMATION

Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2323-12, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 30. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

Fully-Differential Inputs

To achieve the full distortion performance of the LTC2323-12, a low distortion fully-differential signal source driven through the LT1819 configured as two unity-gain buffers, as shown in Figure 31, can be used. This circuit achieves the full data sheet THD specification of –85 dB at input frequencies of 500 kHz and less. Data sheet typical performance curves taken at higher frequencies used a harmonic rejection filter between the ADC and the signal source to eliminate the op amp as the dominant source of distortion.

The fully-differential configuration yields an analog input span (A_{IN+} – $A_{IN–}$) of ±REFOUT. In this configuration, the input signal is driven on each AIN pin, typically at equal spans but opposite polarity. This yields a high common mode rejection on the input signals. The common mode voltage of the analog input can be anywhere within the V_{DD} input range, but will be limited by the peak swing of the full-range input signal. For example, if the internal reference is used with V_{DD} = 5 V_{DC}, the full-range input span will be ±4.096 V. Half of the input span is typically driven on each AIN pin, yielding a signal span for each AIN pin of 4.096 V_{P-P}. This leaves ~0.9 V of common mode variation tolerance. When using external references, it is possible to increase common mode tolerance by compressing the ADC full-range codes into a tighter range. For example, using an external 2.048 V reference with V_{DD} = 5 V the total span would be ±2.048 V and each AIN span would be limited to 2.048 V_{P-P} allowing a common mode range of ~3 V. Compressing the input span would incur a SNR penalty of approximately 1 dB. Input span compression may be useful if single-supply analog input drivers are used which cannot swing rail-to-rail. The fully-differential configuration is illustrated in Figure 32, with the corresponding transfer function illustrated in Figure 33.

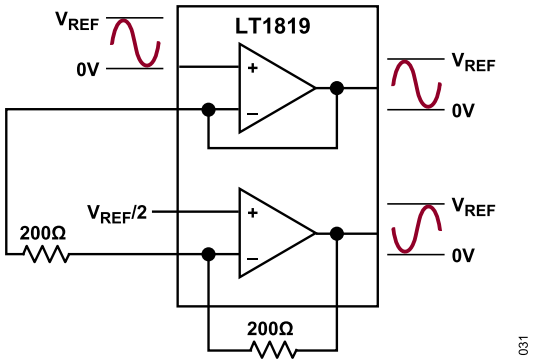


Figure 30. Single-Ended to Differential Driver

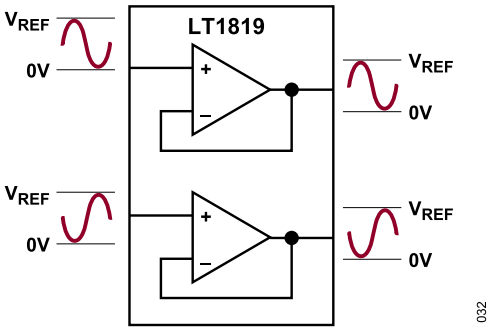


Figure 31. LT1819 Buffering a Fully-Differential Signal Source

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2323-12 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike when during acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2323-12. The amplifier provides low output impedance to minimize gain error and allow for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

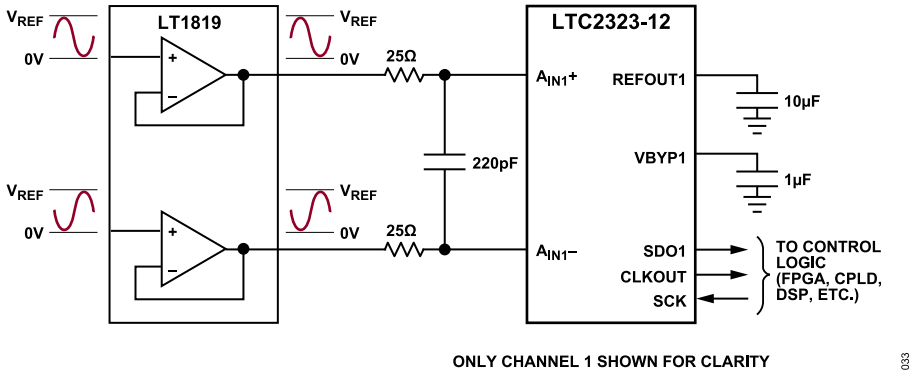


Figure 32. Fully-Differential Application Circuit

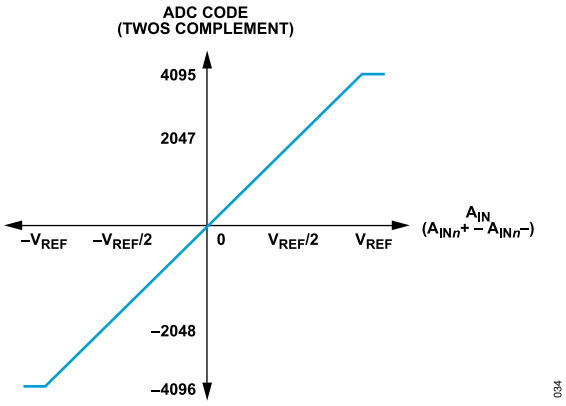


Figure 33. Fully-Differential Transfer Function

APPLICATIONS INFORMATION

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 34 is sufficient for many applications.

The input resistor divider network, sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 110 MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

ADC REFERENCE

Internal Reference

The LTC2323-12 has an on-chip, low noise, low drift (20 ppm/°C max), temperature compensated bandgap reference. It is internally buffered and is available at REFOUT1,2 (Pins 12, 26). The reference buffer gains the internal reference voltage to 4.096 V for supply voltages V_{DD} = 5 V and to 2.048 V for V_{DD} = 3.3 V. Bypass REFOUT1,2 to REFRTN1,2 with the parallel combination of a 0.1 µF (X7R, 0402 size) capacitor and a 10 µF (X5R, 0805 size) ceramic capacitor to compensate the reference buffer and minimize noise. The 0.1 µF capacitor should be as close as possible to the LTC2323-12 package to minimize wiring inductance. Tie the REFINT pin to V_{DD} to enable the internal reference buffer.

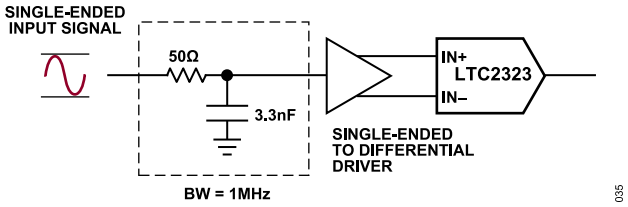


Figure 34. Input Signal Chain

Table 11. Reference Configurations and Ranges

Reference Configuration	V_{DD}	REFINT Pin	REFOUT1,2 Pin	Differential Input Range
Internal Reference	5 V	5 V	4.096 V	±REFOUT
External Reference	5 V	0 V	1.25 V to V_{DD}	±REFOUT
Internal Reference	3.3 V	3.3 V	2.048 V	±REFOUT
External Reference	3.3 V	0 V	1.25 V to V_{DD}	±REFOUT

APPLICATIONS INFORMATION

External Reference

The internal reference buffer can also be overdriven from 1.25 V to 5 V with an external reference at REFOUT1,2 as shown in Figure 36 and Figure 37. To do so, REFINT must be grounded to disable the reference buffer. A 55 k internal resistance loads the REFOUT1,2 pins when the reference buffer is disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT1,2. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5 V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a parallel combination of a 0.1 µF (X7R, 0402 size) ceramic capacitor and a 10 µF ceramic capacitor (X5R, 0805 size) close to each of the REFOUT1,2 and REFRTN1,2 pins.

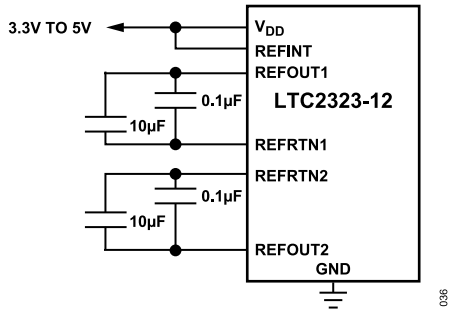


Figure 35. LTC2323-12 Internal Reference Circuit

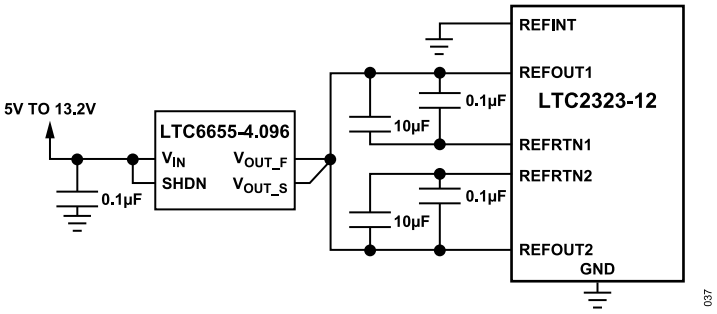


Figure 36. LTC2323-12 with a Shared External Reference Circuit

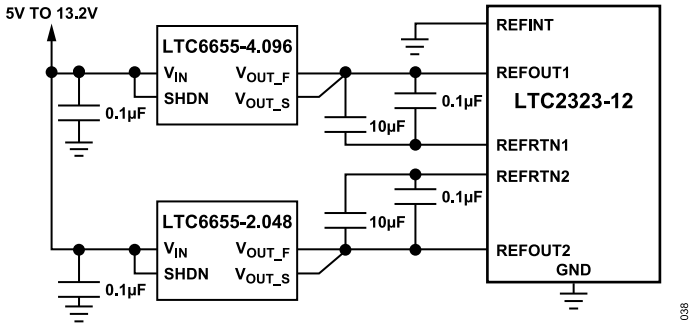


Figure 37. LTC2323-12 with Different External Reference Voltages

APPLICATIONS INFORMATION

Internal Reference Buffer Transient Response

The REFOUT1,2 pins of the LTC2323-12 draw charge (Q_{CONV}) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REF} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of REFOUT1,2 depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 38 , I_{REFBUF} quickly goes from approximately ~75 µA to a maximum of 500 µA for REFOUT1,2 = 5 V at 5 Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT1,2 will affect the accuracy of the output code. Due to the one-cycle conversion latency, the first conversion result at the beginning of a burst sampling period will be invalid. If an external reference is used to overdrive REFOUT1,2 the fast settling LTC6655 reference is recommended.

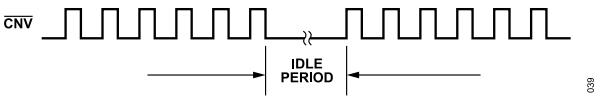


Figure 38. $\overline{CNV}$ Waveform Showing Burst Sampling

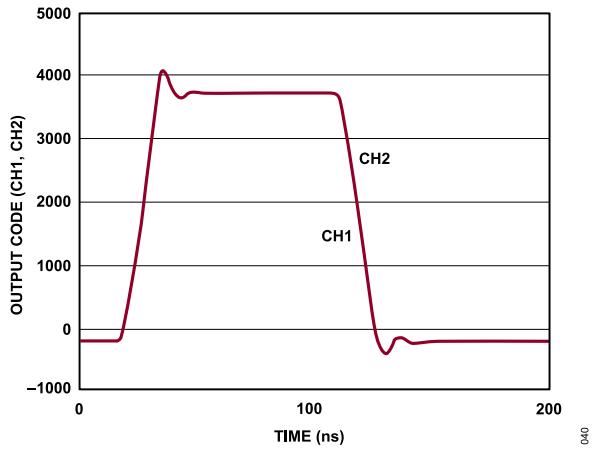


Figure 39. Transient Response of the LTC2323-12

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2323-12 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling frequency. Figure 40 shows that the LTC2323-12 achieves a typical SINAD of 72.9 dB at a 5 MHz sampling rate with a 2.2 MHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 40 shows that the LTC2323-12 achieves a typical SNR of 73 dB at a 5 MHz sampling rate with a 2.2 MHz input.

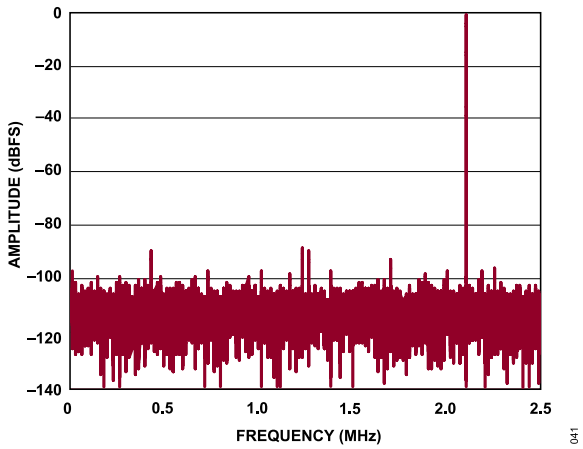


Figure 40. 16 k Point FFT of the LTC2323-12

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N^2}}{V1} \quad (1)$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

APPLICATIONS INFORMATION

POWER CONSIDERATIONS

The LTC2323-12 requires two power supplies: the 5 V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2323-12 to communicate with any digital logic operating between 1.8 V and 2.5 V. When using LVDS I/O, the OV_{DD} supply must be set to 2.5 V.

Power Supply Sequencing

The LTC2323-12 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2323-12 has a power-on-reset (POR) circuit that will reset the LTC2323-12 at initial power-up or whenever the power supply voltage drops below 2 V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10 ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

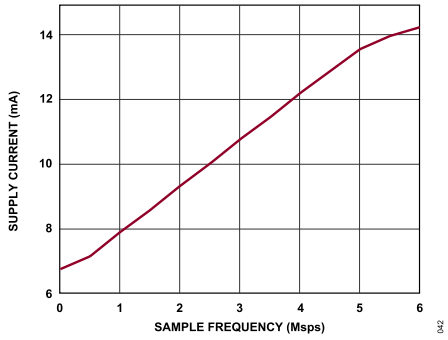


Figure 41. Power Supply Current of the LTC2323-12 Versus Sampling Rate

APPLICATIONS INFORMATION

TIMING AND CONTROL

$\overline{CNV}$ Timing

A rising edge on $\overline{CNV}$ initiates the acquisition phase and puts the internal sample-and-hold into the sample mode. A falling edge on $\overline{CNV}$ puts the internal sample-and-hold into the hold mode and starts a conversion cycle. The $\overline{CNV}$ pulse must be at least 35 ns wide for proper operation. $\overline{CNV}$ must be driven by a fast low jitter signal with a fall time from OV_{DD} to below 100 mV of less than 1 ns. To achieve this fast falling edge, the distance from the $\overline{CNV}$ source to the $\overline{CNV}$ pin should be minimized. The trace for this pulse should be kept as narrow as possible and routed away from adjacent traces or planes to minimize capacitance. The drive strength of the gate driving the $\overline{CNV}$ line must be sufficient to yield a fast falling edge at the ADC pin to below 100 mV. We recommend the Typical Application on the back page, which uses a high speed flip-flop to generate the $\overline{CNV}$ pulse to the ADC, eliminating the effect of jitter from the FPGA. If jitter from the FPGA is not a concern, the flip-flop can be eliminated and replaced with an inverter such as the NC7SZ04P5X.

SCK Serial Data Clock Input

The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 105 MHz external clock must be applied at the SCK pin to achieve 5 Msps throughput.

CLKOUT Serial Data Clock Output

The CLKOUT output provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. For low throughput applications, $CLKOUT^+$ can be disabled by tying CLKOUT– to OV_{DD}.

Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2323-12, the SCK signal must be held high or low and a series of two $\overline{CNV}$ pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of $\overline{CNV}$ initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further $\overline{CNV}$ pulses are applied. The SCK rising edge will put the LTC2323-12 back into the operational (full-power) state. When in nap mode, two additional pulses will put the LTC2323-12 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2323-12 into operational mode. A 10 ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth $\overline{CNV}$ pulse. The fifth pulse will return the LTC2323-12 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive $\overline{CNV}$ pulses will cycle the LTC2323-12 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 42, Figure 43, Figure 44, and Figure 45 for more detailed timing information about sleep and nap modes.

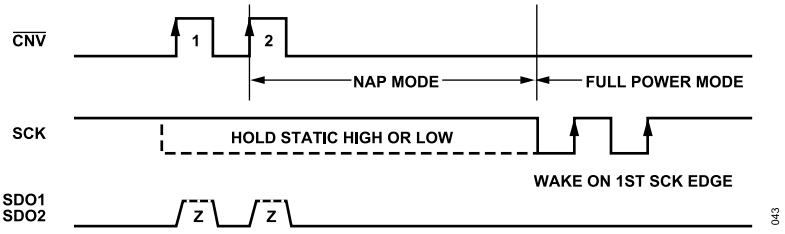


Figure 42. CMOS and LVDS Mode NAP and WAKE Using SCK

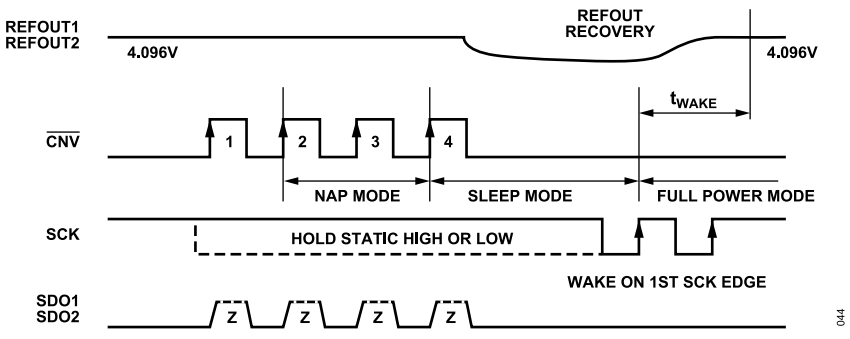


Figure 43. CMOS Mode SLEEP and WAKE Using SCK

APPLICATIONS INFORMATION

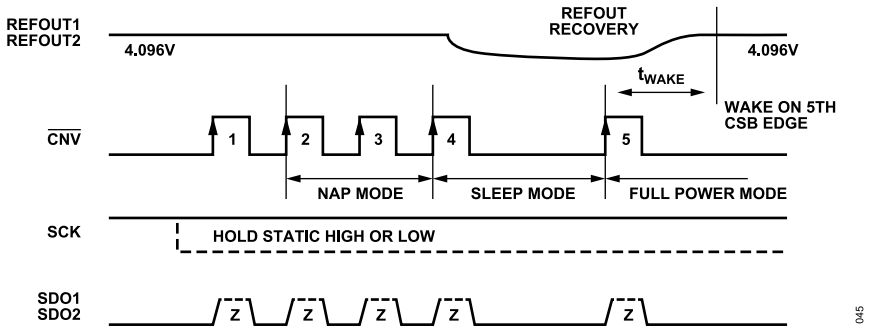


Figure 44. LVDS and CMOS Mode SLEEP and WAKE Using $\overline{CNV}$

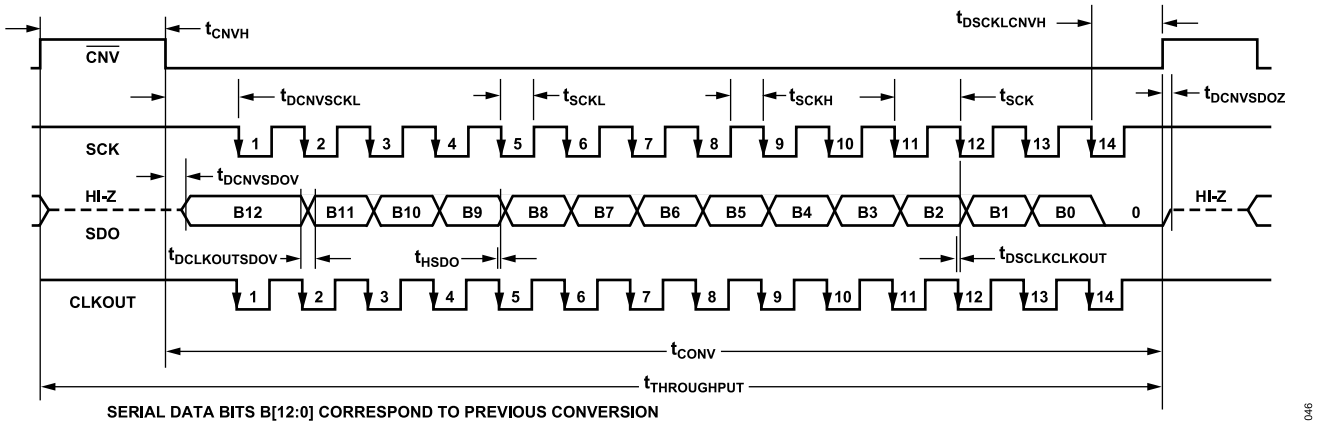


Figure 45. Detailed LTC2323-12 Timing Diagram

APPLICATIONS INFORMATION

DIGITAL INTERFACE

The LTC2323-12 features a serial digital interface that is simple and straight forward to use. The flexible OV_{DD} supply allows the LTC2323-12 to communicate with any digital logic operating between 1.8 V and 2.5 V. A 105 MHz external clock must be applied at the SCK pin to achieve 5 Msps throughput.

In addition to a standard CMOS SPI interface, the LTC2323-12 provides an optional LVDS SPI interface to support low noise digital design. The CMOS/LVDS pin is used to select the digital interface mode.

The falling edge of SCK outputs the conversion result MSB first on the SDO pins. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver.

In CMOS mode, use the $SDO1^+$, $SDO2^+$ and $CLKOUT^+$ pins as outputs. Use the SCK^+ pin as an input. Do not connect the $SDO1^-$, $SDO2^-$, SCK^- and $CLKOUT^-$ pins, as they each have internal pull-down circuitry to OGND.

In LVDS mode, use the $SDO1^+/SDO1^-$, $SDO2^+/SDO2^-$ and $CLKOUT^+/CLKOUT^-$ pins as differential outputs. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA). The SCK^+/SCK^- pins are differential inputs and must be terminated differentially by an external 100 Ω resistor at the receiver (ADC).

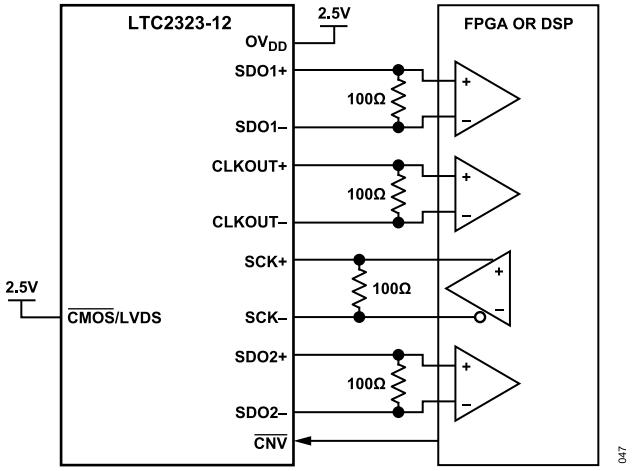


Figure 46. LTC2323 Using the LVDS Interface

APPLICATIONS INFORMATION

BOARD LAYOUT

To obtain the best performance from the LTC2323-12, a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

Recommended Layout

The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information, refer to the DC1996A-E, the evaluation kit for the LTC2323-12.

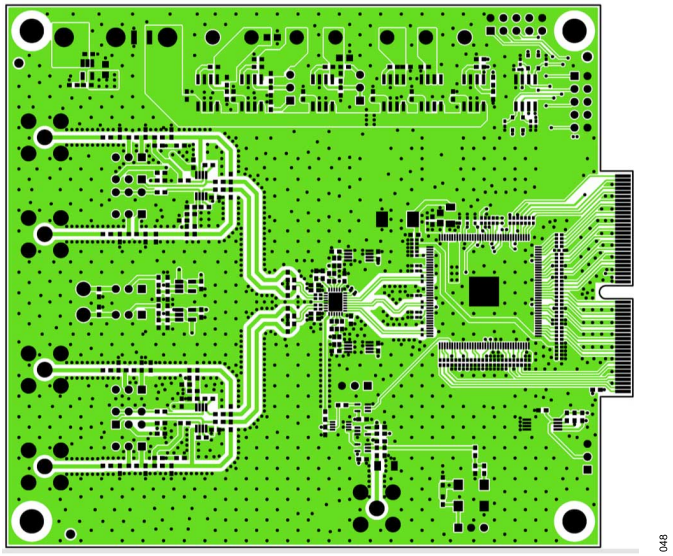


Figure 47. Layer 1, Top Layer

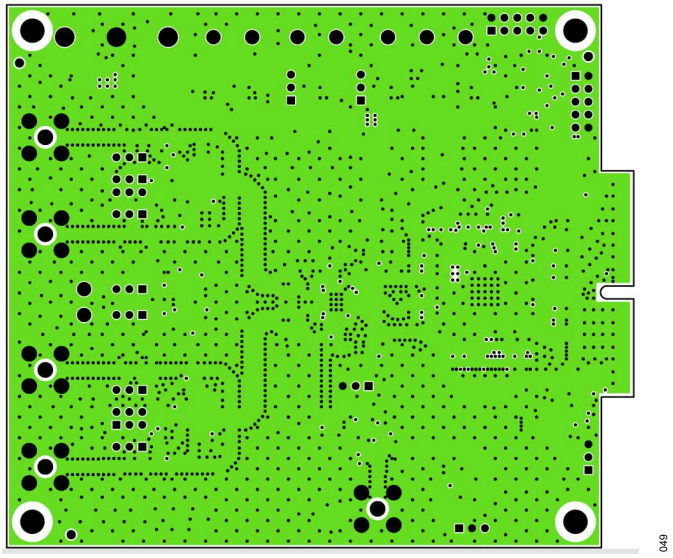


Figure 48. Layer 2, Ground Plane

APPLICATIONS INFORMATION

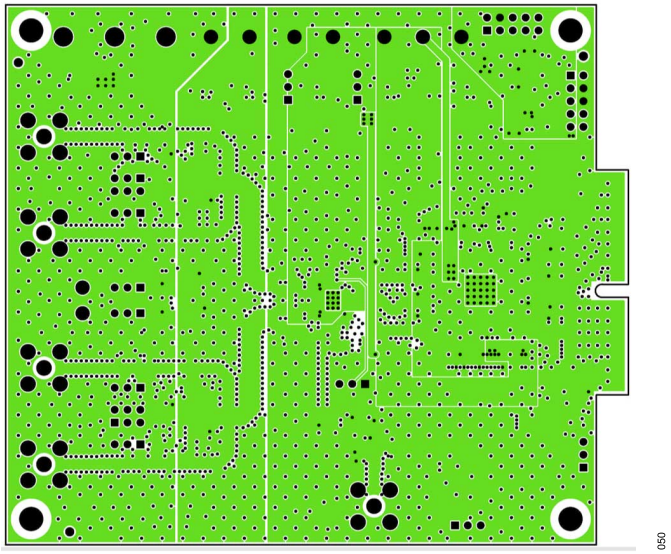


Figure 49. Layer 3, Power Plane

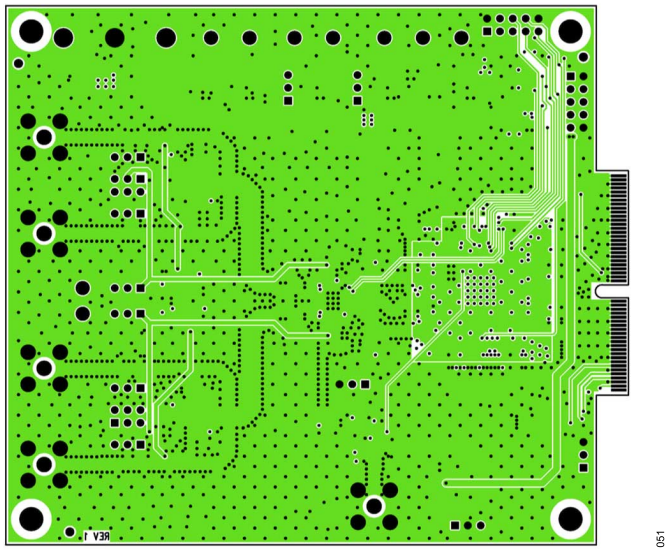


Figure 50. Layer 4, Bottom Layer

TYPICAL APPLICATION

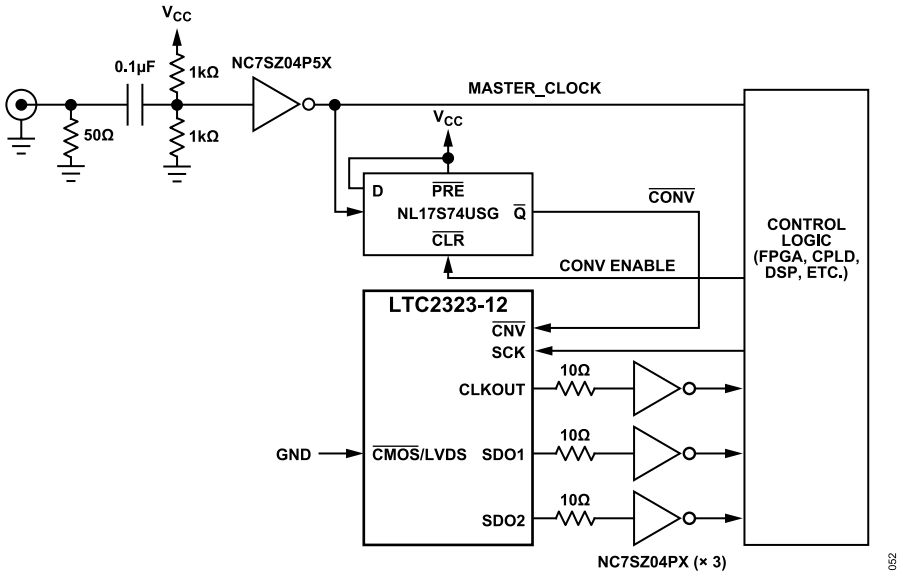


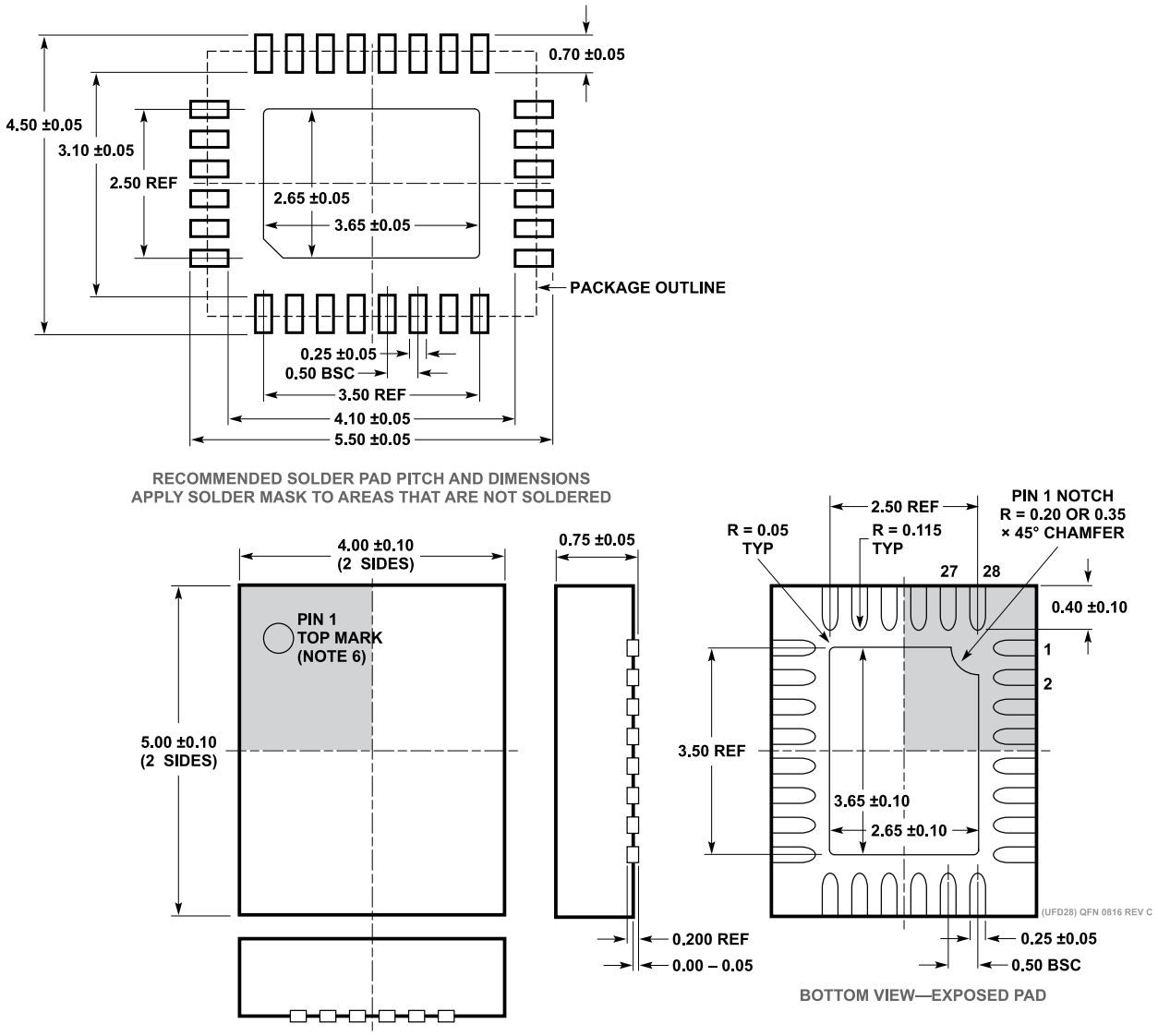
Figure 51. Low Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Retiming Flip-Flop

RELATED PARTS

Table 12.

Part Number	Description	Comments
ADCs		
LTC2323-16/LTC2323-14	16-/14-Bit, 5 Msps Simultaneous Sampling ADC	3.3 V/5 V Supply, Differential Input with Wide Input Common Mode Range, 45 mW/Ch, 4 mm × 5 mm QFN-28 Package
LTC2321-16/LTC2321-14/ LTC2321-12	16-/14-/12-Bit, Dual, 2 Msps Simultaneous Sampling ADC	3.3 V/5 V Supply, Differential Input with Wide Input Common Mode Range, 33 mW/Ch, 4 mm × 5 mm QFN-28 Package
LTC2314	14-Bit, 4.5 Msps Serial ADC	3 V/5 V Supply, 18 mW/31 mW, 20 ppm/°C Max Internal Reference, Unipolar Inputs, 8-Lead TSOT-23 Package
LTC2370-16/LTC2368-16/ LTC2367-16/LTC2364-16	16-Bit, 2 Msps/1 Msps/500 ksps/250 ksps Serial, Low Power ADC	2.5 V Supply, Pseudo-Differential Unipolar Input, 94 dB SNR, 5 V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4 mm × 3 mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2 Msps/1 Msps/500 ksps/250 ksps Serial, Low Power ADC	2.5 V Supply, Differential Input, 96.2 dB SNR, ±5 V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4 mm × 3 mm DFN-16 Packages
DACs		
LTC2632	Dual 12-/10-/8-Bit, SPI V_{OUT} DACs with Internal Reference	2.7 V to 5.5 V Supply Range, 10 ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 8-Pin ThinSOT™ Package
LTC2602/LTC2612/LTC2622	Dual 16-/14-/12-Bit SPI V_{OUT} DACs with External Reference	300 µA per DAC, 2.5 V to 5.5 V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
References		
LTC6655	Precision Low Drift, Low Noise Buffered Reference	5 V/4.096 V/3.3 V/3 V/2.5 V/2.048 V/1.25 V, 5 ppm/°C, 0.25 ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift, Low Noise Buffered Reference	5 V/4.096 V/3.3 V/3 V/2.5 V/2.048 V/1.25 V, 5 ppm/°C, 2.1 ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1818/LT1819	400 MHz, 2500 V/µs, 9 mA Single/Dual Operational Amplifiers	–85 dBc Distortion at 5 MHz, 6 nV/√Hz Input Noise Voltage, 9 mA Supply Current, Unity-Gain Stable
LT1806	325 MHz, Single, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps	–80 dBc Distortion at 5 MHz, 3.5 nV/√Hz Input Noise Voltage, 9 mA Supply Current, Unity-Gain Stable

OUTLINE DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 52. 28-Lead Plastic QFN (4 mm × 5 mm)
(Reference LTC DWG # 05-08-1712 Rev C)

OUTLINE DIMENSIONS

Updated: April 01, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC2323CUFD-12#PBF	0°C to +70°C	28-Lead QFN (4mm x 5mm x 0.75mm w/ EP)		05-08-1712
LTC2323CUFD-12#TRPBF	0°C to +70°C	28-Lead QFN (4mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1712
LTC2323HUFD-12#PBF	-40°C to +125°C	28-Lead QFN (4mm x 5mm x 0.75mm w/ EP)		05-08-1712
LTC2323HUFD-12#TRPBF	-40°C to +125°C	28-Lead QFN (4mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1712
LTC2323IUFD-12#PBF	-40°C to +85°C	28-Lead QFN (4mm x 5mm x 0.75mm w/ EP)		05-08-1712
LTC2323IUFD-12#TRPBF	-40°C to +85°C	28-Lead QFN (4mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1712

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
DC1996A-E	Evaluation Board
DC890B	Evaluation Board

[1] All models are RoHS compliant.