Click here to ask about the production status of specific part numbers.

MAX77958

Standalone USB Type-C and USB Power Delivery Controller

General Description

The MAX77958 is a robust solution for USB Type-C CC detection and power delivery (PD) protocol implementation. It detects connected accessories or devices by using Type-C CC detection and USB PD messaging. The IC protects against overvoltage and overcurrent, and detects moisture and prevents corrosion on the USB Type-C connector. The IC also has a D+/D- USB switch and BC1.2 detection to support legacy USB standards. It contains V_{CONN} switches for USB PD and an enable pin for an external V_{CONN} boost or buck converter.

The IC is compliant with USB Type-C Specification Release 1.3 and PD 3.0. It can be customized easily without affecting the compliance.

The IC has an I^2C master that can read and write to other devices in the system so that its firmware can configure related devices without the main processor's assistance. For example, it can configure an external charger based on BC1.2 detection, CC detection, and PD communication.

The IC has an interrupt output pin to report event detection and status changes. It also has an I^2C interface that system can use to read/write and configure internal registers.

The IC has nine configurable GPIOs that can be used for detection, as interrupts, and as the enable/disable pin for external devices, or as ADC inputs.

The IC is available in a 3.10mm x 2.65mm, 0.5mm pitch, wafer-level package (WLP).

Applications

- Smartphones
- Tablets
- Cameras
- Game Players
- Power Banks
- Industrial Equipment PoE to USB Type-C Adapters
- Handheld Devices
- Portable Devices
- Monitors
- Healthcare and Medical Devices
- Other USB Type-C Devices

Benefits and Features

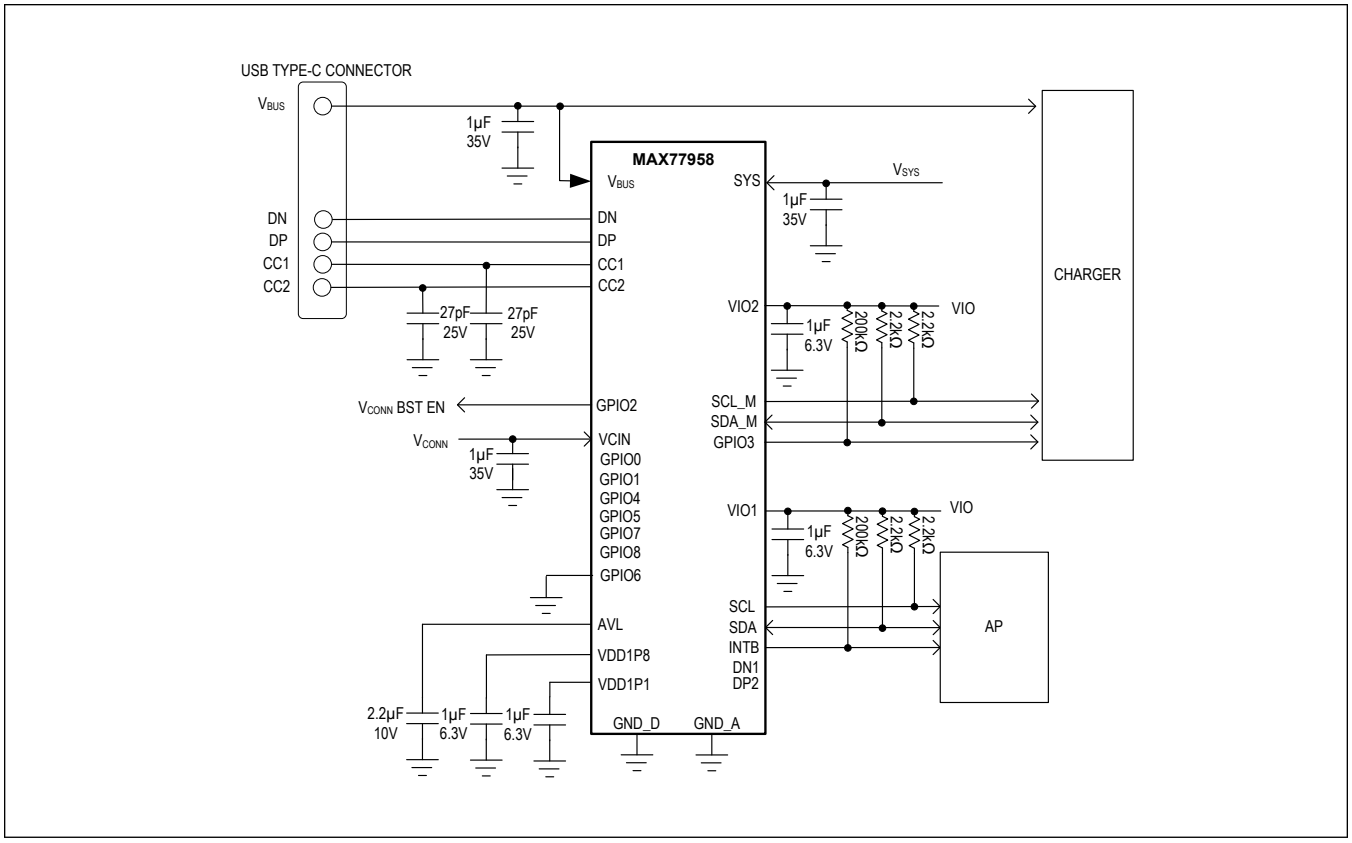
- Customizable Firmware
  - USB Compliant Default Embedded Firmware
  - Supports Customizable Actions on Events
  - Firmware Updates for Future Specification Revisions
- USB Type-C Support and USB-PD Support
  - USB Type-C Version 1.3 and PD3.0 Compliant
  - Mode Configuration: Sink/Source/Dual Role Port
  - Programmable Power Supply (PPS) Sink Support
  - Fast Role Swap (FRS) Initial Sink Support
  - Cable Orientation and Power Role Detection
  - Integrated V_{CONN} Switch with OCP
  - Support Try.Snk State
  - Audio and Debug Accessory Sink/Source Mode
- Supports BC1.2 Legacy/Proprietary Charger Detection
  - Integrated D+/D- Switches
- Moisture Detection/Corrosion Prevention
- High Voltage V_{BUS} (28V)
- Short to V_{BUS} Protection on CC Pins (22V)
- Dead Battery Support
- Dual Supply Inputs from SYS and V_{BUS}
- I^2C Programmable Configuration
- I^2C Master to Control External Charger or Direct Charge IC
- Nine Configurable GPIOs (GPIO6 for SID)
  - SuperSpeed Mux/Detection/IRQ
  - EN/DISABLE External Switches or Devices
- WLP 6x5 Bumps 0.5mm Pitch Package

***Ordering Information* appears at end of data sheet.**

19-100687; Rev 1; 4/20

maxim integrated™

Simplified Block Diagram



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Absolute Maximum Ratings

TOP and Interface Logic
- SYS to GND ..... -0.3V to +22.0V
- V_{BUS} to GND ..... -0.3V to +30.0V
- AVL to GND ..... -0.3V to +6.0V
- VDD1P8 to GND ..... -0.3V to +2.2V
- VIO1 to GND ..... -0.3V to +6.0V
- VIO2 to GND ..... -0.3V to +6.0V
- SCL, SDA, INTB to GND ..... -0.3V to VIO1 + 0.3V
- GND_A, GND_D to GND ..... -0.3V to +0.3V

USB Type-C
- VCIN to GND ..... -0.3V to +6.0V
- DN, DP, DN1, DP2 to GND..... -0.3V to +6.0V
- CC1, CC2 to GND ..... -0.3V to +22.0V
- VDD1P1 to GND ..... -0.3V to VDD1P8 + 0.3V
- SCL_M, SDA_M to GND .....-0.3V to VIO2 + 0.3V
- GPIO0, GPIO1, GPIO2, GPIO3, GPIO8 to GND -0.3V to VIO2 + 0.3V
- GPIO4, GPIO5, GPIO6, GPIO7 to GND ..-0.3V to VIO1 + 0.3V

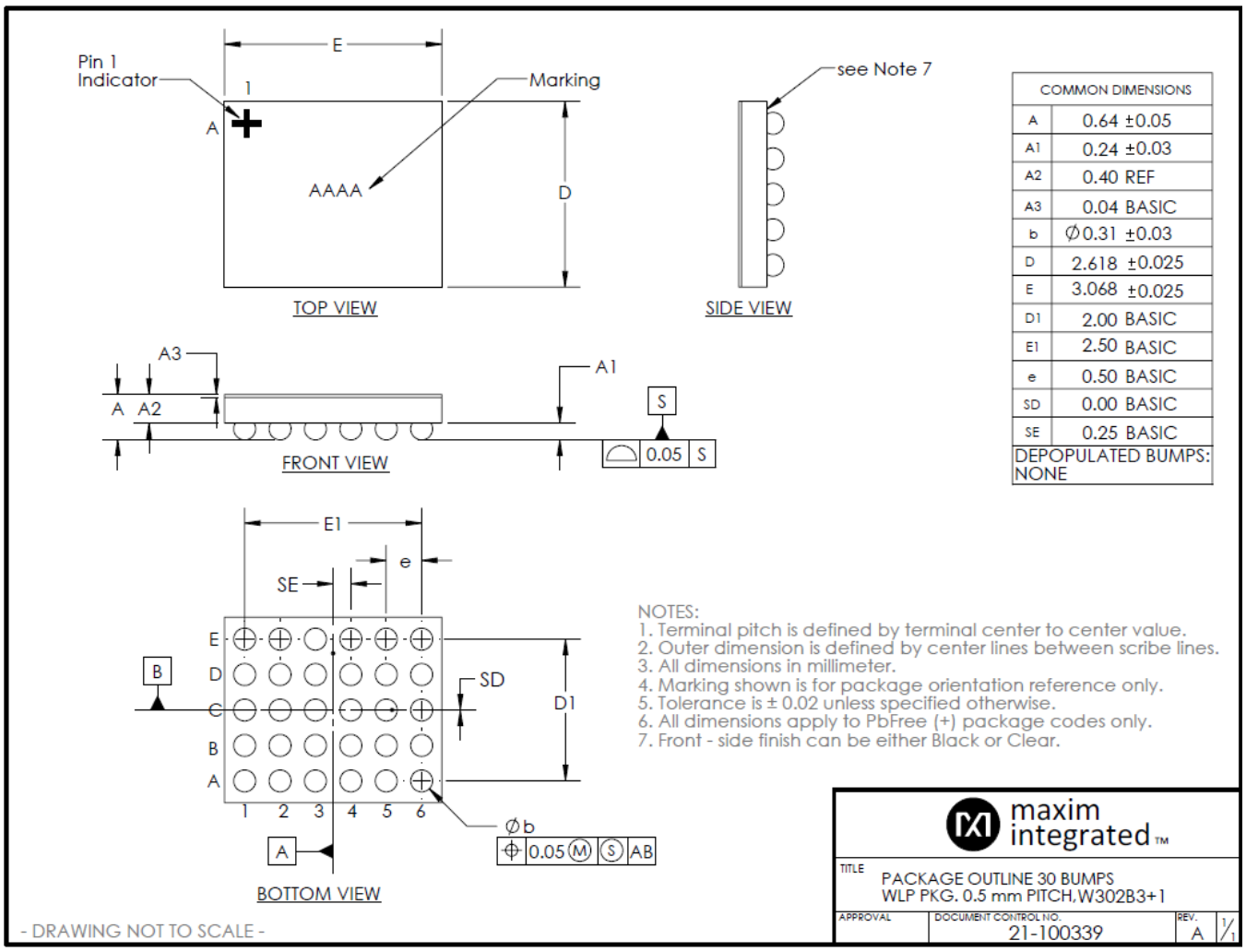
Thermal Absolute Maximum Rating
- Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 24.4mW/°C above +70°C.)..... 21.0mW to 24.4mW
- Operating Temperature Range .....-40°C to +85°C
- Storage Temperature Range.....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W302B3+1
Outline Number	21-100339
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	N/A



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.24 ±0.03
A2	0.40 REF
A3	0.04 BASIC
b	Ø0.31 ±0.03
D	2.618 ±0.025
E	3.068 ±0.025
D1	2.00 BASIC
E1	2.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC
DEPOPULATED BUMPS: NONE	

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS							
SYS Operating Voltage	V_{SYS}			AVL_{UVLOR}		+20	V
AVL UVLO Rising	AVL_{UVLOR}	AVL		2.6	2.7	2.8	V
AVL UVLO Falling	AVLUVLOF	AVL		2.4	2.5	2.6	V
AVL UVLO Hysteresis	AVLUVLOHYS	AVL			200		mV
AVL Operating Voltage	V_{AVL}			AVL_{UVLOF}		+5.5	V
SYS OV HR Rising	SYS_OV_HR_R	SYS		4.60	4.87	5.15	V
SYS OV HR Falling	SYS_OV_HR_F	SYS		4.40	4.71	5.05	V
SYS OV HR Hysteresis	SYS_OV_HR_H	SYS			160		mV
SYS OV LR Rising	SYS_OV_LR_R	SYS		3.60	3.87	4.15	V
SYS OV LR Falling	SYS_OV_LR_F	SYS		3.50	3.75	4.00	V
SYS OV LR Hysteresis	SYS_OV_LR_H	SYS			115		mV
SYS Factory Ship Supply Current	I_{FSHIP}	VIO1 = VIO2 = 0V, CCdetEn = 0, chgDetEn = 0,V_{BUS} = 0V	SYS = 4.2V		7		µA
			SYS = 8.4V		14		
			SYS = 12.6V		19		
		VIO1 = VIO2 = 0V, CCdetEn = 0, chgDetEn = 0,VBUS = 0V	SYS = 16.8V		25		
SYS Dead Battery Supply Current	$I_{DEADBAT}$	VIO1 = VIO2 = 0V, CCdetEn = 0, chgDetEn = 0,V_{BUS} = 0V	SYS = 4.2V, SYS_OV_HR		87		µA
			SYS = 8.4V		51		
			SYS = 12.6V		59		
			SYS = 16.8V		67		
SYS Shutdown Supply Current	I_{SHDN}	VIO1 = VIO2 = 0V, CCdetEn = 0, chgDetEn = 0, V_{BUS} = 0V	SYS = 4.2V, SYS_OV_HR		146		µA
			SYS = 8.4V		109		
			SYS = 12.6V		117		
			SYS = 16.8V		124		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYS Standby Supply Current	$I_{STANDBY}$	Sink mode, CCdetEn = 1, chgDetEn = 1, VIO1 = VIO2 = 1.8V, V_{BUS} = 0V	SYS = 4.2V, SYS_OV_LR		110		µA
			SYS = 4.2V, SYS_OV_HR		158		
			SYS = 8.4V		120		
			SYS = 12.6V		128		
			SYS = 16.8V		135		
V_{BUS} Operating Voltage	V_{BUS}			V_{BDET_R}		+28	V
V_{BUS} Detect Rising	V_{BDET_R}	550mV hysteresis	V_{BUS}	3.6	3.8	4.0	V
V_{BUS} Detect Falling	V_{BDET_F}	550mV hysteresis	V_{BUS}	2.95	3.25	3.55	V
V_{BUS} Detect Hysteresis	V_{BDET_H}	550mV hysteresis	V_{BUS}		525		mV
V_{BUS} Supply Current	$I_{STANDBY}$	V_{BUS} = 5V, VIO1 = 1.8V, VIO2 = 1.8V, CCdetEn = 1, sink only, STOP mode	V_{SYS} = 4.2V		150		µA
			V_{SYS} = 16.8V		192		
V_{BUS} Debounce	t_{VBDeb}			9	10	11	ms
VIO_OK	VIO_OK_LV_R	VIO1, VIO2, rising		1.0	1.30	1.65	V
	VIO_OK_LV_F	VIO1, VIO2, falling		0.8	1.0	1.4	
	VIO_OK_LV_H	VIO1, VIO2, hysteresis			225		mV
	VIO_OK_HV_R	VIO1, VIO2, rising		1.3	1.55	1.80	V
	VIO_OK_HV_F	VIO1, VIO2, falling		1.25	1.52	1.8	
	VIO_OK_HV_H	VIO1, VIO2, hysteresis			25		mV
	$t_{VIO\_OK\_DEB}$	Debounce			50		µs
Output Low Voltage INTB		I_{SINK} = 1mA				0.4	V
Output High Leakage INTB		V_{INTB} = 5.5V, T_A = +25°C		-1000	0	+1000	nA
		V_{INTB} = 5.5V, T_A = +85°C			100		
VDD_OK	VDD_OK_R	VDD1P8, rising		1.30	1.65	1.70	V
	VDD_OK_F	VDD1P8, falling		1.15	1.55	1.65	
	VDD_OK_H	VDD1P8, hysteresis			100		mv
INTERFACE / I²C INTERFACE AND INTERRUPT							
SCL, SDA Input Low Level		T_A = +25°C				0.3 x VIO1	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL, SDA Input High Level		T_A = +25°C	0.7 x VIO1			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 x VIO1		V
SCL, SDA Logic Input Current		SDA = SCL = 5.5V	-10		+10	µA
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
Output High Leakage INTB		V_{INTB} = 5.5V, T_A = +25°C	-1000		+1000	nA
INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		260			ns
CLK Low Period	t_{LOW}		500			ns
CLK High Period	t_{HIGH}		260			ns
Setup Time Repeated START Condition	$t_{SU;STA}$		260			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Valid Time	$t_{VD:DAT}$				450	ns
DATA Valid Acknowledge Time	$t_{VD:ACK}$				450	ns
Rise/Fall Time of SCL	t_{SCL}				120	ns
Rise/Fall Time of SDA	t_{SDA}				120	ns
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
Bus-Free Time Between STOP and START	t_{BUF}		500			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns
INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK High Period	t_{HIGH}		60			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Rise/Fall time of SCL	t_{SCL}		10		40	ns
Rise/Fall time of SDA	t_{SDA}		10		80	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Rise/Fall Time of SCL	t_{SCL}		20		80	ns
Rise/Fall Time of SDA	t_{SDA}		10		160	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
USB TYPE-C / CHARGER DETECTION						
BC1.2 State Timeout	t_{TMO}		180	200	220	ms
Data Contact Detect Timeout	t_{DCDtmo}	DCDCpl = 0b1 (default), DCDCpl = 0b0	700	800	900	ms
Primary to Secondary Timer	$t_{PDSDWait}$		27	35	39	ms
Charger Detection Debounce	t_{CDDeb}		45	50	55	ms
I_{WEAK} Current	I_{WEAK}		10	100	500	nA
R_{DM_DWN} Resistor	R_{DM_DWN}		14.25	20	24.8	kΩ
I_{DP_SRC} Current	I_{DP_SRC}/I_{DCD}	Accurate over 0V to 2.5V	-13	-10	-7	µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DM_SINK} Current	I_{DM_SINK}/I_{DAT_SINK}	Accurate over 0.15V to 3.6V	50	80	110	µA
V_{LGC} Threshold	V_{LGC}		1.62	1.7	1.9	V
V_{LGC} Hysteresis	V_{LGC_H}			0.015		V
V_{DAT_REF} Threshold	V_{DAT_REF}		0.25	0.32	0.4	V
V_{DAT_REF} Hysteresis	$V_{DAT\_REF\_H}$			0.015		V
OVDX Comparator Falling Threshold	V_{OVDX_THF}	Falling DP/DN threshold with respect to AVL	-40		+80	mV
OVDX Comparator Rising Threshold	V_{OVDX_THR}	Rising DP/DN threshold with respect to AVL	0		150	mV
DP/DN Overvoltage Debounce	$t_{OVDxDeb}$		90	100	110	µs
DN/DP Load Resistor	R_{USB}	Load resistor on DP/DN	3	6.1	12	MΩ
VD33 Voltage	$V_{DP/DM\_3p3VSRC}/V_{SRC33}$	Tested at zero load and at 200µA load	2.6	3.0	3.3	V
VSRC33ILIM Current Limit	$I_{LIMVSRC33}$	Force 1.6V on DP/DN, measure current		1.5	3	mA
VDN_SRC Voltage	V_{DN_SRC}/V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
VDP_SRC Voltage	V_{DP_SRC}/V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
USB TYPE-C / CC DETECTION						
CC Pin Voltage, in DFP 1.5A Mode	V_{CC_PIN}	Measured at CC pins with 126kΩ load, IDFP1.5_CC enable and V_{AVL} ≥ 2.6V	1.85			V
CC Pin Voltage, in DFP 3.0A Mode	VCC_PIN	Measured at CC pins with 126kΩ load, IDFP3.0_CC enable and AVL ≥ 3.65V	3.1			V
CC Pin Clamp Voltage	V_{CC_CLAMP}	60µA ≤ I_{CC} ≤ 600µA	0.88	1.1	1.32	V
CC UFP Pulldown Resistance	R_{PD_UFP}		-10%	5.1	+10%	kΩ
CC DFP Low-Power Mode	V_{DFPLP_CC}	AVL ≥ 2.6V, I_{DFPULP_CC} current source enabled, 1.1V	1.2			V
CC DFP Ultra-Low-Power Current Source	I_{DFPULP_CC}	Measured at CC = 0.5V	-10%	1	+10%	µA
		Measured at CC = 1.0V, T_A = +25°C	-10%	1	+10%	
		Measured at CC = 1.0V	-12%	1	+12%	
CC DFP 0.5A Current Source	$I_{DFP0.5\_CC}$		-20%	80	+20%	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC}$		-8%	180	+8%	µA
CC DFP 3A Current Source	I_{DFP3A_CC}		-8%	330	+8%	µA
CC RA RD Threshold	$V_{RA\_RD0.5}$		0.15	0.2	0.25	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC UFP 0.5A RD Threshold	$V_{UFP\_RD0.5}$		0.61	0.66	0.7	V
CC UFP 0.5A RD Hysteresis	$V_{UFP\_RD0.5\_H}$			0.015		V
CC UFP 1.5A RD Threshold	$V_{UFP\_RD1.5}$		1.16	1.23	1.31	V
CC UFP 1.5A RD Hysteresis	$V_{UFP\_RD1.5\_H}$			0.015		V
CC DFP V_{OPEN} Detect Threshold	V_{DFP_VOPEN}		1.5	1.575	1.65	V
CC DFP V_{OPEN} Detect Hysteresis	$V_{DFP\_VOPEN\_H}$			0.030		V
CC DFP V_{OPEN} With 3.0A Detect Threshold	$V_{DFP\_VOPEN3A}$	V_{AVL} ≥ 3.5V	2.45	2.6	2.75	V
CC DFP V_{OPEN} With 3.0A Detect Hysteresis	$V_{DFP\_VOPEN3A\_H}$	V_{AVL} ≥ 3.5V		0.030		V
V_{BUS} Discharge Value Threshold	V_{SAFE0V}	Falling voltage level where a connected UFP finds the V_{BUS} removed	0.6	0.67	0.75	V
V_{BUS} Discharge Value Hysteresis	V_{SAFE0V_h}	Rising hysteresis		40		mV
CC Pin Power-Up Time	$t_{ClampSwap}$	Max time allowed from removal of voltage clamp until a 5.1kΩ resistor attached			15	ms
CC Detection Debounce	t_{CCDeb}		100	119	200	ms
Type-C Debounce	t_{PDDeb}		10	15	20	ms
Type-C Quick Debounce	t_{QDeb}		0.9	1	1.1	ms
VSAFE0V Debounce	$t_{VSAFE0VDeb}$		9	10	11	ms
Type-C Error Recovery Delay	$t_{ErrorRecovery}$		25			ms
Type-C DRP Toggle Time	t_{DRP}		50	75	100	ms
DFP Duty Cycle at DRP		Programmable from 35% to 50% in 5% step, CCDRPPhase = 0b00		35		%
Type-C DRP Try	t_{DRPtry}		90	100	110	ms
DRP Transition Time	$t_{DRPTrans}$	Time for a role swap from DFP to UFP or the reverse is completed			1	ms
V_{CONN} Enable Time	$t_{VCONNON}$				2	ms
V_{CONN} Disable Time	$t_{VCONNOFF}$	Time from UFP detached or as directed by I^2C command until V_{CONN} is removed			35	ms
CC Pin Current Change Time	$I_{SINKADJ}$	Time from CC pin changes state in UFP mode until current drawn from DFP reaches a new value			60	ms
V_{BUS} On Time	t_{VBUSON}	Time from UFP is attached until V_{BUS} ON			275	ms

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BUS} Off Time	$t_{VBUSOFF}$	Time from UFP is detached until V_{BUS} reaches V_{SAFE0V}			650	ms
V_{BUS} Input Self-Discharge Resistance	$R_{VBUS\_SD\_USB}$			10		kΩ
CC1/2 Water Comp Threshold	V_{CC_Comp}	1.0V Comp	-8%	1.00	+8%	V
		0.8V Comp	-8%	0.8	+8%	
		0.6V Comp	-8%	0.6	+8%	
		0.4V Comp	-8%	0.4	+8%	
CC1/2 Water Comp Hysteresis	VCC_Comp_H			0.015		V
CC_OVP Threshold	CC_OVP	Rising	5.375	5.735	6.325	V
		Falling	5.175	5.670	6.275	
CC_OVP Hysteresis	CC_OVP_H			85		mV
USB TYPE-C / V_{CONN} Switch						
V_{CIN_PRES}	$V_{CIN\_PRES\_R}$	Rising	0.75	1.38	2.45	V
	$V_{CIN\_PRES\_F}$	Falling	0.45	0.75	1.75	
	$V_{CIN\_PRES\_H}$	Hysteresis		600		mV
	$t_{VCIN\_PRES\_DEB}$	Debounce		50		µs
V_{CIN_OK}	$CC\_V_{CIN\_OK\_R}$	Rising	2.40	2.75	3.00	V
	$CC\_V_{CIN\_OK\_F}$	Falling	2.35	2.72	3.00	
	$CC\_V_{CIN\_OK\_H}$	Hysteresis		30		mV
	$t_{VCIN\_OK\_DEB}$	Debounce		50		µs
V_{CONN} Source Requirements			3.0		5.5	V
V_{CONN} SW Ron	$R_{ONVCONNSW}$	VCIN = 5.0V, ICC = 0.5A		500	900	mΩ
OCP Accuracy		VCIN = 5.0V, T_A = +25°C	-40	-20		%
OCP_ShortCircuit Protection	I_{SCP}			700		mA
OCP Programmable Step	I_{STEP}	Programmable range is 200mA to 500mA		100		mA
OCP Interrupt Debounce Time T1	t_{Deb1}	From detecting OCP to generating INT		2		ms
Wait Time Before Turn Off T2	t_{Deb2}	From generating INT to turning OFF V_{CONN} switch		12		ms

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Startup Time At 90%		Time from V_{CONN} switch enable to CC settled at 90% of final value with VCIN = 3.0V			0.05	0.2	ms
Turn Off Time At 10%		Time from V_{CONN} switch disable to CC settled at 10% of final value with VCIN = 3.0V			0.05	0.06	ms
VCIN Leakage Current		VCIN detection disabled, VCIN = 4.4V		-2000		+2000	nA
USB TYPE-C / PD Controller							
Time Until BMC Bus Drive End	$t_{EndDriveBMC}$	Time to cease driving the line after the end of the last bit of the frame, Min value is limited by $t_{HoldLowBMC}$				23	µs
Transmit Hold Time	$t_{HoldLowBMC}$	Time to cease driving the line after the final high-to-low transition		1			µs
BMC TX Rise Time	t_{Rise}	10% to 90% with no load on CC wires		300	410	540	ns
BMC TX Fall Time	t_{Fall}	90% to 10% with no load on CC wires		300	410	540	ns
BMC TX Swing	V_{SWING}	Applies to no load and with max load defined by cable/receiver model for both Sink and Source		1.05	1.125	1.2	V
BMC Driver Output Impedance	z_{Driver}	Source output impedance at the Nyquist frequency of [USB 2.0] low speed (750kHz)			42	75	Ω
BMC Receiver Noise Filter	$t_{RXFilter}$	Time constant of noise filter in RX path		100			ns
Time To Detect Non-Idle Bus	$t_{TransitionWindow}$			12		20	µs
Receiver Detect Rising Threshold in SRC Mode				0.63	0.66	0.68	V
Receiver Detect Falling Threshold in SRC Mode				0.56	0.58	0.61	V
Receiver Detect Rising Threshold SNK Mode				0.51	0.54	0.56	V
Receiver Detect Falling Threshold in SNK Mode				0.44	0.46	0.49	V
Hysteresis of BMC RX	RX_Hys				60		mV
USB TYPE-C / V_{BUS} ADC							
V_{BUS} ADC Threshold 1	THV_{BUS}_01	ADCIN_SEL = 0	VBADC = 0b00000	3.0	3.5	4.0	V
V_{BUS} ADC Threshold 2	THV_{BUS}_02	ADCIN_SEL = 0	VBADC = 0b00001	4.0	4.5	5.0	V
V_{BUS} ADC Threshold 3	THVBUS_03	ADCIN_SEL = 0	VBADC = 0b00010	5.0	5.5	6.0	V
V_{BUS} ADC Threshold 4	THV_{BUS}_04	ADCIN_SEL = 0	VBADC = 0b00011	6.0	6.5	7.0	V
V_{BUS} ADC Threshold 5	THV_{BUS}_05	ADCIN_SEL = 0	VBADC = 0b00100	7.0	7.5	8.0	V
V_{BUS} ADC Threshold 6	THV_{BUS}_06	ADCIN_SEL = 0	VBADC = 0b00101	8.0	8.5	9.0	V
V_{BUS} ADC Threshold 7	THV_{BUS}_07	ADCIN_SEL = 0	VBADC = 0b00110	9.0	9.5	10.0	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BUS} ADC Threshold 8	THV_{BUS}_08	ADCIN_SEL = 0	VBADC = 0b00111	10.0	10.5	11.0	V
V_{BUS} ADC Threshold 9	THV_{BUS}_09	ADCIN_SEL = 0	VBADC = 0b01000	11.0	11.5	12.0	V
V_{BUS} ADC Threshold 10	THV_{BUS}_10	ADCIN_SEL = 0	VBADC = 0b01001	12.0	12.5	13.0	V
V_{BUS} ADC Threshold 11	THV_{BUS}_11	ADCIN_SEL = 0	VBADC = 0b01010	13.0	13.5	14.0	V
V_{BUS} ADC Threshold 12	THV_{BUS}_12	ADCIN_SEL = 0	VBADC = 0b01011	14.0	14,5	15.0	V
V_{BUS} ADC Threshold 13	THV_{BUS}_13	ADCIN_SEL = 0	VBADC = 0b01100	15.0	15.5	16.0	V
V_{BUS} ADC Threshold 14	THV_{BUS}_14	ADCIN_SEL = 0	VBADC = 0b01101	16.0	16.5	17.0	V
V_{BUS} ADC Threshold 15	THV_{BUS}_15	ADCIN_SEL = 0	VBADC = 0b01110	17.0	17.5	18.0	V
V_{BUS} ADC Threshold 16	THV_{BUS}_16	ADCIN_SEL = 0	VBADC = 0b01111	18.0	18.5	19.0	V
V_{BUS} ADC Threshold 17	THV_{BUS}_17	ADCIN_SEL = 0	VBADC = 0b10000	19.0	19.5	20.0	V
V_{BUS} ADC Threshold 18	THV_{BUS}_18	ADCIN_SEL = 0	VBADC = 0b10001	20.0	20.5	21.0	V
V_{BUS} ADC Threshold 19	THV_{BUS}_19	ADCIN_SEL = 0	VBADC = 0b10010	21.0	21.5	22.0	V
V_{BUS} ADC Threshold 20	THV_{BUS}_20	ADCIN_SEL = 0	VBADC = 0b10011	22.0	22.5	23.0	V
V_{BUS} ADC Threshold 21	THV_{BUS}_21	ADCIN_SEL = 0	VBADC = 0b10100	23.0	23.5	24.0	V
V_{BUS} ADC Threshold 22	THV_{BUS}_22	ADCIN_SEL = 0	VBADC = 0b10101	24.0	24.5	25.0	V
V_{BUS} ADC Threshold 23	THV_{BUS}_21	ADCIN_SEL = 0	VBADC = 0b10110	25.0	25.5	26.0	V
V_{BUS} ADC Threshold 24	THV_{BUS}_24	ADCIN_SEL = 0	VBADC = 0b10111	26.0	26.5	27.0	V
V_{BUS} ADC Threshold 25	THV_{BUS}_25	ADCIN_SEL = 0	VBADC = 0b11000	27.0	27.5	28.0	V
V_{BUS} ADC Hysteresis	HV_{BUS}	ADCIN_SEL = 0			150		mV
USB TYPE-C / ADCIN ADC							
GPIO ADC Threshold 1	THGPIO_01	ADCIN_SEL = 1	VBADC = 0b00000	0.6	0.7	0.8	V
GPIO ADC Threshold 2	THGPIO_02	ADCIN_SEL = 1	VBADC = 0b00001	0.8	0.9	1.0	V
GPIO ADC Threshold 3	THGPIO_03	ADCIN_SEL = 1	VBADC = 0b00010	1.0	1.1	1.2	V
GPIO ADC Threshold 4	THGPIO_04	ADCIN_SEL = 1	VBADC = 0b00011	1.2	1.3	1.4	V
GPIO ADC Threshold 5	THGPIO_05	ADCIN_SEL = 1	VBADC = 0b00100	1.4	1.5	1.6	V
GPIO ADC Threshold 6	THGPIO_06	ADCIN_SEL = 1	VBADC = 0b00101	1.6	1.7	1.8	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GPIO ADC Threshold 7	THGPIO_07	ADCIN_SEL = 1	VBADC = 0b00110	1.8	1.9	2.0	V
GPIO ADC Threshold 8	THGPIO_08	ADCIN_SEL = 1	VBADC = 0b00111	2.0	2.1	2.2	V
GPIO ADC Threshold 9	THGPIO_09	ADCIN_SEL = 1	VBADC = 0b01000	2.2	2.3	2.4	V
GPIO ADC Threshold 10	THGPIO_10	ADCIN_SEL = 1	VBADC = 0b01001	2.4	2.5	2.6	V
GPIO ADC Threshold 11	THGPIO_11	ADCIN_SEL = 1	VBADC = 0b01010	2.6	2.7	2.8	V
GPIO ADC Threshold 12	THGPIO_12	ADCIN_SEL = 1	VBADC = 0b01011	2.8	2.9	3.0	V
GPIO ADC Threshold 13	THGPIO_13	ADCIN_SEL = 1	VBADC = 0b01100	3.0	3.1	3.2	V
GPIO ADC Threshold 14	THGPIO_14	ADCIN_SEL = 1	VBADC = 0b01101	3.2	3.3	3.4	V
GPIO ADC Threshold 15	THGPIO_15	ADCIN_SEL = 1	VBADC = 0b01110	3.4	3.5	3.6	V
GPIO ADC Threshold 16	THGPIO_16	ADCIN_SEL = 1	VBADC = 0b01111	3.6	3.7	3.8	V
GPIO ADC Threshold 17	THGPIO_17	ADCIN_SEL = 1	VBADC = 0b10000	3.8	3.9	4.0	V
GPIO ADC Threshold 18	THGPIO_18	ADCIN_SEL = 1	VBADC = 0b10001	4.0	4.1	4.2	V
GPIO ADC Threshold 19	THGPIO_19	ADCIN_SEL = 1	VBADC = 0b10010	4.2	4.3	4.4	V
GPIO ADC Threshold 20	THGPIO_20	ADCIN_SEL = 1	VBADC = 0b10011	4.4	4.5	4.6	V
GPIO ADC Threshold 21	THGPIO_21	ADCIN_SEL = 1	VBADC = 0b10100	4.6	4.7	4.8	V
GPIO ADC Threshold 22	THGPIO_22	ADCIN_SEL = 1	VBADC = 0b10101	4.8	4.9	5.0	V
GPIO ADC Threshold 23	THGPIO_23	ADCIN_SEL = 1	VBADC = 0b10110	5.0	5.1	5.2	V
GPIO ADC Threshold 24	THGPIO_24	ADCIN_SEL = 1	VBADC = 0b10111	5.2	5.3	5.4	V
GPIO ADC Threshold 25	THGPIO_25	ADCIN_SEL = 1	VBADC = 0b11000	5.4	5.5	5.6	V
GPIO ADC Hysteresis	HGPIO	ADCIN_SEL= 1			25		mV
USB TYPE-C / CC ADC RANGE 1							
CC ADC Threshold 1	THCC_01	ADCIN_SEL = 001 or 011	VBADC = 0b00000	0.312	0.362	0.416	V
CC ADC Threshold 2	THCC_02	ADCIN_SEL = 001 or 011	VBADC = 0b00001	0.416	0.468	0.520	V
CC ADC Threshold 3	THCC_03	ADCIN_SEL = 001 or 011	VBADC = 0b00010	0.520	0.573	0.624	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CC ADC Threshold 4	THCC_04	ADCIN_SEL = 001 or 011	VBADC = 0b00011	0.624	0.682	0.728	V
CC ADC Threshold 5	THCC_05	ADCIN_SEL = 001 or 011	VBADC = 0b00100	0.728	0.783	0.832	V
CC ADC Threshold 6	THCC_06	ADCIN_SEL = 001 or 011	VBADC = 0b00101	0.832	0.885	0.936	V
CC ADC Threshold 7	THCC_07	ADCIN_SEL = 001 or 011	VBADC = 0b00110	0.936	0.988	1.040	V
CC ADC Threshold 8	THCC_08	ADCIN_SEL = 001 or 011	VBADC = 0b00111	1.040	1.093	1.144	V
CC ADC Threshold 9	THCC_09	ADCIN_SEL = 001 or 011	VBADC = 0b01000	1.144	1.196	1.248	V
CC ADC Threshold 10	THCC_10	ADCIN_SEL = 001 or 011	VBADC = 0b01001	1.248	1.308	1.352	V
CC ADC Threshold 11	THCC_11	ADCIN_SEL = 001 or 011	VBADC = 0b01010	1.352	1.408	1.456	V
CC ADC Threshold 12	THCC_12	ADCIN_SEL = 001 or 011	VBADC = 0b01011	1.456	1.513	1.560	V
CC ADC Threshold 13	THCC_13	ADCIN_SEL = 001 or 011	VBADC = 0b01100	1.560	1.618	1.664	V
CC ADC Threshold 14	THCC_14	ADCIN_SEL = 001 or 011	VBADC = 0b01101	1.664	1.725	1.768	V
CC ADC Threshold 15	THCC_15	ADCIN_SEL = 001 or 011	VBADC = 0b01110	1.768	1.823	1.872	V
CC ADC Threshold 16	THCC_16	ADCIN_SEL = 001 or 011	VBADC = 0b01111	1.872	1.930	1.976	V
CC ADC Threshold 17	THCC_17	ADCIN_SEL = 001 or 011	VBADC = 0b10000	1.976	2.026	2.080	V
CC ADC Threshold 18	THCC_18	ADCIN_SEL = 001 or 011	VBADC = 0b10001	2.080	2.143	2.184	V
CC ADC Threshold 19	THCC_19	ADCIN_SEL = 001 or 011	VBADC = 0b10010	2.184	2.240	2.288	V
CC ADC Threshold 20	THCC_20	ADCIN_SEL = 001 or 011	VBADC = 0b10011	2.288	2.345	2.392	V
CC ADC Threshold 21	THCC_21	ADCIN_SEL = 001 or 011	VBADC = 0b10100	2.392	2.450	2.496	V
CC ADC Threshold 22	THCC_22	ADCIN_SEL = 001 or 011	VBADC = 0b10101	2.496	2.550	2.600	V
CC ADC Threshold 23	THCC_23	ADCIN_SEL = 001 or 011	VBADC = 0b10110	2.600	2.660	2.704	V
CC ADC Threshold 24	THCC_24	ADCIN_SEL = 001 or 011	VBADC = 0b10111	2.704	2.757	2.808	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CC ADC Threshold 25	THCC_25	ADCIN_SEL = 001 or 011	VBADC = 0b11000	2.808	2.858	2.912	V
CC ADC Hysteresis	HCC	ADCIN_SEL = 001 or 011			15		mV
USB TYPE-C / CC ADC RANGE 2							
CC ADC Threshold 1	THCC_01	ADCIN_SEL = 001 or 011	VBADC = 0b00000	0.189	0.220	0.252	V
CC ADC Threshold 2	THCC_02	ADCIN_SEL = 001 or 011	VBADC = 0b00001	0.252	0.284	0.315	V
CC ADC Threshold 3	THCC_03	ADCIN_SEL = 001 or 011	VBADC = 0b00010	0.315	0.347	0.378	V
CC ADC Threshold 4	THCC_04	ADCIN_SEL = 001 or 011	VBADC = 0b00011	0.378	0.413	0.441	V
CC ADC Threshold 5	THCC_05	ADCIN_SEL = 001 or 011	VBADC = 0b00100	0.441	0.475	0.504	V
CC ADC Threshold 6	THCC_06	ADCIN_SEL = 001 or 011	VBADC = 0b00101	0.504	0.536	0.567	V
CC ADC Threshold 7	THCC_07	ADCIN_SEL = 001 or 011	VBADC = 0b00110	0.567	0.599	0.630	V
CC ADC Threshold 8	THCC_08	ADCIN_SEL = 001 or 011	VBADC = 0b00111	0.630	0.662	0.693	V
CC ADC Threshold 9	THCC_09	ADCIN_SEL = 001 or 011	VBADC = 0b01000	0.693	0.724	0.756	V
CC ADC Threshold 10	THCC_10	ADCIN_SEL = 001 or 011	VBADC = 0b01001	0.756	0.792	0.819	V
CC ADC Threshold 11	THCC_11	ADCIN_SEL = 001 or 011	VBADC = 0b01010	0.819	0.853	0.882	V
CC ADC Threshold 12	THCC_12	ADCIN_SEL = 001 or 011	VBADC = 0b01011	0.882	0.917	0.945	V
CC ADC Threshold 13	THCC_13	ADCIN_SEL = 001 or 011	VBADC = 0b01100	0.945	0.980	1.008	V
CC ADC Threshold 14	THCC_14	ADCIN_SEL = 001 or 011	VBADC = 0b01101	1.008	1.045	1.071	V
CC ADC Threshold 15	THCC_15	ADCIN_SEL = 001 or 011	VBADC = 0b01110	1.071	1.104	1.134	V
CC ADC Threshold 16	THCC_16	ADCIN_SEL = 001 or 011	VBADC = 0b01111	1.134	1.166	1.197	V
CC ADC Threshold 17	THCC_17	ADCIN_SEL = 001 or 011	VBADC = 0b10000	1.197	1.227	1.260	V
CC ADC Threshold 18	THCC_18	ADCIN_SEL = 001 or 011	VBADC = 0b10001	1.260	1.293	1.323	V
CC ADC Threshold 19	THCC_19	ADCIN_SEL = 001 or 011	VBADC = 0b10010	1.323	1.357	1.386	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CC ADC Threshold 20	THCC_20	ADCIN_SEL = 001 or 011	VBADC = 0b10011	1.386	1.421	1.449	V
CC ADC Threshold 21	THCC_21	ADCIN_SEL = 001 or 011	VBADC = 0b10100	1.449	1.484	1.512	V
CC ADC Threshold 22	THCC_22	ADCIN_SEL = 001 or 011	VBADC = 0b10101	1.512	1.545	1.575	V
CC ADC Threshold 23	THCC_23	ADCIN_SEL = 001 or 011	VBADC = 0b10110	1.575	1.612	1.638	V
CC ADC Threshold 24	THCC_24	ADCIN_SEL = 001 or 011	VBADC = 0b10111	1.638	1.671	1.701	V
CC ADC Threshold 25	THCC_25	ADCIN_SEL = 001 or 011	VBADC = 0b11000	1.701	1.731	1.764	V
CC ADC Hysteresis	HCC	ADCIN_SEL = 001 or 011			15		mV
USB TYPE-C / CC ADC RANGE 3							
CC ADC Threshold 1	THCC_01	ADCIN_SEL = 001 or 011	VBADC = 0b00000	0.150	0.175	0.200	V
CC ADC Threshold 2	THCC_02	ADCIN_SEL = 001 or 011	VBADC = 0b00001	0.200	0.225	0.250	V
CC ADC Threshold 3	THCC_03	ADCIN_SEL = 001 or 011	VBADC = 0b00010	0.250	0.275	0.300	V
CC ADC Threshold 4	THCC_04	ADCIN_SEL = 001 or 011	VBADC = 0b00011	0.300	0.325	0.350	V
CC ADC Threshold 5	THCC_05	ADCIN_SEL = 001 or 011	VBADC = 0b00100	0.350	0.375	0.400	V
CC ADC Threshold 6	THCC_06	ADCIN_SEL = 001 or 011	VBADC = 0b00101	0.400	0.425	0.450	V
CC ADC Threshold 7	THCC_07	ADCIN_SEL = 001 or 011	VBADC = 0b00110	0.450	0.475	0.500	V
CC ADC Threshold 8	THCC_08	ADCIN_SEL = 001 or 011	VBADC = 0b00111	0.500	0.525	0.550	V
CC ADC Threshold 9	THCC_09	ADCIN_SEL = 001 or 011	VBADC = 0b01000	0.550	0.575	0.600	V
CC ADC Threshold 10	THCC_10	ADCIN_SEL = 001 or 011	VBADC = 0b01001	0.600	0.625	0.650	V
CC ADC Threshold 11	THCC_11	ADCIN_SEL = 001 or 011	VBADC = 0b01010	0.650	0.675	0.700	V
CC ADC Threshold 12	THCC_12	ADCIN_SEL = 001 or 011	VBADC = 0b01011	0.700	0.725	0.750	V
CC ADC Threshold 13	THCC_13	ADCIN_SEL = 001 or 011	VBADC = 0b01100	0.750	0.775	0.800	V
CC ADC Threshold 14	THCC_14	ADCIN_SEL = 001 or 011	VBADC = 0b01101	0.800	0.825	0.850	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CC ADC Threshold 15	THCC_15	ADCIN_SEL = 001 or 011	VBADC = 0b01110	0.850	0.875	0.900	V
CC ADC Threshold 16	THCC_16	ADCIN_SEL = 001 or 011	VBADC = 0b01111	0.900	0.925	0.950	V
CC ADC Threshold 17	THCC_17	ADCIN_SEL = 001 or 011	VBADC = 0b10000	0.950	0.975	1.000	V
CC ADC Threshold 18	THCC_18	ADCIN_SEL = 001 or 011	VBADC = 0b10001	1.000	1.025	1.050	V
CC ADC Threshold 19	THCC_19	ADCIN_SEL = 001 or 011	VBADC = 0b10010	1.050	1.075	1.100	V
CC ADC Threshold 20	THCC_20	ADCIN_SEL = 001 or 011	VBADC = 0b10011	1.100	1.125	1.150	V
CC ADC Threshold 21	THCC_21	ADCIN_SEL = 001 or 011	VBADC = 0b10100	1.150	1.175	1.200	V
CC ADC Threshold 22	THCC_22	ADCIN_SEL = 001 or 011	VBADC = 0b10101	1.200	1.225	1.250	V
CC ADC Threshold 23	THCC_23	ADCIN_SEL = 001 or 011	VBADC = 0b10110	1.250	1.275	1.300	V
CC ADC Threshold 24	THCC_24	ADCIN_SEL = 001 or 011	VBADC = 0b10111	1.300	1.325	1.350	V
CC ADC Threshold 25	THCC_25	ADCIN_SEL = 001 or 011	VBADC = 0b11000	1.350	1.375	1.400	V
CC ADC Hysteresis	HCC	ADCIN_SEL = 001 or 011			7		mV
USB TYPE-C / USB ANALOG SWITCH (DN1/DP2)							
Analog Signal Range	V_{DN1}, V_{DP2}			0		V_{AVL}	V
On-Resistance	R_{ONUSB}	AVL = 3.0V, I_{DN}/I_{DP} = 10mA, V_{DN}/V_{DP} = 0V to 3.0V			3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	AVL = 3.0V, I_{DN}/I_{DP} = 10mA, V_{DN}/V_{DP} = 400mV				0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	AVL = 3.0V, I_{DN}/I_{DP} = 10mA, V_{DN}/V_{DP} = 0V to 3.0V			0.1	0.4	Ω
Off Leakage Current	$I_{LUSBOFF}$	AVL = 4.2V; Switch opened; V_{DN1} or V_{DP2} = 0.3V, 2.5V; V_{DN} or V_{DP} = 2.5V, 0.3V		-360		+360	nA
USB TYPE-C / DYNAMIC PERFORMANCE							
Analog Switch Turn On Time	t_{ON}	I²C stop to switch on; RL = 50Ω			0.1	0.3	ms
Analog Switch Turn Off Time	t_{OFF}	I²C stop to switch off; RL = 50Ω			0.1	0.3	ms
USB TYPE-C / GPIO0, 1, 2, 3, 8							
Input Low Voltage	V_{IL}					0.3 x VIO2	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}			0.7 x VIO2			V
Input Hysteresis (Schmitt)	V_{IHYS}				250		mV
Output Low Voltage	V_{OL}	I_{SINK} = 2mA				0.4	V
Output High Voltage	V_{OH}	I_{SINK} = 2mA		0.7 x VIO2			V
Input Leakage Current	IL	T_A = +25°C			100		nA
Input Pullup Resistor	R_{PU}				100		kΩ
Input Pulldown Resistor	R_{PD}				100		kΩ
USB TYPE-C / GPIO4, 5, 6, 7							
Input Low Voltage	V_{IL}					0.3 x VIO1	V
Input High Voltage	V_{IH}			0.7 x VIO1			V
Input Hysteresis (Schmitt)	V_{IHYS}				250		mV
Output Low Voltage	V_{OL}	I_{SINK} = 2mA				0.4	V
Output High Voltage	V_{OH}	I_{SINK} = 2mA		0.7 x VIO1			V
Input Leakage Current	IL	T_A = +25°C			100		µA
Input Pullup Resistor	R_{PU}				100		kΩ
Input Pulldown Resistor	R_{PD}				100		kΩ
USB TYPE-C / I²C Master / I²C Logic level							
SCL_M, SDA_M Input Low Level		T_A = +25°C				0.3 x VIO2	V
SCL_M, SDA_M Input High Level		T_A = +25°C		0.7 x VIO2		VIO2	V
SCL_M, SDA_M Input Hysteresis		T_A = +25°C			0.05 x VIO2		V
SCL_M, SDA_M Logic Input Current		SCL_M = SD_AM = VIO2 = 5.5V		-1000		+1000	nA
SCL_M, SDA_M Input Capacitance					10		pF
SCL_M, SDA_M Output Low Voltage		Sinking 3mA	VIO = HV			0.4	V
			VIO = LV			0.2 x VIO	
SCL_M, SDA_M Input Leakage Current	I_{LK}	T_A = +25°C		-1000		+1000	nA
		T_A = +85°C			100		
USB TYPE-C / I²C Master / I²C Timing for Standard, Fast, and Fast-Mode Plus							
Clock Frequency	f_{SCL}					1000	kHz

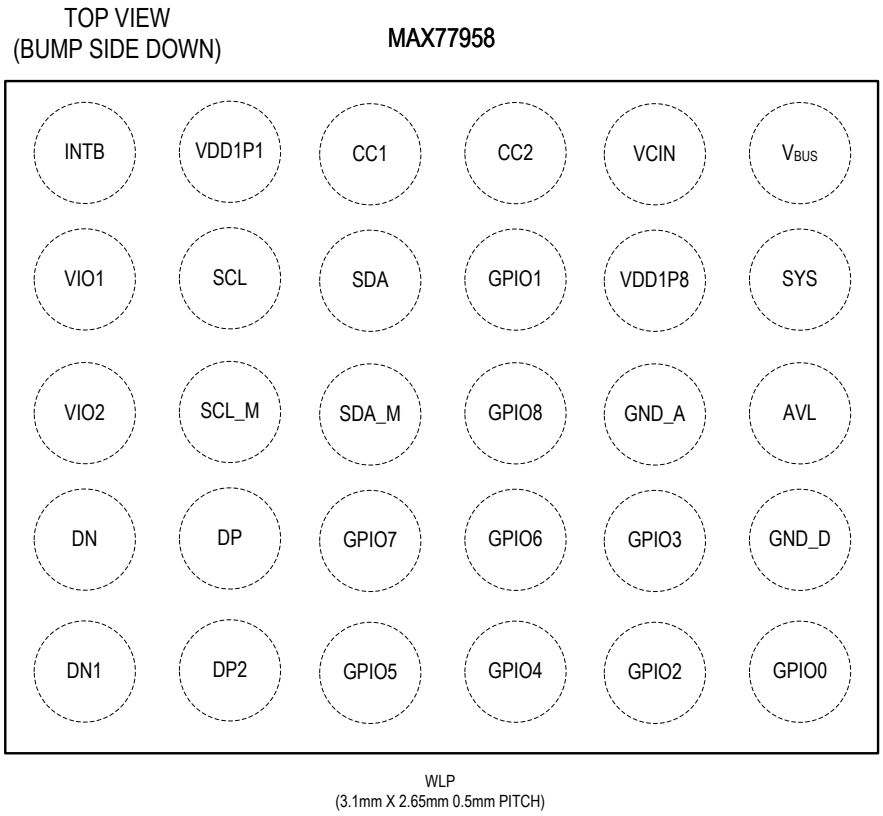
Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns
USB TYPE-C / MTP						
VCIN Input Supply	VCIN_MTP	Reading, Erasing, Programming	4.5	5.15	5.5	V
VCIN Current Consumption	IVCIN_MTP_ERASE	Erasing		8		mA
	IVCIN_MTP_PROG	Programming		16		
MTP Erasing / Programming Time	tMTP_ERASE	Erasing (1 page = 128 * 32-bits word)		100		ms
	tMTP_PROG	Programing		500		µs / 32-bit word
MTP Write Capacity	NWrite	VDD1P8 = 2V, VCIN = 5.5V		100		Write
MTP Data Retention	tMTP	VDD1P8 = 2V, VCIN = 5.5V		10		Year
USB TYPE-C / Power Supply						
LDO—Output Voltage		I_L = 1mA	1.05	1.125	1.2	V
LDO—Current Limit			-19	-11	-5	mA
LDO—Power Up Consumption				5	12	µA
LDO—Turn On Time		From BMC_PWDN_LDO = 0 to V1P1 = 95% of final value			300	µs
LDO—Output Pulldown Current		VDD1P1 = 1.125V and BMC_LDO_LOAD = 1	330			µA

Pin Configuration

MAX77958



Pin Description

PIN	NAME	FUNCTION
B1	VIO1	System IO Voltage Input. Connect a 1µF/6.3V ceramic capacitor to GND.
C1	VIO2	System IO Voltage Input. Connect a 1µF/6.3V ceramic capacitor to GND.
A6	V_{BUS}	V_{BUS} Input. V_{BUS} provides power for internal circuitry when SYS is less than V_{BUS}. Bypass V_{BUS} to GND with a 1µF (min) ceramic capacitor.
B6	SYS	Power Input. SYS provides power for internal circuitry when V_{BUS} is less than SYS. Bypass SYS to GND with a 1µF (min) ceramic capacitor.
C6	AVL	Analog Voltage Level. Output of the on-chip LDO is used to power the on-chip and low-noise circuits. Bypass with a 2.2µF/10V ceramic capacitor to GND. Powering external loads from AVL is not recommended, other than pullup resistors.
B5	VDD1P8	1.8V Internal LDO Output. Bypass the pin to ground with a 1µF/6.3V ceramic capacitor.
A2	VDD1P1	Digital Supply Voltage of 1.1V. Bypass with a 1µF/6.3V ceramic capacitor.
B3	SDA	I^2C Serial Data. Add an external 2.2kΩ pullup resistor to VIO1.

Pin Description (continued)

PIN	NAME	FUNCTION
B2	SCL	I^2C Serial Clock. Add an external 2.2kΩ pullup resistor to VIO1.
A1	INTB	Interrupt Output. Active-low open-drain output. Add a 200kΩ pullup resistor to VIO1.
E1	DN1	USB Input 1 for D-
E2	DP2	USB Input 2 for D+
D1	DN	Common Negative Output 1. Connect to D- on USB Type-C connector.
D2	DP	Common Positive Output 2. Connect to D+ on USB Type-C connector.
A3	CC1	USB Type-C CC Pin 1
A4	CC2	USB Type-C CC Pin 2
A5	VCIN	V_{CONN} Power Supply. Supplies V_{CONN} to the unused CC pin if required.
E6	GPIO0	GPIO0—ADC Input 0
B4	GPIO1	GPIO1—ADC Input 1
E5	GPIO2	GPIO2
D5	GPIO3	GPIO3
E4	GPIO4	GPIO4
E3	GPIO5	GPIO5
D4	GPIO6	SID Selection Table 2
D3	GPIO7	GPIO7
C4	GPIO8	GPIO8
C5	GND_A	Analog GND
D6	GND_D	Digital GND
C3	SDA_M	Master I^2C Serial Data. Add an external 2.2kΩ pullup resistor to VIO2.
C2	SCL_M	Master I^2C Serial Clock. Add an external 2.2kΩ pullup resistor to VIO2.

Detailed Description

The MAX77958 is a robust solution for USB Type-C CC detection and power delivery (PD) protocol implementation. It detects connected accessories or devices by using Type-C CC detection and USB PD messaging. The IC protects against overvoltage and overcurrent, and detects moisture and prevents corrosion on the USB Type-C connector. The IC also has a D+/D- USB switch and BC1.2 detection to support legacy USB standards. It contains V_{CONN} switches for USB PD and an enable pin for an external V_{CONN} boost or buck converter.

The IC can be used in sink mode to determine the source capabilities of the connected device to optimize power into the sink device. The IC can also be used in source mode to advertise the power capabilities of the source to connected devices and accessories.

The IC is compliant with USB Type-C Version 1.3 and PD 3.0. It can be further customized without affecting the compliance. Customization is available through the customization script in the evaluation kit (EV kit) GUI to support different Maxim chargers.

USB Type-C Interface and Control

The MAX77958 is a complete solution for USB port charger detection and High-Power USB charging on a single USB Type-C connector. It can also be used in any power sink or source application.

The USB Type-C is an internal block that detects connected accessories by using USB Type-C, USB PD messaging and USB BC1.2 charger detection. The USB Type-C block auto-configures switches for common connected accessories including USB cables (SDP/CDP/DCP).

CC/USB PD Interface

The MAX77958 works as a Dual Role Port (DRP) compliant to USB Type-C Version 1.3. The USB Type-C functions are controlled by a logic state machine which follows the USB Type-C requirements. There is support for the optional Try.Sink function which places priority on the sink role. This creates the appearance of legacy operation when the device is connected to another DRP. The IC automatically becomes a sink and draws power from the source. The IC firmware can optionally set an external charger's input current limit based on the current advertised on the CC lines through the master I^2C interface.

USB Type-C Definitions

- UFP—Upstream Facing Port. Typical USB device role for data transfer.
- DFP—Down Stream Facing Port. Typical USB host role for data transfer.
- DRP—Dual Role Port. USB Type-C port that can operate in either DFP or UFP roles.
- Source—Initial power state for a DFP. Power role can be swapped by USB Power Delivery command.
- Sink—Initial power state for a UFP. Power role can be swapped by USB Power Delivery command.

DRP

The USB Type-C connector management block supports DRP operation. The port cycles between advertising DFP/source and UFP/sink operations while waiting for a port to be connected. The internal state machine handles all the tasks of detecting and configuring the CC pins for the correct mode. A manual mode allows forcing either DFP or UFP operation in cases where the DRP operation is not appropriate

Detecting Connected DFP

When a DFP is detected (either from DRP mode or force UFP mode), the USB Type-C Connection State Machine detects the active CC line and reports this with an interrupt to the host application processor (AP). The AP then uses this information to de-mux the SuperSpeed USB lines as required. The USB Type-C Connection State Machine also auto detects the UFP advertised current (default, 1.5A and 3.0A). Upon detection of a change in the advertised current, an interrupt is sent to the AP.

Detecting Connected UFP

When a UFP is detected (either from DRP mode or force DFP mode), the USB Type-C State Machine detects the active CC line. If the Interrupt is enabled, and an AP is present, the IC toggles the INT line to report this to the host AP. Additionally, if an active cable is connected, the IC detects the presence of R_A on the unconnected CC line to determine if it is necessary to turn on V_{CONN}. The advertised initial supply current is the default USB current (500mA/900mA depending on if SuperSpeed is active). The advertised current can be changed through an I^2C command or automatically to 1.5A. 3.0A is optionally available but is disabled by default.

Controls

Reported Status and Interrupts

- Connected Device Detection
- Active CC Line
- V_{CONN} Enabled (R_A Present)
- Advertised Current in UFP (Source) Mode
- Error State

Operation Controls

- Force Source (DFP) or Sink (UFP) State
- Control Swap of Power Role or V_{CONN} Role
- Enable/Disable of Audio or Debug Accessories
- Set Advertisement of CC Pin Current in Source Role

Try.SNK Support

The MAX77958 operates as a DRP by default. This type of port can act as either a Power Sink/USB Data Peripheral or a Power Source/USB Data Host. The USB Type-C logic state machine cycles between Source and Sink at a rate typically around 75ms. This means that when the IC is connected to another device, which is also a DRP (for example, PC with a C port), the source and sink roles are randomly assigned. The customer prefers that the mobile phone assumes the sink role if connected to a PC. The IC includes support for Try.SNK, which allows it to be set to strongly prefer the sink role if connected to a standard DRP. If two devices with Try.SNK enable are connected, the role setting is again random.

Audio Accessory Mode Support

The IC detects an audio accessory device when both the CC1 and CC2 pins are pulled down to ground by an R_A resistor from the connected device.

DebugAcessory.SRC Support

The IC detects a connection to a debug and test system (DTS) when it operates in source power role. A debug accessory device is detected when the CC1 and CC2 pins are pulled down to ground by an R_D resistor from the connected device.

DebugAcessory.SNK Support

The IC detects a connection to a DTS when it operates in sink power role. A debug accessory device is detected when the CC1 and CC2 pins are pulled up by an Rp resistor from the connected device.

The voltage levels on the CC1 and CC2 pins give the orientation and current capability.

Table 1. Rp/Rp Charging Current Values for a DTS Source

MODE OF OPERATION	CC1	CC2
Default USB Power	Rp for 3A	Rp for 1.5A
USB Type-C Current at 1.5A	Rp for 1.5A	Rp for Default
USB Type-C Current at 3A	Rp for 3A	Rp for Default

USB Type-C Interface and Control

Automatic Accessory Detection

Autoconfiguration Details

CCDetEn = 0 or ChgDetEn = 0

1. Nothing happens when V_{BUS} is attached. Nothing occurs when ChgDetMan is set to 1.

CCDetEn = 1 and ChgDetEn = 1

1. Charger detection runs automatically when V_{BUS} is attached
2. If V_{BUS} voltage enters the valid range, all switches connected to DP/DN are opened
3. Charger detection algorithm begins.
4. When charger detection finishes, DP/DN switch settings are restored.

USBAuto = 0

1. No automatic switch configuration happens

USBAuto = 1

1. Operates only after charger detection completes, SDP or CDP is found, and if no special charger is found (SpChgTyp = 000 unknown).
2. Set DP/DN connected to DP2/DN1, over-riding any previous switch setting.
3. At any time, the AP is allowed to change these switch settings.
4. If AP has not changed the switch settings when V_{BUS} drops below the valid level, DP/DN sets to Hi-Z.

USB Power Delivery

Description

The IC supports USB Power Delivery Revision 3.0. The power delivery subsystem is separated into 2 parts: Automatic Power Control and Application Processor Message Passthrough.

Automatic Power Control

When a USB Type-C connection is made, the IC automatically handles the initial PD power contract. If a source is connected, the IC reads selects an appropriate voltage and current from the offered capabilities. The IC automatically configures the companion chip input current limit based on the contract if the I_{LIM_FW} bit is set to 1. The AP may later negotiate a new operating power and manually set the input limiter and charger. If a sink is connected, the IC sends a capabilities message to the attached sink.

Application Processor Message Passthrough

There are many USB PD messages that are unrelated to power control. These messages pass on to the AP to decode and reply. USB PD messages have time critical components and the IC automatically handles these time critical events.

IC Wakeup events

The IC automatically operates in the lowest possible power state. The IC power consumption depends on the following conditions:

- Request has been made across the I^2C bus
- USB Type-C end-to-end detection is valid
- V_{BUS} is present

The lowest possible power consumption state is no V_{BUS}, CCDetEn = 0, and no I^2C traffic requests.

Interrupt Output (INTB)

INTB is an open-drain and active-low output. It reports an interrupt event to the main microprocessor. Individual interrupt sources can be masked. Once the main microprocessor reads the interrupt registers, the INTB pin is cleared.

Interconnected Block Diagram

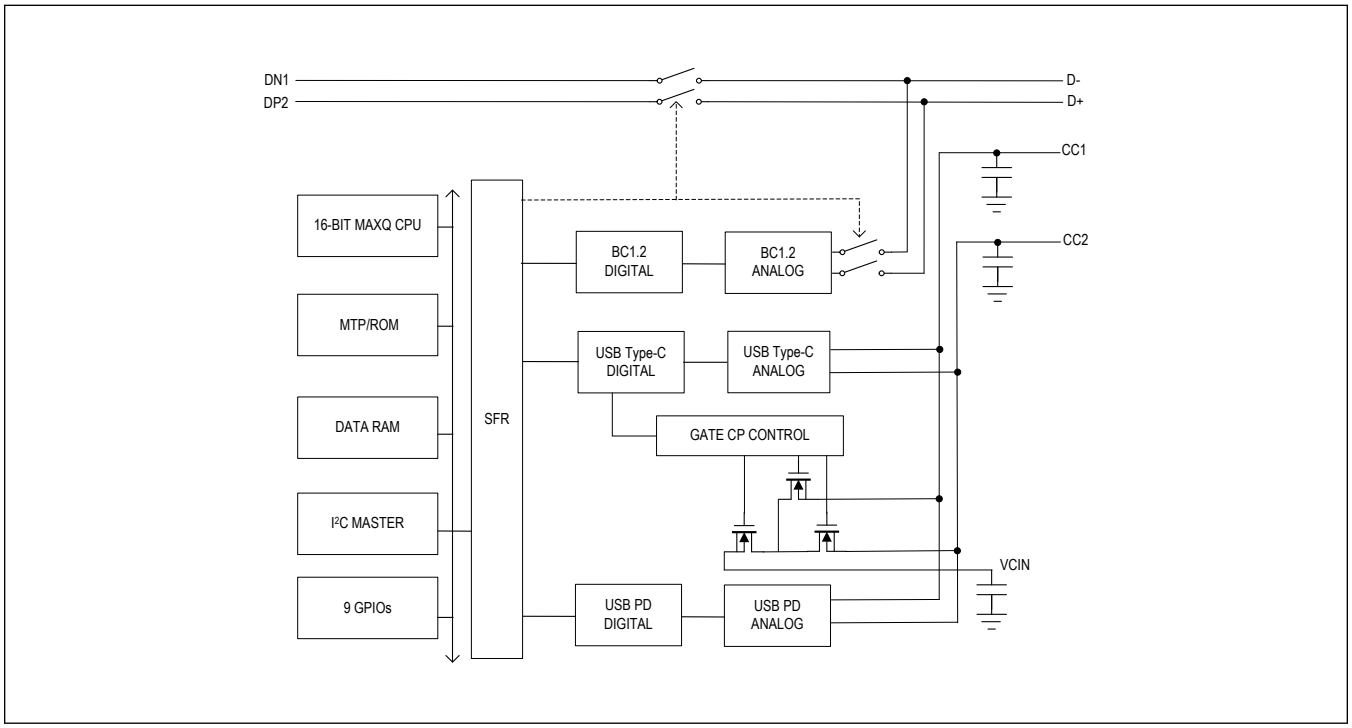


Figure 1. Interconnected Block Diagram

System Faults

The IC monitors the system for the following faults:

- Undervoltage lockout
- VIO fault

Undervoltage Lockout

When the V_{AVL} falls below AVL_{UVLOF} (2.6V max) for more than 8ms, the MAX77958 enters into a shutdown state. Once the V_{AVL} voltage is higher than AVL_{UVLOR} (2.8V max), the MAX77958 exits shutdown state to be functional.

VIO Fault

When VIO1 and VIO2 fall below 1.0V, the IC goes into shutdown state. Once VIO1 and VIO2 voltages rise higher than 1.3V, the IC comes out of shutdown state.

Reset Conditions

The IC has different levels of reset as follows:

- **Type S:** Registers are reset each time when VDD1P8 < VDD_OK_F
- **Type O:** Registers are reset each time when VDD1P8 < VDD_OK_F or when the software reset command is transmitted (SW_RESET = 0x0F)

WDT Reset

1. Firmware restarts a watchdog timer in 1.86s.
2. If the watchdog timer is not kicked in 1.86s, it executes the following actions:
   a.) MAX77958 reboots
   b.) MAX77958 notifies MA_SYSERROR_BOOT_WDT

I²C Serial Interface

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 2 shows an example of a typical I²C system. A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX77958 I²C-compatible interface is operating, it is a slave on the I²C bus and it can be both a transmitter and a receiver.

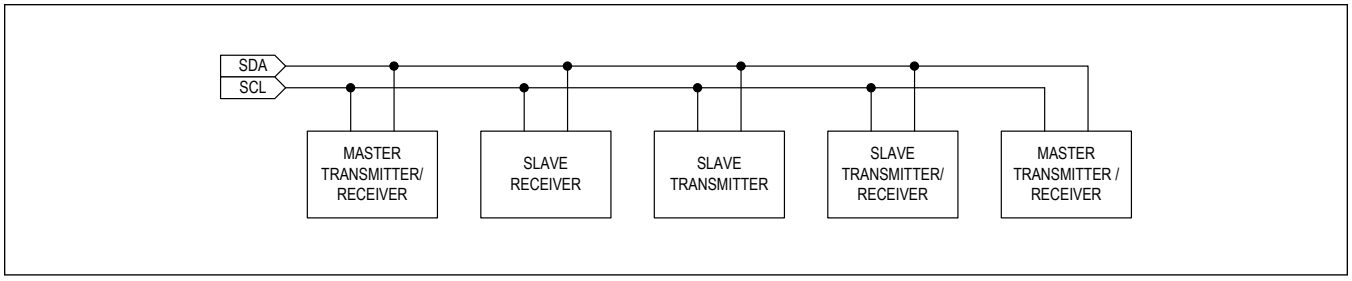


Figure 2. Functional Logic Diagram for Communications Controller

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of the SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

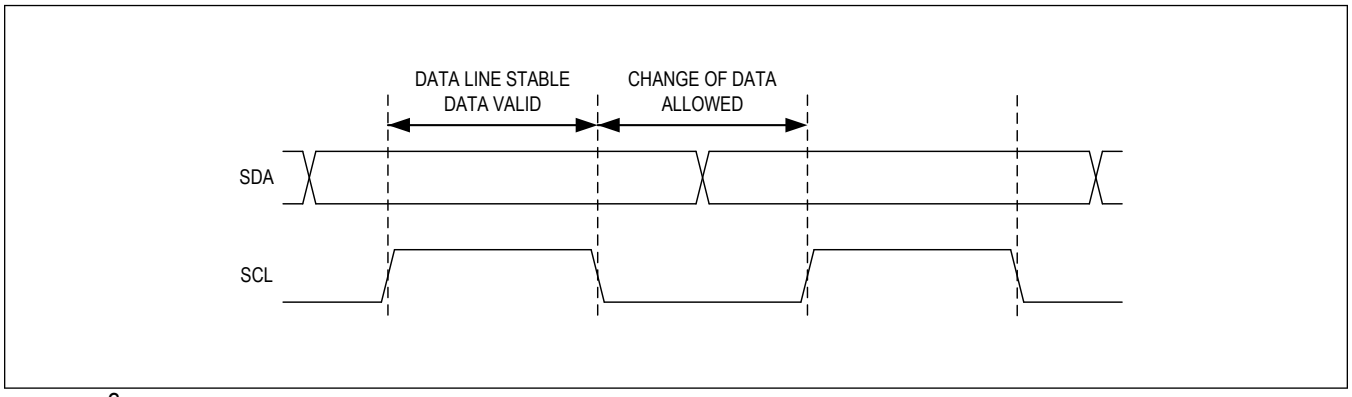


Figure 3. I2C Bit Transfer

START and STOP Conditions

When the I2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from the I2C serial interface until the next START condition, minimizing digital noise and feed-through.

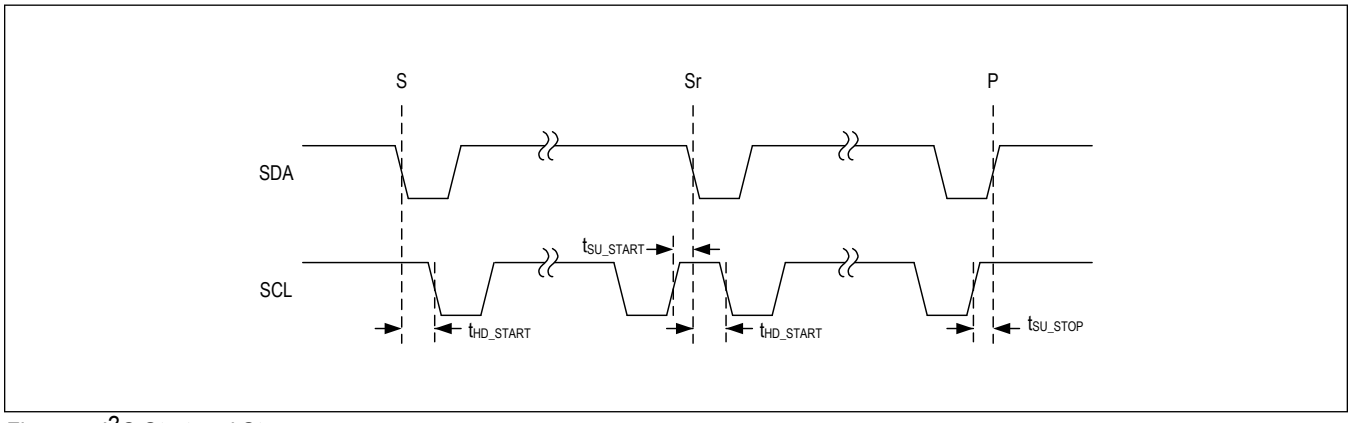


Figure 4. I2C Start and Stop

Acknowledge

Both the I2C bus master and the IC (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The IC acts as a slave transmitter/receiver. The slave address of the IC is 0x4Ah/0x4Bh,0x4Ch/0x4Dh and 0x4Eh/0x4Fh depending on configuration of GPIO6.The least significant bit is the read/write indicator (1 for read, 0 for write).

Table 2. I2C Slave Address

GPIO6	SLAVE ADDRESS (7-BIT)	SLAVE ADDRESS (WRITE)	SLAVE ADDRESS (READ)
GND	010 0101	0x4A (0100 1010)	0x4B (0100 1011)
Pullup (330kΩ) to VIO1	010 0110	0x4C (0100 1100)	0x4D (0100 1101)
Pulldown (330kΩ) to GND	010 0111	0x4E (0100 1110)	0x4F (0100 1111)

Clock Stretching

In general, the clock signal generation for I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

General Call Address

The IC does not implement an I2C specification general call address. If the IC sees general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

Communication Speed

The IC provides I2C 3.0-compatible (1MHz) serial interface.

- I2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast-Mode Plus)
- Does not Support I2C Clock Stretching

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *"Pullup Resistor Sizing"* section of the I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, see the I2C 3.0 specification. The major considerations with respect to the IC are:

- I2C bus master uses current source pullups to shorten the signal rise times.

- I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the IC input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Communication Protocols* section.

Communication Protocols

The IC supports both writing and reading from its registers.

Writing to a Single Register

Figure 5 shows the protocol for the I2C master device to write one byte of data to the IC. This protocol is the same as SMBus specification's "Write Byte" protocol.

The "Write Byte" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

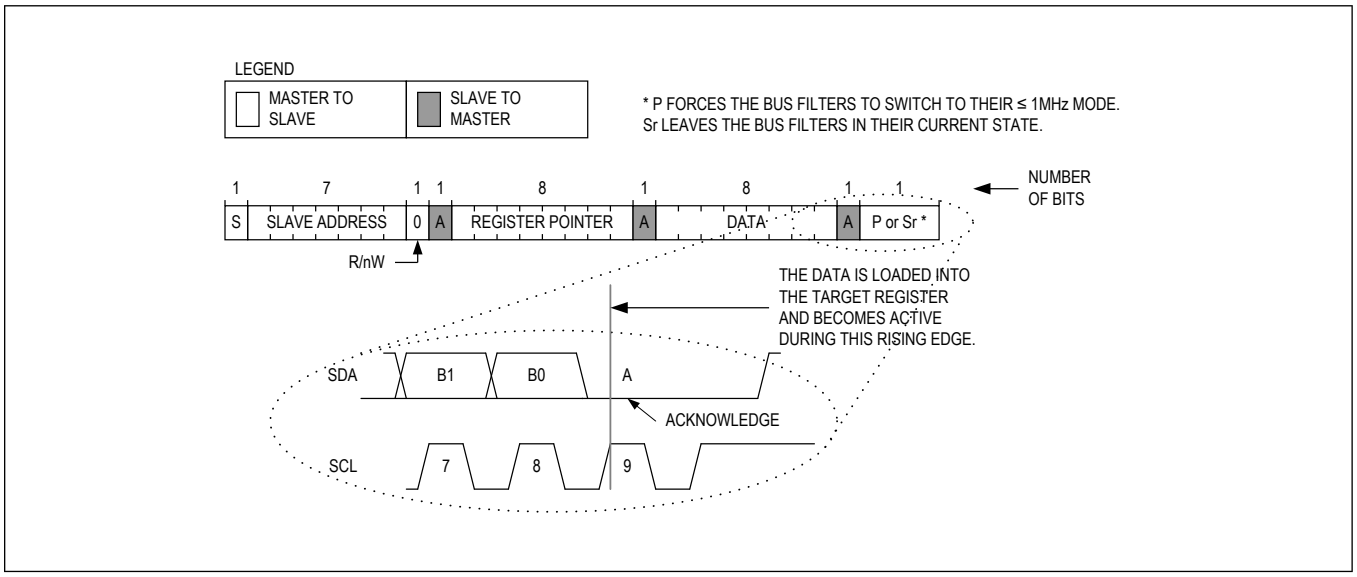


Figure 5. Writing to a Single Register

Writing to Sequential Registers

Figure 6 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The “Writing to Sequential Registers” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

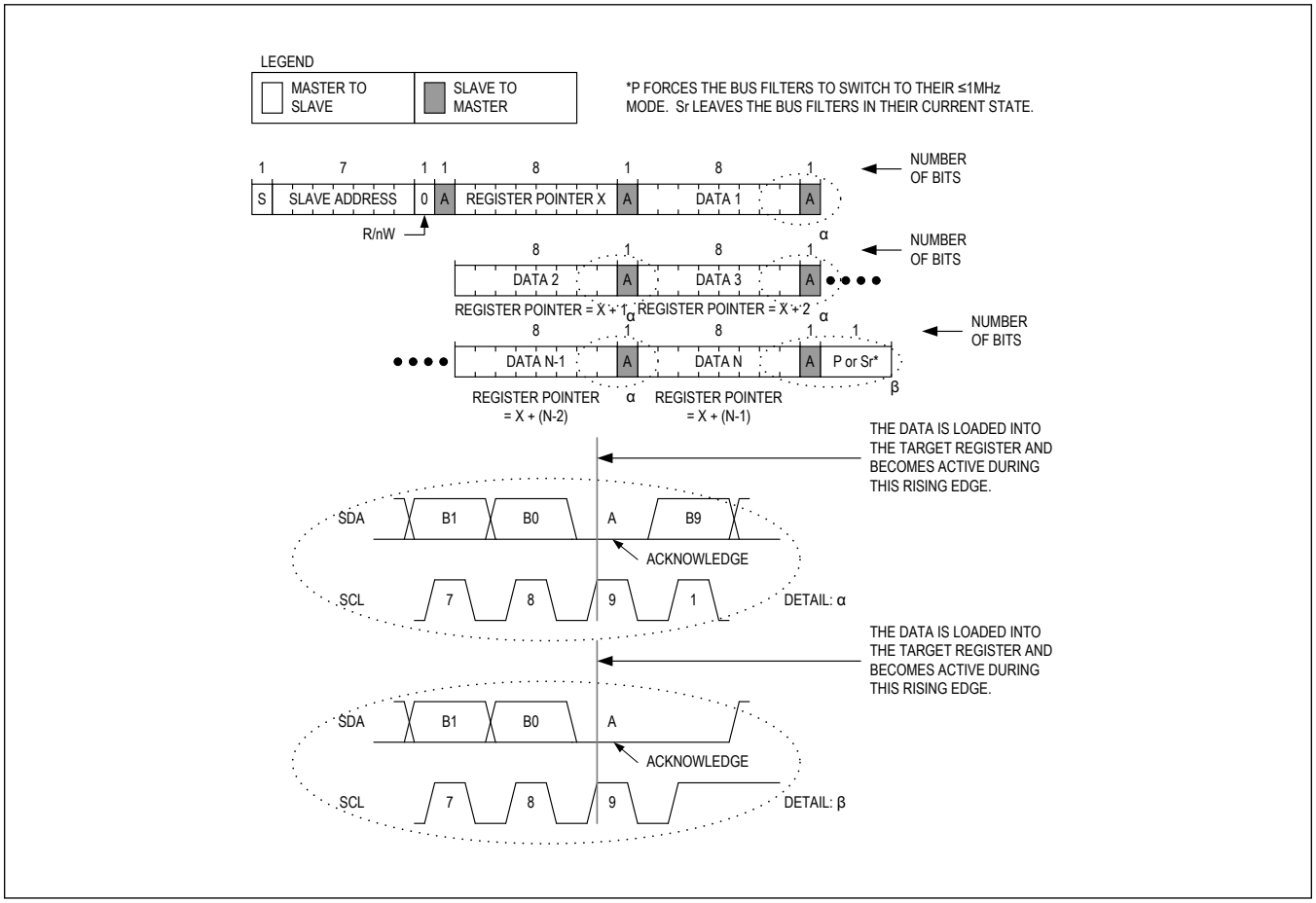


Figure 6. Writing to Sequential Registers

Reading from a Single Register

The I2C master device reads one byte of data to the IC. This protocol is the same as SMBus specification's "Read Byte" protocol.

The "Read Byte" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

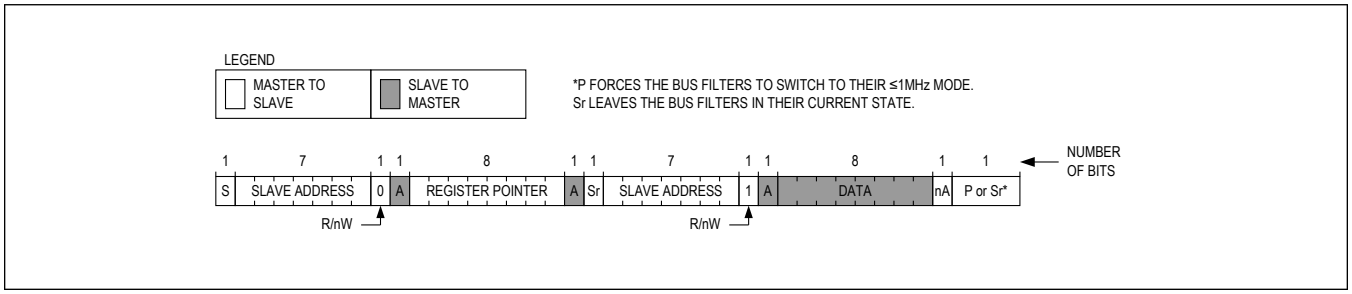


Figure 7. Reading from a Single Register

Reading from Sequential Registers

Figure 8 shows the protocol for reading from sequential registers. This protocol is similar to the "Read Byte" protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data—when the master has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP (P) to end the transmission.

The "Continuous Read from Sequential Registers" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ =1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

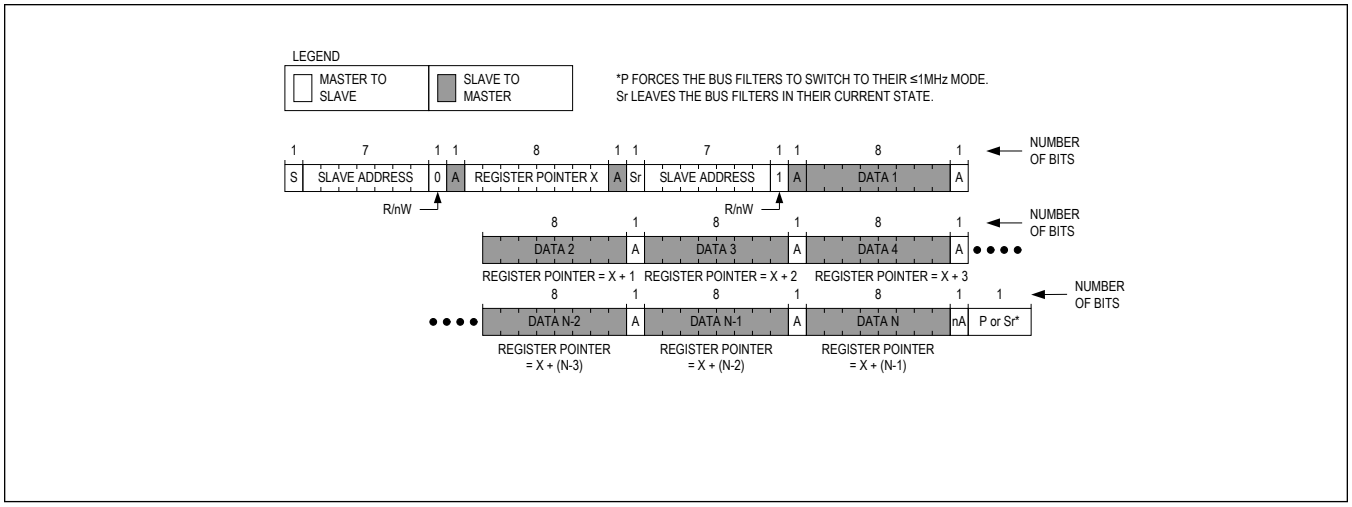


Figure 8. Reading from Sequential Registers

Engaging HS-Mode for Operation up to 3.4MHz

Figure 9 shows the protocol for engaging HS-Mode operation. HS-Mode operation allows for a bus operating speed up to 3.4MHz.

The “Engaging HS-Mode” protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START command (S).
3. The master sends the 8-bit master code of 0000 1xx0b, where ‘xx’ are don’t care bits.
4. The addressed slave issues a NOT-ACKNOWLEDGE (nA).
5. The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a STOP (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation.

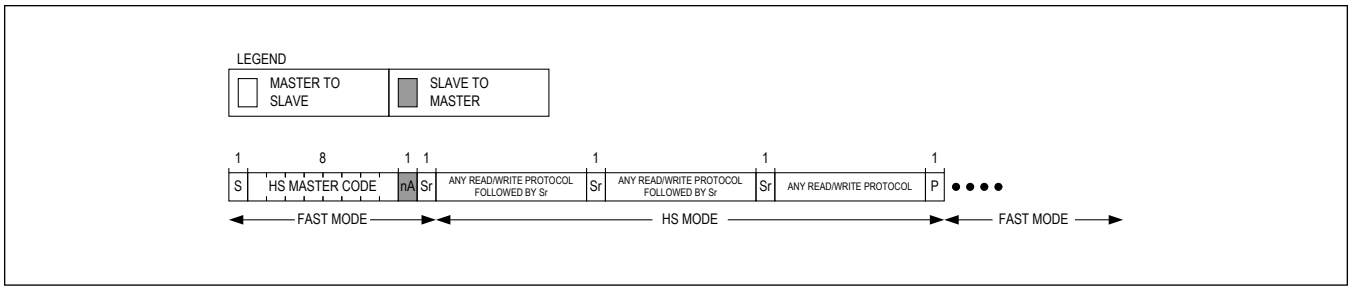


Figure 9. Engaging HS-Mode

The MAX77958 I2C supports the HS mode extension feature. The HS extension feature keeps the high-speed operation even after a ‘STOP’ condition. This eliminates the need for HS master code issued by the I2C master controller when the I2C master controller wants to stay in HS mode for multiple read/write cycles.

As shown in Figure 10, the HS extension mode can be enabled by setting HS_EXT bit in I2C_CFG register (ADDR 0x15) from LS mode only (entering HS extension mode from HS mode is not supported).

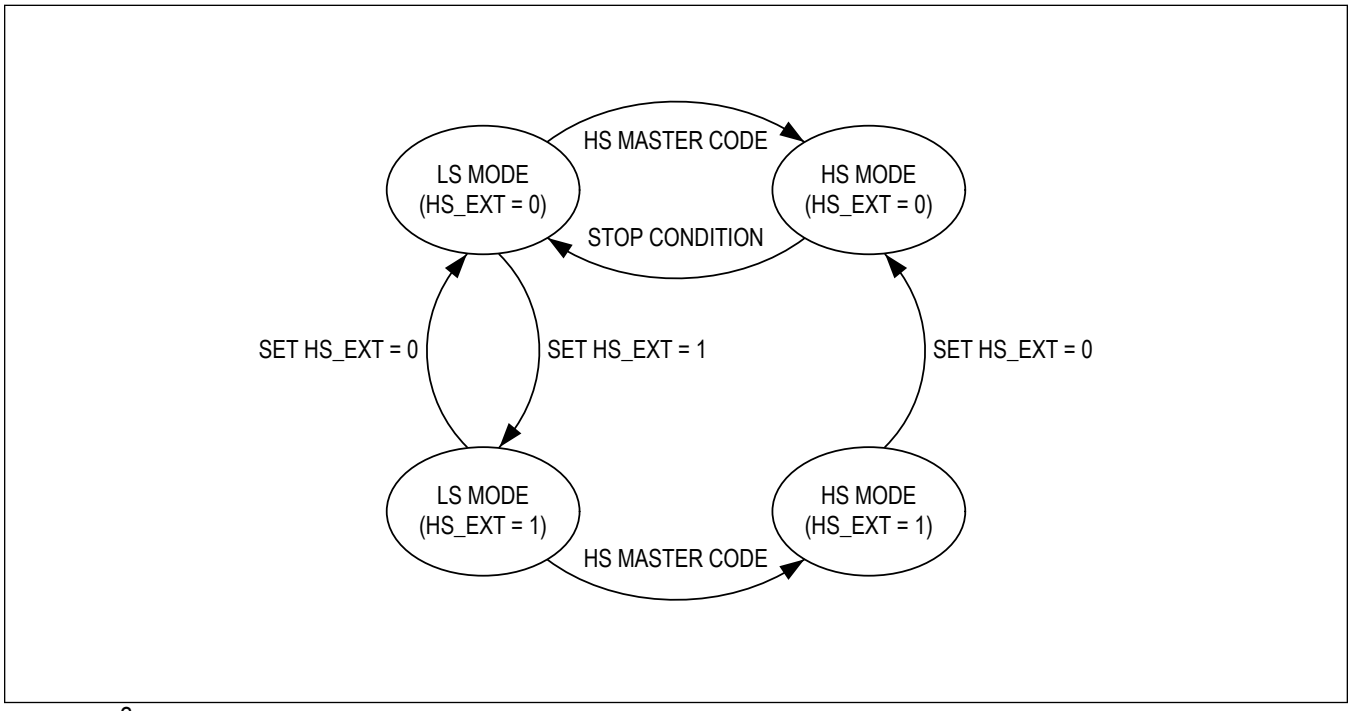


Figure 10. I2C Operating Mode State Diagram

Register Map

FUNC

I2C Slave Address

The MAX77958 has a total of 4 slave addresses. See Table 2 for more information.

Functional Reset Conditions

The IC has different levels of reset as follows:

- Type S: Registers are reset each time when VDD1P8 < VDD_OK_F
- Type O: Registers are reset each time when VDD1P8 < VDD_OK_F or when the software reset command is transmitted (SW_RESET = 0x0F)

Functional Register Reset Type Summary

	REGISTER ADDRESS (HEX)	REGISTER FUNCTION	REGISTER NAME	RESET TYPE
USBC SID (functional registers)				
USBC	0x00	USBC	UIC_HW_REV	S
USBC	0x01	USBC	UIC_FW_REV	S
USBC	0x02	USBC	UIC_INT	O
USBC	0x03	USBC	CC_INT	O
USBC	0x04	USBC	PD_INT	O
USBC	0x06	USBC	USBC_STATUS1	S
USBC	0x07	USBC	USBC_STATUS2	S
USBC	0x08	USBC	BC_STATUS	S
USBC	0x0A	USBC	CC_STATUS0	S
USBC	0x0B	USBC	CC_STATUS1	S
USBC	0x0C	USBC	PD_STATUS0	S
USBC	0x0D	USBC	PD_STATUS1	S
USBC	0x0E	USBC	UIC_INT_M	O
USBC	0x0F	USBC	CC_INT_M	O
USBC	0x10	USBC	PD_INT_M	O
USBC	0x21	USBC	AP_DATAOUT0	O
USBC	0x22	USBC	AP_DATAOUT1	O
USBC	0x23	USBC	AP_DATAOUT2	O
USBC	0x24	USBC	AP_DATAOUT3	O
USBC	0x25	USBC	AP_DATAOUT4	O
USBC	0x26	USBC	AP_DATAOUT5	O
USBC	0x27	USBC	AP_DATAOUT6	O
USBC	0x28	USBC	AP_DATAOUT7	O
USBC	0x29	USBC	AP_DATAOUT8	O
USBC	0x2A	USBC	AP_DATAOUT9	O
USBC	0x2B	USBC	AP_DATAOUT10	O

USBC	0x2C	USBC	AP_DATAOUT11	O
USBC	0x2D	USBC	AP_DATAOUT12	O
USBC	0x2E	USBC	AP_DATAOUT13	O
USBC	0x2F	USBC	AP_DATAOUT14	O
USBC	0x30	USBC	AP_DATAOUT15	O
USBC	0x31	USBC	AP_DATAOUT16	O
USBC	0x32	USBC	AP_DATAOUT17	O
USBC	0x33	USBC	AP_DATAOUT18	O
USBC	0x34	USBC	AP_DATAOUT19	O
USBC	0x35	USBC	AP_DATAOUT20	O
USBC	0x36	USBC	AP_DATAOUT21	O
USBC	0x37	USBC	AP_DATAOUT22	O
USBC	0x38	USBC	AP_DATAOUT23	O
USBC	0x39	USBC	AP_DATAOUT24	O
USBC	0x3A	USBC	AP_DATAOUT25	O
USBC	0x3B	USBC	AP_DATAOUT26	O
USBC	0x3C	USBC	AP_DATAOUT27	O
USBC	0x3D	USBC	AP_DATAOUT28	O
USBC	0x3E	USBC	AP_DATAOUT29	O
USBC	0x3F	USBC	AP_DATAOUT30	O
USBC	0x40	USBC	AP_DATAOUT31	O
USBC	0x41	USBC	AP_DATAOUT32	O
USBC	0x51	USBC	AP_DATAIN0	S
USBC	0x52	USBC	AP_DATAIN1	S
USBC	0x53	USBC	AP_DATAIN2	S
USBC	0x54	USBC	AP_DATAIN3	S
USBC	0x55	USBC	AP_DATAIN4	S
USBC	0x56	USBC	AP_DATAIN5	S
USBC	0x57	USBC	AP_DATAIN6	S
USBC	0x58	USBC	AP_DATAIN7	S
USBC	0x59	USBC	AP_DATAIN8	S
USBC	0x5A	USBC	AP_DATAIN9	S
USBC	0x5B	USBC	AP_DATAIN10	S
USBC	0x5C	USBC	AP_DATAIN11	S
USBC	0x5D	USBC	AP_DATAIN12	S
USBC	0x5E	USBC	AP_DATAIN13	S
USBC	0x5F	USBC	AP_DATAIN14	S
USBC	0x60	USBC	AP_DATAIN15	S
USBC	0x61	USBC	AP_DATAIN16	S
USBC	0x62	USBC	AP_DATAIN17	S
USBC	0x63	USBC	AP_DATAIN18	S
USBC	0x64	USBC	AP_DATAIN19	S

USBC	0x65	USBC	AP_DATAIN20	S
USBC	0x66	USBC	AP_DATAIN21	S
USBC	0x67	USBC	AP_DATAIN22	S
USBC	0x68	USBC	AP_DATAIN23	S
USBC	0x69	USBC	AP_DATAIN24	S
USBC	0x6A	USBC	AP_DATAIN25	S
USBC	0x6B	USBC	AP_DATAIN26	S
USBC	0x6C	USBC	AP_DATAIN27	S
USBC	0x6D	USBC	AP_DATAIN28	S
USBC	0x6E	USBC	AP_DATAIN29	S
USBC	0x6F	USBC	AP_DATAIN30	S
USBC	0x70	USBC	AP_DATAIN31	S
USBC	0x71	USBC	AP_DATAIN32	S

ADDRESS	NAME	MSB							LSB
USBC_FUNC									
0x00	DEVICE_ID[7:0]	DeviceId[7:0]							
0x01	DEVICE_REV[7:0]	DeviceRev[7:0]							
0x02	FW_REV[7:0]	FwRev[7:0]							
0x03	FW_SUB_VER[7:0]	FwSubRev[7:0]							
0x04	UIC_INT[7:0]	APCmdResI	SYSMsgI	VBUSDetI	VbADCI	DCDTmoI	StopModeI	ChgTypI	AttachedHoldI
0x05	CC_INT[7:0]	VCONNOCPI	VSAFE0VI	DetAbrtI	WtrI	CCPinStatI	CCIStatI	CCVcnStatI	CCStatI
0x06	PD_INT[7:0]	PDMsgI	PSRDYI	DataRoleI	RSVD	RSVD	DisplayPortI	–	–
0x08	USBC_STATUS1[7:0]	VbADC[4:0]					RSVD[2:0]		
0x09	USBC_STATUS2[7:0]	SYSMsg[7:0]							
0x0A	BC_STATUS[7:0]	V_{BUSDet}	RSVD	PrChgTyp[2:0]			DCDTmo	ChgTyp[1:0]	
0x0C	CC_STATUS0[7:0]	CCPinStat[1:0]		CCIStat[1:0]		CCVcnStat	CCStat[2:0]		
0x0D	CC_STATUS1[7:0]	RSVD[1:0]		V_{CONN}OCP	V_{CONN}SC	VSafeOV	DetAbrt	Wtr	RSVD
0x0E	PD_STATUS0[7:0]	PDMsg[7:0]							
0x0F	PD_STATUS1[7:0]	DataRole	PowerRole	VCONNS	PSRDY	–	–	–	–
0x10	UIC_INT_M[7:0]	APCmdResM	SYSMsgM	VBUSDetM	VbADCM	DCDTmoM	StopModeM	ChgTypM	AttachedHoldM
0x11	CC_INT_M[7:0]	VCONNOCPM	VSAFE0VM	DetAbrtM	WtrM	CCPinStatM	CCIStatM	CCVcnStatM	CCStatM
0x12	PD_INT_M[7:0]	PDMsgM	PSRDYM	DataRoleM	RSVD	RSVD	DisplayPortM	–	–
0x21	AP_DATAOUT0[7:0]	AP_REQUEST_OPCODE[7:0]							
0x22	AP_DATAOUT1[7:0]	OPCODE_DATAOUT_01[7:0]							
0x23	AP_DATAOUT2[7:0]	OPCODE_DATAOUT_02[7:0]							

ADDRESS	NAME	MSB							LSB
0x24	AP_DATAOUT3[7:0]	OPCODE_DATAOUT_03[7:0]							
0x25	AP_DATAOUT4[7:0]	OPCODE_DATAOUT_04[7:0]							
0x26	AP_DATAOUT5[7:0]	OPCODE_DATAOUT_05[7:0]							
0x27	AP_DATAOUT6[7:0]	OPCODE_DATAOUT_06[7:0]							
0x28	AP_DATAOUT7[7:0]	OPCODE_DATAOUT_07[7:0]							
0x29	AP_DATAOUT8[7:0]	OPCODE_DATAOUT_08[7:0]							
0x2A	AP_DATAOUT9[7:0]	OPCODE_DATAOUT_09[7:0]							
0x2B	AP_DATAOUT10[7:0]	OPCODE_DATAOUT_10[7:0]							
0x2C	AP_DATAOUT11[7:0]	OPCODE_DATAOUT_11[7:0]							
0x2D	AP_DATAOUT12[7:0]	OPCODE_DATAOUT_12[7:0]							
0x2E	AP_DATAOUT13[7:0]	OPCODE_DATAOUT_13[7:0]							
0x2F	AP_DATAOUT14[7:0]	OPCODE_DATAOUT_14[7:0]							
0x30	AP_DATAOUT15[7:0]	OPCODE_DATAOUT_15[7:0]							
0x31	AP_DATAOUT16[7:0]	OPCODE_DATAOUT_16[7:0]							
0x32	AP_DATAOUT17[7:0]	OPCODE_DATAOUT_17[7:0]							
0x33	AP_DATAOUT18[7:0]	OPCODE_DATAOUT_18[7:0]							
0x34	AP_DATAOUT19[7:0]	OPCODE_DATAOUT_19[7:0]							
0x35	AP_DATAOUT20[7:0]	OPCODE_DATAOUT_20[7:0]							
0x36	AP_DATAOUT21[7:0]	OPCODE_DATAOUT_21[7:0]							
0x37	AP_DATAOUT22[7:0]	OPCODE_DATAOUT_22[7:0]							
0x38	AP_DATAOUT23[7:0]	OPCODE_DATAOUT_23[7:0]							
0x39	AP_DATAOUT24[7:0]	OPCODE_DATAOUT_24[7:0]							
0x3A	AP_DATAOUT25[7:0]	OPCODE_DATAOUT_25[7:0]							
0x3B	AP_DATAOUT26[7:0]	OPCODE_DATAOUT_26[7:0]							
0x3C	AP_DATAOUT27[7:0]	OPCODE_DATAOUT_27[7:0]							
0x3D	AP_DATAOUT28[7:0]	OPCODE_DATAOUT_28[7:0]							
0x3E	AP_DATAOUT29[7:0]	OPCODE_DATAOUT_29[7:0]							
0x3F	AP_DATAOUT30[7:0]	OPCODE_DATAOUT_30[7:0]							
0x40	AP_DATAOUT31[7:0]	OPCODE_DATAOUT_31[7:0]							
0x41	AP_DATAOUT32[7:0]	OPCODE_DATAOUT_32[7:0]							
0x51	AP_DATAIN0[7:0]	USBC_RESPONSE_OPCODE[7:0]							
0x52	AP_DATAIN1[7:0]	OPCODE_DATAIN_01[7:0]							
0x53	AP_DATAIN2[7:0]	OPCODE_DATAIN_02[7:0]							
0x54	AP_DATAIN3[7:0]	OPCODE_DATAIN_03[7:0]							
0x55	AP_DATAIN4[7:0]	OPCODE_DATAIN_04[7:0]							
0x56	AP_DATAIN5[7:0]	OPCODE_DATAIN_05[7:0]							
0x57	AP_DATAIN6[7:0]	OPCODE_DATAIN_06[7:0]							
0x58	AP_DATAIN7[7:0]	OPCODE_DATAIN_07[7:0]							
0x59	AP_DATAIN8[7:0]	OPCODE_DATAIN_08[7:0]							
0x5A	AP_DATAIN9[7:0]	OPCODE_DATAIN_09[7:0]							
0x5B	AP_DATAIN10[7:0]	OPCODE_DATAIN_10[7:0]							

ADDRESS	NAME	MSB							LSB
0x5C	AP_DATAIN11[7:0]	OPCODE_DATAIN_11[7:0]							
0x5D	AP_DATAIN12[7:0]	OPCODE_DATAIN_12[7:0]							
0x5E	AP_DATAIN13[7:0]	OPCODE_DATAIN_13[7:0]							
0x5F	AP_DATAIN14[7:0]	OPCODE_DATAIN_14[7:0]							
0x60	AP_DATAIN15[7:0]	OPCODE_DATAIN_15[7:0]							
0x61	AP_DATAIN16[7:0]	OPCODE_DATAIN_16[7:0]							
0x62	AP_DATAIN17[7:0]	OPCODE_DATAIN_17[7:0]							
0x63	AP_DATAIN18[7:0]	OPCODE_DATAIN_18[7:0]							
0x64	AP_DATAIN19[7:0]	OPCODE_DATAIN_19[7:0]							
0x65	AP_DATAIN20[7:0]	OPCODE_DATAIN_20[7:0]							
0x66	AP_DATAIN21[7:0]	OPCODE_DATAIN_21[7:0]							
0x67	AP_DATAIN22[7:0]	OPCODE_DATAIN_22[7:0]							
0x68	AP_DATAIN23[7:0]	OPCODE_DATAIN_23[7:0]							
0x69	AP_DATAIN24[7:0]	OPCODE_DATAIN_24[7:0]							
0x6A	AP_DATAIN25[7:0]	OPCODE_DATAIN_25[7:0]							
0x6B	AP_DATAIN26[7:0]	OPCODE_DATAIN_26[7:0]							
0x6C	AP_DATAIN27[7:0]	OPCODE_DATAIN_27[7:0]							
0x6D	AP_DATAIN28[7:0]	OPCODE_DATAIN_28[7:0]							
0x6E	AP_DATAIN29[7:0]	OPCODE_DATAIN_29[7:0]							
0x6F	AP_DATAIN30[7:0]	OPCODE_DATAIN_30[7:0]							
0x70	AP_DATAIN31[7:0]	OPCODE_DATAIN_31[7:0]							
0x71	AP_DATAIN32[7:0]	OPCODE_DATAIN_32[7:0]							
0x80	SW_RESET[7:0]	UIC_SWRST[7:0]							
I2C_FUNC									
0xE0	I2C_CNFG[7:0]	SPR_7	PAIR[2:0]			SPR_3_1[2:0]			HS_EXT_EN

Register Details

DEVICE_ID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DeviceId[7:0]							
Reset	0x58							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DeviceId	7:0	Device ID	0x00: Reserved 0x01: Reserved 0x58: MAX77958

DEVICE_REV (0x1)

BIT	7	6	5	4	3	2	1	0
Field	DeviceRev[7:0]							
Reset	0x02							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DeviceRev	7:0	FW Revision	0x01: Initial release 0x02: Second release

FW_REV (0x2)

BIT	7	6	5	4	3	2	1	0
Field	FwRev[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FwRev	7:0	FW Revision	0x00: Initial release 0x01: Second release

FW_SUB_VER (0x3)

BIT	7	6	5	4	3	2	1	0
Field	FwSubRev[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FwSubRev	7:0	FW Revision	0x00: Initial release 0x01: Second release

UIC_INT (0x4)

BIT	7	6	5	4	3	2	1	0
Field	APCmdResI	SYSMsgI	VBUSDetI	VbADCI	DCDTmoI	StopModeI	ChgTypI	AttachedHoldI
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
APCmdResI	7	AP Command Response Interrupt	0b0: No interrupt. 0b1: AP command response pending.
SYSMsgI	6	USBC System Message Interrupt	0b0: No interrupt. 0b1: USBC system message pending.
VBUSDetI	5	V_{BUS} Detection Interrupt	0b0: No interrupt. 0b1: New V_{BUSDet} status interrupt.

BITFIELD	BITS	DESCRIPTION	DECODE
VbADCI	4	V_{BUS} Voltage ADC Interrupt	0b0: No interrupt. 0b1: New VbADC status interrupt.
DCDTmoI	3	DCD Timer Interrupt	0b0: No interrupt. 0b1: New DCDTmo status interrupt.
StopModeI	2	Stop Mode Interrupt	0b0: No interrupt. 0b1: New stop mode status interrupt.
ChgTypI	1	Charger Type Interrupt	0b0: No interrupt. 0b1: New ChgTyp status interrupt.
AttachedHoldI	0	Attached Hold Interrupt	0b0: No interrupt. 0b1: New attached hold status interrupt.

CC_INT (0x5)

BIT	7	6	5	4	3	2	1	0
Field	VCONNOCPI	VSAFE0VI	DetAbrtI	WtrI	CCPinStatI	CCIStatI	CCVcnStatI	CCStatI
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VCONNOCPI	7	V_{CONN} OCP Interrupt	0b0: No interrupt. 0b1: New V_{CONN}OCP status interrupt.
VSAFE0VI	6	VSAFE0V Interrupt	0b0: No interrupt. 0b1: New VSAFE0V status interrupt.
DetAbrtI	5	CC Detection Abort Interrupt	0b0: No interrupt. 0b1: New CC detection abort interrupt.
WtrI	4	Moisture/Dry Interrupt	0b0: No interrupt. 0b1: New moisture/dry status interrupt.
CCPinStatI	3	CC Pin State Interrupt	0b0: No interrupt. 0b1: New CCPinStat status interrupt.
CCIStatI	2	CCIStat Interrupt	0b0: No interrupt. 0b1: New CCIStat status interrupt.
CCVcnStatI	1	CCVcnStat Interrupt	0b0: No interrupt. 0b1: New CCVcnStat status interrupt.
CCStatI	0	CCStat Interrupt	0b0: No interrupt. 0b1: New CCStat status interrupt.

PD_INT (0x6)

BIT	7	6	5	4	3	2	1	0
Field	PDMsgI	PSRDYI	DataRoleI	RSVD	RSVD	DisplayPortI	–	–
Reset	0b0	0b0	0b0	0b0	0b0	0x0	–	–
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Clears All	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PDMsgI	7	PD Message Interrupt	0b0: No interrupt. 0b1: New PD message issued.
PSRDYI	6	Spare	

BITFIELD	BITS	DESCRIPTION	DECODE
DataRoleI	5	Data Role Change Interrupt	0b0: No interrupt. 0b1: DataRole status is changed.
RSVD	4	Spare	
RSVD	3	Spare	
DisplayPortI	2	Display Port Interrupt	0x0: No interrupt. 0x1: New display port interrupt.

USBC_STATUS1 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VbADC[4:0]					RSVD[2:0]		
Reset	0x0					0b111		
Access Type	Read Only					Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
VbADC	7:3	Indicates Value on V_{BUS} Input	0x00: V_{BUS} < 3.5V 0x01: 3.5V ≤ V_{BUS} < 4.5V 0x02: 4.5V ≤ V_{BUS} < 5.5V 0x03: 5.5V ≤ V_{BUS} < 6.5V 0x04: 6.5V ≤ V_{BUS} < 7.5V 0x05: 7.5V ≤ V_{BUS} < 8.5V 0x06: 8.5V ≤ V_{BUS} < 9.5V 0x07: 9.5V ≤ V_{BUS} < 10.5V 0x08: 10.5V ≤ V_{BUS} < 11.5V 0x09: 11.5V ≤ V_{BUS} < 12.5V 0x0A: 12.5V ≤ V_{BUS} < 13.5V 0x0B: 13.5V ≤ V_{BUS} < 14.5V 0x0C: 14.5V ≤ V_{BUS} < 15.5V 0x0D: 15.5V ≤ V_{BUS} < 16.5V 0x0E: 16.5V ≤ V_{BUS} < 17.5V 0x0F: 17.5V ≤ V_{BUS} < 18.5V 0x10: 18.5V ≤ V_{BUS} < 19.5V 0x11: 19.5V ≤ V_{BUS} < 20.5V 0x12: 20.5V ≤ V_{BUS} < 21.5V 0x13: 21.5V ≤ V_{BUS} < 22.5V 0x14: 22.5V ≤ V_{BUS} < 23.5V 0x15: 23.5V ≤ V_{BUS} < 24.5V 0x16: 24.5V ≤ V_{BUS} < 25.5V 0x17: 25.5V ≤ V_{BUS} < 26.5V 0x18: 26.5V ≤ V_{BUS} < 27.5V 0x19: 27.5V ≤ V_{BUS} 0x1A: RSVD
RSVD	2:0		

USBC_STATUS2 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	SYSMsg[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
SYSMsg	7:0	SYSMsg	0x00: SYSERROR_NONE 0x01: Reserved 0x02: Reserved 0x03: SYSERROR_BOOT_WDT 0x04: SYSERROR_BOOT_SWRSTREQ 0x05: SYSMSG_BOOT_POR 0x10: SYSERROR_HV_NOVBUS 0x11: SYSERROR_HV_FMETHOD_RXPERR 0x12: SYSERROR_HV_FMETHOD_RXBUFOW 0x13: SYSERROR_HV_FMETHOD_RXTFR 0x14: SYSERROR_HV_FMETHOD_MPNACK 0x15: SYSERROR_HV_FMETHOD_RESET_FAIL 0x20: SYSMsg_AFC_Done 0x30: SYSERROR_SYSPOS 0x31: SYSERROR_APCMD_UNKNOWN 0x32: SYSERROR_APCMD_INPROGRESS 0x33: SYSERROR_APCMD_FAIL

BC_STATUS (0xA)

BIT	7	6	5	4	3	2	1	0
Field	V_{BUSDet}	RSVD	PrChgTyp[2:0]			DCDTmo	ChgTyp[1:0]	
Reset	0b0	0b0	0b000			0b0	0b00	
Access Type	Read Only	Read Only	Read Only			Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
V_{BUSDet}	7	Status of V_{BUS} Detection	0b0: $V_{BUS} < V_{BDET}$ 0b1: $V_{BUS} > V_{BDET}$
RSVD	6	Spare	
PrChgTyp	5:3	Output of Proprietary Charger Detection	0b000: Unknown 0b001: RSVD 0b010: RSVD 0b011: RSVD 0b100: RSVD 0b101: RSVD 0b110: 3A DCP (If enabled AND chgTyp=DCP) 0b111: Nikon TA (If enabled AND chgTyp=SDP)
DCDTmo	2	During Charger Detection, DCD Detection Timed Out. Indicates D+/D- are open. BC1.2 detection continues as required by BC1.2 specification but SDP most likely is found.	0b0: No timeout or detection has not run. 0b1: DCD timeout occurred.
ChgTyp	1:0	Output of Charger Detection	0b00: Nothing attached. 0b01: SDP, USB cable attached. 0b10: CDP, Charging Downstream Port: current depends on USB operating speed. 0b11: DCP, Dedicated Charger: current up to 1.5A.

CC_STATUS0 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	CCPinStat[1:0]		CCIStat[1:0]		CCVcnStat	CCStat[2:0]		
Reset	0b00		0b00		0b0	0b000		
Access Type	Read Only		Read Only		Read Only	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
CCPinStat	7:6	Output of Active CC Pin	0b00: No determination 0b01: CC1 Active 0b10: CC2 Active 0b11: RFU
CCIStat	5:4	CC Pin Detected and Allows V_{BUS} Current in UFP Mode	0b00: Not in UFP mode 0b01: 500mA 0b10: 1.5A 0b11: 3.0A
CCVcnStat	3	Status of V_{CONN} Output	0b0: V_{CONN} disabled 0b1: V_{CONN} enabled
CCStat	2:0	CC Pin State Machine Detection	0b000: No connection 0b001: SINK 0b010: SOURCE 0b011: Audio accessory 0b100: DebugSrc accessory 0b101: Error 0b110: Disabled 0b111: DebugSnk accessory

CC_STATUS1 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		V_{CONN} OCP	V_{CONN}SC	VSafeOV	DetAbrt	Wtr	RSVD
Reset	0b00		0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Spare	
V_{CONN} OCP	5	V_{CONN} Overcurrent Detection	0b0: V_{CONN} current < V_{CONN_ILIM} 0b1: V_{CONN} current > V_{CONN_ILIM}
V_{CONN}SC	4	V_{CONN} Short-Circuit Detection	0b0: V_{CONN} current < V_{CONN_SC} 0b1: V_{CONN} current > V_{CONN_SC}
VSafeOV	3	Status of V_{BUS} Detection. Valid only in Attached.SRC_CCx, Attached.SNK_CCx state.	0b0: V_{BUS} < V_{SAFE0V} 0b1: V_{BUS} > V_{SAFE0V}

BITFIELD	BITS	DESCRIPTION	DECODE
DetAbrt	2	Charger Detection Abort Status	0b0: Charger detection runs if CHGDetEn = 1 and V_{BUS} is valid for the debounce time. 0b1: Charger detection is aborted by USB Type-C State Machine. Charger does not run if CHGDetEn = 1 and V_{BUS} is valid for the debounce time. CHGDetMan allows manual run of charger detection. If charger detection is in progress, DetAbrt = 1 immediately stops the in progress detection.
Wtr	1	Moisture/Dry Status	0x0: Dry 0x1: Moisture
RSVD	0	Spare	

PD_STATUS0 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	PDMsg[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PDMsg	7:0	PD Message	0x00: Nothing happened 0x01: Sink_PD_PSRdy_received 0x02: Sink_PD_Error Recovery 0x03: Sink_PD_SenderResponseTimer_Timeout 0x04: Source_PD_PSRdy_Sent 0x05: Source_PD_Error Recovery 0x06: Source_PD_SenderResponseTimer_Timeout 0x07: PD_DR_Swap_Request_Received 0x08: PD_PR_Swap_Request_Received 0x09: PD_V_{CONN}_Swap_Request_Received 0x10: Samsung accessory is attached 0x11: VDM Attention message received

PD_STATUS1 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	DataRole	PowerRole	VCONNS	PSRDY	–	–	–	–
Reset	0b0	0b0	0b0	0b0	–	–	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DataRole	7	Current Data Role	0b0: UFP 0b1: DFP
PowerRole	6	Power Role	0b0: Sink 0b1: Source
VCONNS	5	VCONNS	0b0: V_{CONN} Sink 0b1: V_{CONN} Source
PSRDY	4	PSRDY Received as Sink	0b0: Nothing happened 0b1: PSRDY received

UIC_INT_M (0x10)

BIT	7	6	5	4	3	2	1	0
Field	APCmdResM	SYSMsgM	VBUSDetM	VbADCM	DCDTmoM	StopModeM	ChgTypM	AttachedHoldM
Reset	0b1	0b0	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
APCmdResM	7	APCmdRes Interrupt Mask	0b0: Unmask 0b1: Mask
SYSMsgM	6	SYSMsg Interrupt Mask	0b0: Unmask 0b1: Mask
VBUSDetM	5	VBUSDet Interrupt Mask	0 = Unmask 1 = Mask
VbADCM	4	VbADC Interrupt Mask	0 = Unmask 1 = Mask
DCDTmoM	3	DCDTmo Interrupt Mask	0 = Unmask 1 = Mask
StopModeM	2	Fake V_{BUS} Interrupt Mask	
ChgTypM	1	ChgTyp Interrupt Mask	0 = Unmask 1 = Mask
AttachedHoldM	0	UIDADC Interrupt Mask	0 = Unmask 1 = Mask

CC_INT_M (0x11)

BIT	7	6	5	4	3	2	1	0
Field	VCONNOCPM	VSAFE0VM	DetAbrtM	WtrM	CCPinStatM	CCIStatM	CCVcnStatM	CCStatM
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VCONNOCPM	7	VCONNOCP Interrupt Mask	0b0: Unmask 0b1: Mask
VSAFE0VM	6	VSAFE0V Interrupt Mask	0b0: Unmask 0b1: Mask
DetAbrtM	5	DetAbrt Interrupt Mask	0b0: Unmask 0b1: Mask
WtrM	4	Wtr Interrupt Mask	0b0: Unmask 0b1: Mask
CCPinStatM	3	CCPinStat Interrupt Mask	0b0: Unmask 0b1: Mask
CCIStatM	2	CCIStat Interrupt Mask	0b0: Unmask 0b1: Mask
CCVcnStatM	1	CCVcnStat Interrupt Mask	0b0: Unmask 0b1: Mask

BITFIELD	BITS	DESCRIPTION	DECODE
CCStatM	0	CCStat Interrupt Mask	0b0: Unmask 0b1: Mask

PD_INT_M (0x12)

BIT	7	6	5	4	3	2	1	0
Field	PDMsgM	PSRDYM	DataRoleM	RSVD	RSVD	DisplayPortM	–	–
Reset	0b1	0b1	0b1	0b1	0b1	0b1	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PDMsgM	7	PDMsg Interrupt Mask	0b0: Unmask 0b1: Mask
PSRDYM	6	PDRDY Interrupt Mask	
DataRoleM	5	DataRole Interrupt Mask	0b0: Unmask 0b1: Mask
RSVD	4	Display Port Attention Interrupt Mask	0b0: Unmask 0b1: Mask
RSVD	3	Display Port Configure Interrupt Mask	0b0: Unmask 0b1: Mask
DisplayPortM	2	Display Port Interrupt Mask	

AP_DATAOUT0 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	AP_REQUEST_OPCODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AP_REQUEST_OPCODE	7:0	All configuration and control commands to the USBC are sent and received as a packet using an opcode to identify the packet. **A. Messages sent to the USBC** • 0x21—Opcode sent to USBC. • 0x22 to 0x41—Message sent to USBC. • Message size can be as short as 1 byte (Opcode only) and up to 33 bytes (Opcode plus 32 bytes). But all messages must write to all bytes even if the rest of the message is stuffed with 0s. • Registers 0x21 to 0x41 act as a scratch pad for writing the message to the USBC. The message is latched in when a value is written to register 0x41. • All messages are acknowledged by the USBC by sending and generating an interrupt. • Data written to 0x21 to 0x41 is not auto cleared—the data remains in the registers until the application processor overwrites it with a new message. **B. Messages received from USBC** • 0x51—Opcode identifying the message type. • 0x52 to 0x71—Message sent to application processor. • Message size can be as short as 1 byte (Opcode only) and up to 33 bytes (Opcode plus 32 bytes). • Data written to 0x51 to 0x71 is not auto cleared—the data remains in the registers until the USBC overwrites them with a new message.

AP_DATAOUT1 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_01[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_01	7:0	

AP_DATAOUT2 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_02[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_02	7:0	

AP_DATAOUT3 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_03[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_03	7:0	

AP_DATAOUT4 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_04[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_04	7:0	

AP_DATAOUT5 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_05[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_05	7:0	

AP_DATAOUT6 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_06[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_06	7:0	

AP_DATAOUT7 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_07[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_07	7:0	

AP_DATAOUT8 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_08[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_08	7:0	

AP_DATAOUT9 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_09[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_09	7:0	

AP_DATAOUT10 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_10	7:0	

AP_DATAOUT11 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_11	7:0	

AP_DATAOUT12 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_12	7:0	

AP_DATAOUT13 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_13	7:0	

AP_DATAOUT14 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_14	7:0	

AP_DATAOUT15 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_15	7:0	

AP_DATAOUT16 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_16[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_16	7:0	

AP_DATAOUT17 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_17[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_17	7:0	

AP_DATAOUT18 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_18[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_18	7:0	

AP_DATAOUT19 (0x34)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_19[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_19	7:0	

AP_DATAOUT20 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_20[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_20	7:0	

AP_DATAOUT21 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_21[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_21	7:0	

AP_DATAOUT22 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_22[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_22	7:0	

AP_DATAOUT23 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_23[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_23	7:0	

AP_DATAOUT24 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_24[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_24	7:0	

AP_DATAOUT25 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_25[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_25	7:0	

AP_DATAOUT26 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_26[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_26	7:0	

AP_DATAOUT27 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_27[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_27	7:0	

AP_DATAOUT28 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_28[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_28	7:0	

AP_DATAOUT29 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_29[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_29	7:0	

AP_DATAOUT30 (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_30[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_30	7:0	

AP_DATAOUT31 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_31[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_31	7:0	

AP_DATAOUT32 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAOUT_32[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAOUT_32	7:0	

AP_DATAIN0 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	USBC_RESPONSE_OPCODE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
USBC_RESPONSE_OPCODE	7:0	

AP_DATAIN1 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_01[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_01	7:0	

AP_DATAIN2 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_02[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_02	7:0	

AP_DATAIN3 (0x54)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_03[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_03	7:0	

AP_DATAIN4 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_04[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_04	7:0	

AP_DATAIN5 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_05[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_05	7:0	

AP_DATAIN6 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_06[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_06	7:0	

AP_DATAIN7 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_07[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_07	7:0	

AP_DATAIN8 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_08[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_08	7:0	

AP_DATAIN9 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_09[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_09	7:0	

AP_DATAIN10 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_10[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_10	7:0	

AP_DATAIN11 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_11[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_11	7:0	

AP_DATAIN12 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_12[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_12	7:0	

AP_DATAIN13 (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_13[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_13	7:0	

AP_DATAIN14 (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_14[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_14	7:0	

AP_DATAIN15 (0x60)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_15[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_15	7:0	

AP_DATAIN16 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_16	7:0	

AP_DATAIN17 (0x62)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_17[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_17	7:0	

AP_DATAIN18 (0x63)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_18[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_18	7:0	

AP_DATAIN19 (0x64)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_19[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_19	7:0	

AP_DATAIN20 (0x65)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_20[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_20	7:0	

AP_DATAIN21 (0x66)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_21[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_21	7:0	

AP_DATAIN22 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_22[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_22	7:0	

AP_DATAIN23 (0x68)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_23[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_23	7:0	

AP_DATAIN24 (0x69)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_24[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_24	7:0	

AP_DATAIN25 (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_25[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_25	7:0	

AP_DATAIN26 (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_26[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_26	7:0	

AP_DATAIN27 (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_27[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_27	7:0	

AP_DATAIN28 (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_28[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_28	7:0	

AP_DATAIN29 (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_29[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_29	7:0	

AP_DATAIN30 (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_30[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_30	7:0	

AP_DATAIN31 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_31[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_31	7:0	

AP_DATAIN32 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	OPCODE_DATAIN_32[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OPCODE_DATAIN_32	7:0	

SW_RESET (0x80)

BIT	7	6	5	4	3	2	1	0
Field	UIC_SWRST[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
UIC_SWRST	7:0	UIC (and MAXQ) Software Reset	When AP writes 0x0F, UIC is reset (registers and MAXQ).

I2C_CNFG (0xE0)

Spare mask register.

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	PAIR[2:0]			SPR_3_1[2:0]			HS_EXT_EN
Reset	0b0	0b000			0b000			0b0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Spare	

BITFIELD	BITS	DESCRIPTION	DECODE
PAIR	6:4	I2C Pair Address Mode Control	PAIR[2]: Pair address mode of Shared Bus 3 channel: Slave ID 3 Functional Pair address mode option at burst write operation on customer registers. 1 = Pair address mode is enabled for the channel. 0 = Pair address mode is disabled and sequential mode is used. PAIR[1]: Pair address mode of Shared Bus 2 channel: Slave ID 2 Functional Pair address mode option at burst write operation on customer registers. 1 = Pair address mode is enabled for the channel. 0 = Pair address mode is disabled and sequential mode is used. PAIR[0]: Pair address mode of Shared Bus 1 channel: Slave ID 1 Functional Pair address mode option at burst write operation on customer registers. 1 = Pair address mode is enabled for the channel. 0 = Pair address mode is disabled and sequential mode is used.
SPR_3_1	3:1	Spare	
HS_EXT_EN	0	HS-mode Extension Control	0x0: HS-mode Extension is disabled. (I2C Rev. 4 Compliant) 0x1: HS-mode Extension is enabled. HS-mode is enabled without HS-mode entrance code and keeps HS-mode during STOP condition.

Typical Application Circuits

2/3-Cell Configurable Charger Application

Figure 11 illustrates a configurable charger application diagram using the MAX77958 and buck-boost charger devices. In this application, the USB Type-C connector is used for SINK as well as SOURCE. The SINK role is automatically active when the battery is charged using USB Type-C SOURCE that is connected to the USB Type-C connector in Figure 11. Based on the CC detection result, the SOURCE advertises its capability. The IC negotiates power contract with the SOURCE connected to the USB Type-C connector. AP can choose appropriate SOURCE PDO and configure charging current in the buck-boost charger accordingly.

The SOURCE role is active when SINK device is attached to the UBS Type-C connector as shown in Figure 11. The IC becomes a power provider with the SOURCE role and advertises its capability to a device connected to USB Type-C connector.

In this scenario, AP configures the buck-boost charger as reverse-buck mode to provide OTG voltage to the device connected to the USB Type-C connector. The communication between the IC.

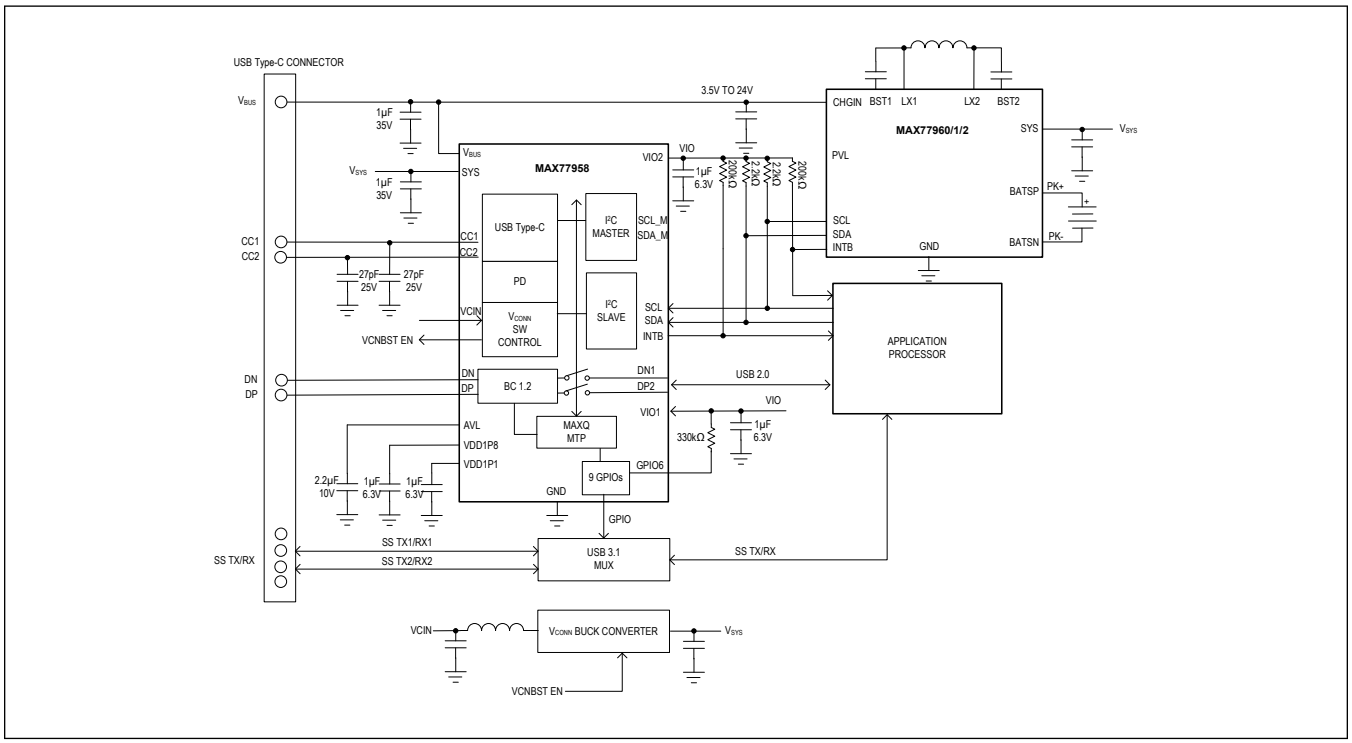


Figure 11. Configurable Charger Application

Typical Application Circuits (continued)

2/3-Cell Autonomous Charger Application

Figure 12 illustrates an autonomous charger application diagram using the MAX77958 and a buck-boost charger device. In this application, the USB Type-C connector is used for SINK as well as SOURCE. The SINK role is automatically active when the battery is charged using the USB Type-C SOURCE that is connected to the USB Type-C connector. Based on the CC detection result, the SOURCE advertises its capability. The IC negotiates a power contract with the SOURCE connected to the USB Type-C connector. The IC chooses an appropriate SOURCE PDO, and configures charging current in the buck-boost charger accordingly through the master I2C interface in the IC.

The SOURCE role is active when a SINK device is attached to the USB Type-C connector as shown in Figure 12. The IC becomes a power provider with the SOURCE role and advertises its capability to a device connected to USB Type-C connector. In this scenario, the IC configures the buck-boost charger to reverse-buck mode to provide OTG voltage to the device connected to the USB Type-C connector.

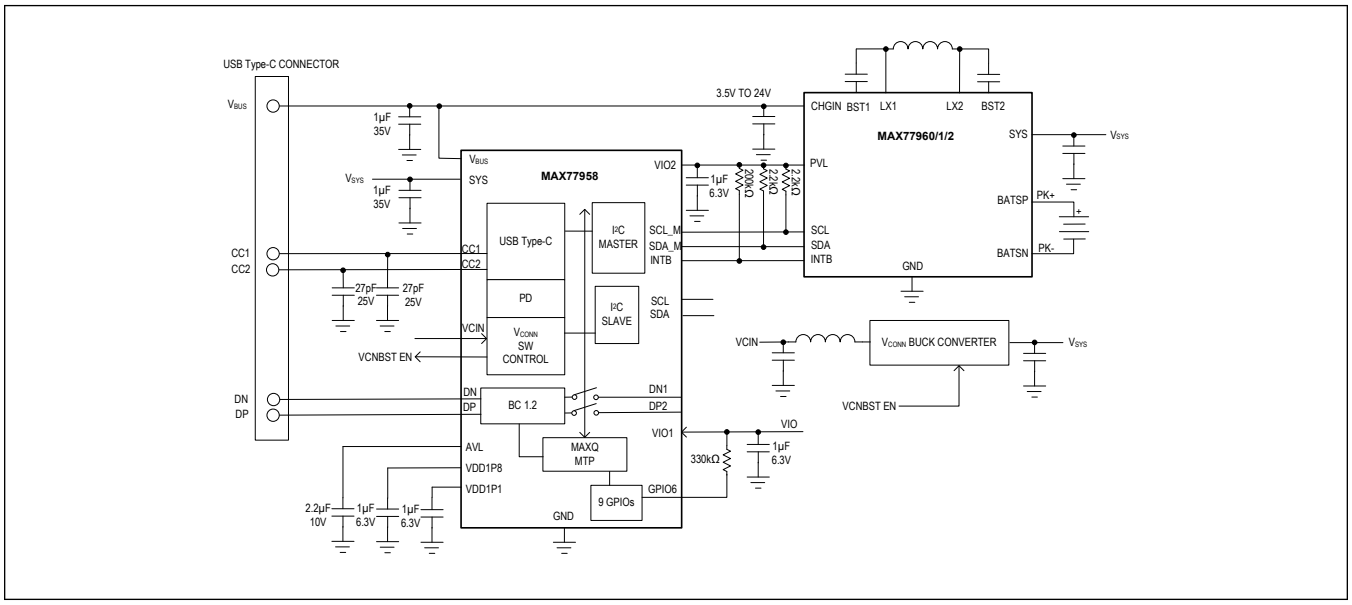


Figure 12. Autonomous Charger Application

Typical Application Circuits (continued)

Autonomous DC-DC Application

Figure 13 illustrates an autonomous DC-DC application diagram using the MAX77958. In this application, the USB Type-C connector is used for SINK. Based on the CC detection result, the SOURCE advertises its capability. The IC negotiates a power contract with the SOURCE connected to the USB Type-C connector. The IC chooses an appropriate SINK PDO among PDOs as shown in Figure 13. The IC then sets the Enable on the DC-DC converter to supply power to the application device.

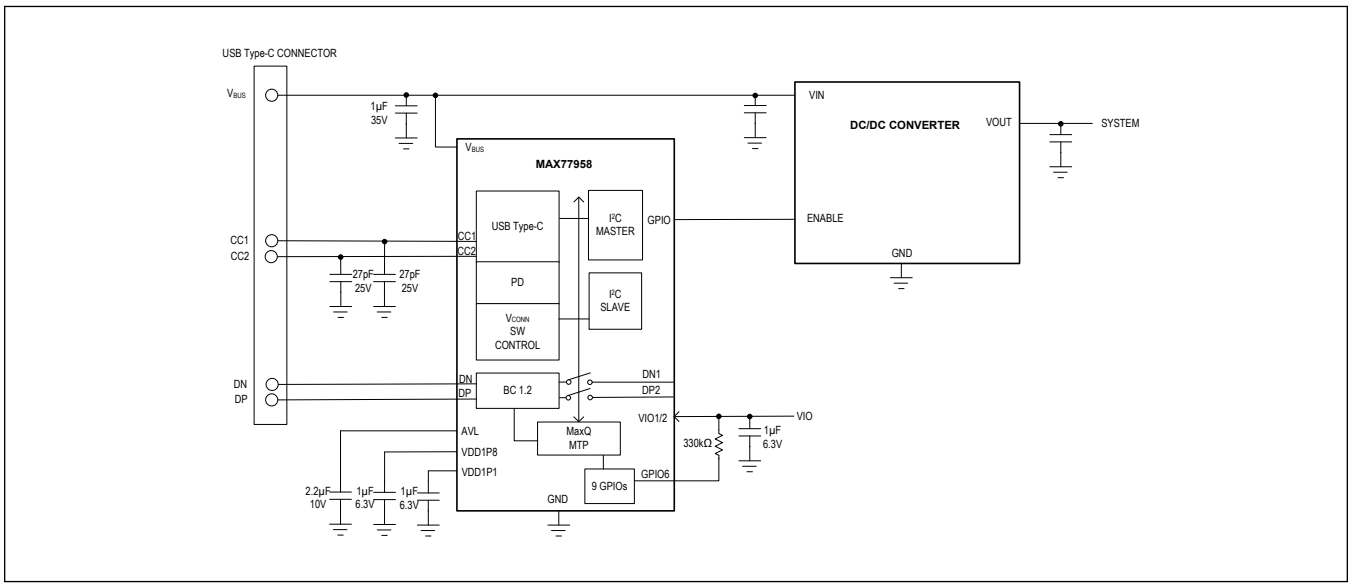


Figure 13. Autonomous DC-DC Application

Typical Application Circuits (continued)

PD Power Adapter Application

Figure 14 illustrates an adapter application diagram using the MAX77958 device. In this application, the USB Type-C connector is only used for SOURCE. The IC negotiates a power contract with the SINK connected to the USB Type-C connector. When SINK is attached, the IC advertises its SOURCE PDO to the SINK. Based on contracts, the IC controls GPIOs to adjust V_{BUS} that the SINK is requesting. When disconnection happens, the IC also controls GPIOs to disconnect the power path on the V_{BUS} path and discharges capacitors on the V_{BUS} path to meet the USB Type-C specification.

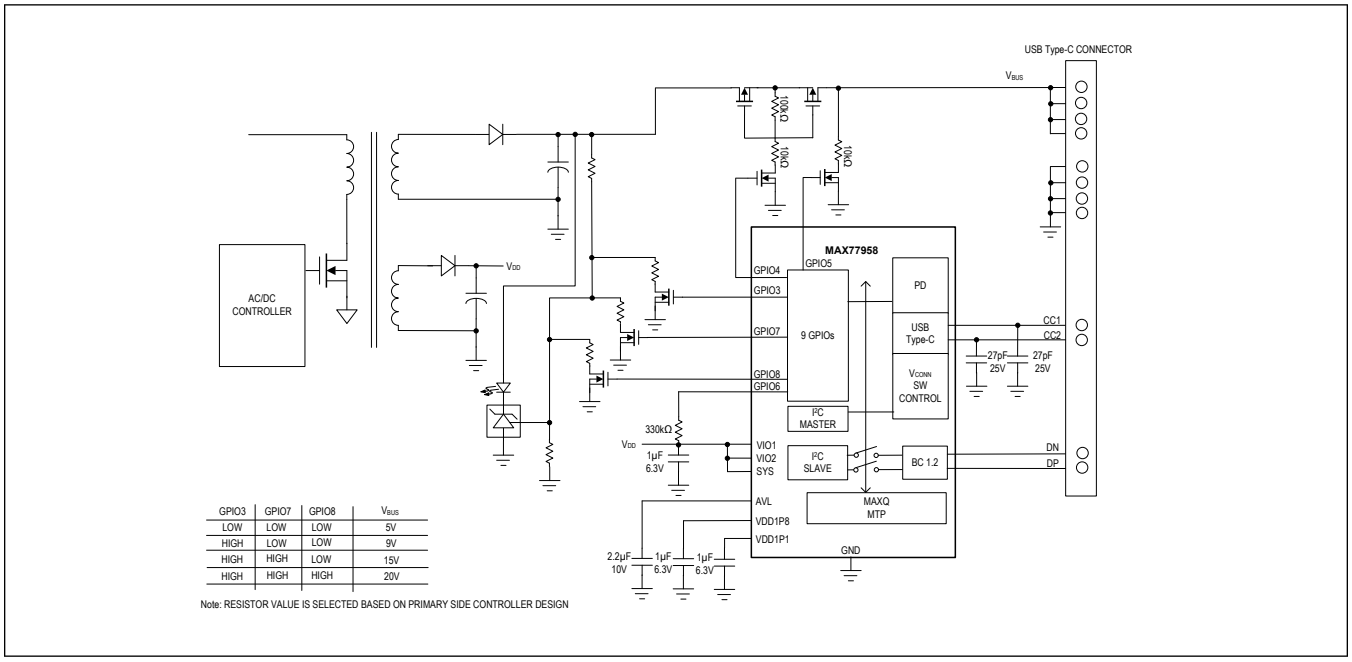


Figure 14. Adapter Application

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77958EWV+T	-40°C to +85°C	6x5 WLP, 0.5mm pitch, 3.1mm x 2.65mm
MAX77958EWV+	-40°C to +85°C	6x5 WLP, 0.5mm pitch, 3.1mm x 2.65mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/19	Initial release	—
1	4/20	Updated data sheet title, updated V_{CIN_OK} and added *USB Type-C/MTP* section to the *Electrical Characteristics* table, updated AVL in the *Pin Description* section, updated the *Detailed Description* and *Register Map* sections, updated *Typical Application Circuits* Figures 11, 12, and 13	1–73