ANALOG DEVICES

Ultra-Low Offset Voltage Operational Amplifier

OP-07

1.0 SCOPE

This specification covers the detail requirements for an ultra-low-offset voltage operational amplifier.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 **Part Number.** The complete part numbers per Table I of this specification follow:

Device	Part Number	Package
X	OP-07J/883	J
A	OP-07AJ/883	J
X	OP-07Z/883	Z
A	OP-07AZ/883	Z
X	OP-07RC/883	RC

1.2.3 **Case Outline.**

Letter	Case Outline (Lead finish per MIL-M-38510)
J	8-lead metal can (TO-99)
Z	8-lead ceramic dual-in-line package (CERDIP)
RC	20-contact hermetic leadless chip carrier (LCC)

1.3 **Absolute Maximum Ratings.** (T_A = 25°C, unless otherwise noted)

Supply Voltage ..... ±22V
Internal Power Dissipation 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Operating Temperature Range ..... -55°C to +125°C
DICE Junction Temperature Range (T_J) ..... -65°C to +150°C

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltages.

1.5 Thermal Characteristics:

Thermal Resistance, TO-99 (J) package:
Junction-to-Case (Θ_{JC}) = 45°C/W MAX
Junction-to-Ambient (Θ_{JA}) = 150°C/W MAX

Thermal Resistance, CERDIP (Z) package:
Junction-to-Case (Θ_{JC}) = 26°C/W MAX
Junction-to Ambient (Θ_{JA}) = 119°C/W MAX

Thermal Resistance, LCC (RC) package:
Junction-to-Case (Θ_{JC}) = 35°C/W MAX
Junction-to-Ambient (Θ_{JA}) = 110°C/W MAX

TABLE 1

V_S = ±15V; R_S = 50Ω; T_A = 25°C unless otherwise specified.

Characteristics	Symbol	Special Conditions	OP-07/883 LIMITS A Min	LIMITS A Max	LIMITS X Min	LIMITS X Max	Units
Input Offset Voltage	V_{OS}		–	25	–	75	µV
		-55°C ≤ T_A ≤ +125°C	–	60	–	200	µV
Average Offset Voltage Drift	TCV_{OS}	-55°C ≤ T_A ≤ +125°C	–	0.6	–	1.3	µV/°C
Input Offset Current	I_{OS}		–	2.0	–	2.8	nA
		-55°C ≤ T_A ≤ +125°C	–	4.0	–	5.6	nA
Input Bias Current	I_B		–	±2.0	–	±3.0	nA
		-55°C ≤ T_A ≤ +125°C	–	±4.0	–	±6.0	nA
Output Voltage Swing	V_O	R_L ≥ 10kΩ	±12.5	–	±12.5	–	V
		R_L ≥ 2kΩ	±12.0	–	±12.0	–	V
		R_L ≥ 1kΩ	±10.5	–	±10.5	–	V
		R_L ≥ 2kΩ -55°C ≤ T_A ≤ +125°C	±12.0	–	±12.0	–	V
Supply Current	I_{SY}	No Load	–	4	–	4	mA
		No Load, V_S = ±3V	–	1	–	1	mA
Power Dissipation	P_d	No Load	–	120	–	120	mW
		No Load, V_S = ±3V	–	6	–	6	mW
Slew Rate	SR	R_L ≥ 2kΩ, C_L = 50pF	0.1	–	0.1	–	V/µs
Input Voltage Range (Note 1)	IVR		±13	–	±13	–	V
		-55°C ≤ T_A ≤ +125°C	±13	–	±13	–	V
Common-Mode Rejection	CMR	V_{CM} = IVR = ±13V	110	–	110	–	dB
		V_{CM} = IVR = ±13V -55°C ≤ T_A ≤ +125°C	106	–	106	–	dB

TABLE 1 (Continued)

V_S = ±15V; R_S = 50Ω; T_A = 25°C unless otherwise specified.

Characteristics	Symbol	Special Conditions	OP-07/883 LIMITS A Min	OP-07/883 LIMITS A Max	OP-07/883 LIMITS X Min	OP-07/883 LIMITS X Max	Units
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	--	10	--	10	µV/V
		V_S = ±3V to ±18V -55°C ≤ T_A ≤ +125°C	--	20	--	20	µV/V
Input Noise Voltage (Note 2)	e_n	f_O = 1Hz to 100Hz	--	150	--	150	nV_{RMS}
Input Noise Current (Note 2)	i_n	f_O = 1Hz to 100Hz	--	8	--	8	pA_{RMS}
Open-Loop Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	300	--	200	--	V/mV
		R_L ≥ 2kΩ, V_O = ±10V -55°C ≤ T_A ≤ +125°C	200	--	150	--	V/mV
Small-Signal Bandwith	BW	A_{VCL} = +1	0.4	--	0.4	--	MHz
Input Offset Adjustment	V_{OS}adj+	R_p = 20kΩ	0.5	--	0.5	--	mV
	V_{OS}adj-	R_p = 20kΩ	--	-0.5	--	-0.5	mV
Output Short Circuit	I_{SC}^+		--	58	--	58	mA
	I_{SC}^-		-50	--	-50	--	mA

NOTES:
1. IVR is defined as the V_{CM} range used for the CMR test.
2. This parameter is 100% tested.

TABLE 2

OP-07/883

Electrical Test Requirements
For Class B Devices

MIL-STD-883 Test Requirements	Subgroups (see Table 3)
Interim Electrical Parameters (pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4
Group A Test Requirements	1, 2, 3, 4, 7, 8

* PDA applies to Subgroup 1 only.
No other Subgroups are included in PDA.
V_{OS} is excluded from PDA calculation.

TABLE 3

Group A Inspection

V_S = ±15V; R_S = 50Ω; T_A = T_J unless otherwise specified.

			OP-07/883				
			LIMITS A		LIMITS X		
Subgroup	Symbol	Special Conditions	Min	Max	Min	Max	Units
Subgroup 1	I_{OS}		–	2.0	–	2.8	nA
T_A = +25°C	I_B		–	±2.0	–	±3.0	nA
	CMR	V_{CM} = ±13V	110	–	110	–	dB
	PSRR	V_S = ±3V, ±18V	–	10	–	10	μV/V
	A_{VO}	R_L = 2kΩ, V_O = ±10V	300	–	200	–	V/mV
	V_O	R_L = 10kΩ	±12.5	–	±12.5	–	V
		R_L = 2kΩ	±12.0	–	±12.0	–	V
		R_L = 1kΩ	±10.5	–	±10.5	–	V
	P_d	No Load	–	120	–	120	mW
		No Load, V_S = ±3V	–	6	–	6	mW
	V_{OS}adj+	R_p = 20kΩ	0.5	–	0.5	–	mV
	V_{OS}adj-	R_p = 20kΩ	–	-0.5	–	-0.5	mV
	I_{SC}^+		–	58	–	58	mA
	I_{SC}^-		-50	–	-50	–	mA
Subgroup 2	I_{OS}		–	4.0	–	5.6	nA
T_A = +125°C	I_B		–	±4.0	–	±6.0	nA
	CMR	V_{CM} = ±13V	106	–	106	–	dB
	PSRR	V_S = ±3V, ±18V	–	20	–	20	μV/V
	A_{VO}	R_L = 2kΩ, V_O = ±10V	200	–	150	–	V/mV
	V_O	R_L = 2kΩ	+12	–	+12	–	V

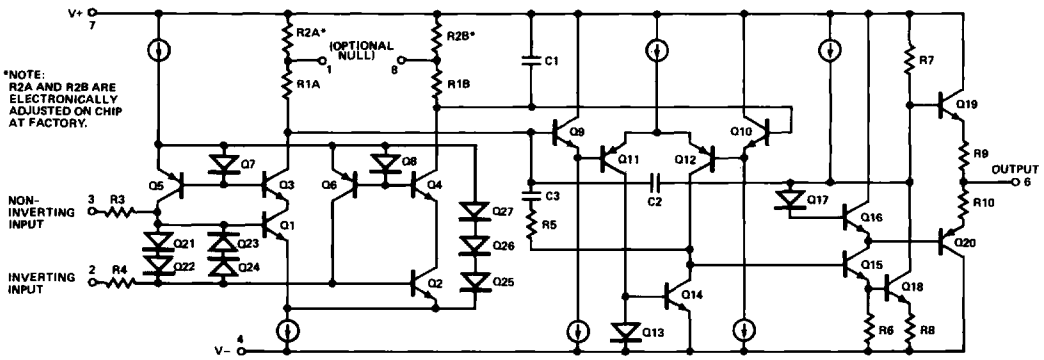
TABLE 3

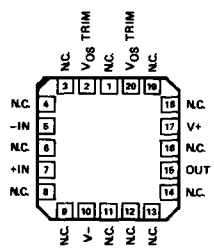
Group A Inspection (Continued)

V_S = ±15V; R_S = 50Ω; T_A = T_J unless otherwise specified.

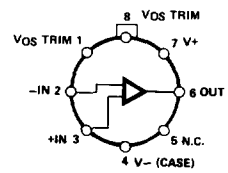
			OP-07/883				
			LIMITS A		LIMITS X		
Subgroup	Symbol	Special Conditions	Min	Max	Min	Max	Units
Subgroup 2 T_A = +125°C (Continued)	V_{OS}		–	60	–	200	µV
Subgroup 3 T_A = -55°C		All Tests, Limits and Conditions are the same as for Subgroup 2.					
Subgroup 4 T_A = +25°C	V_{OS}		–	25	–	75	µV
Subgroup 7	BW	A_{VCL} = +1	0.4	–	0.4	–	MHz
T_A = +25°C	SR	R_L = 2kΩ, C_L = 50pF	0.1	–	0.1	–	V/µs
Subgroup 8 -55°C ≤ T_A ≤ +125°C	TCV_{OS}		–	0.6	–	1.3	µV/°C

3.2.1 Simplified Schematic and Pin Connections.

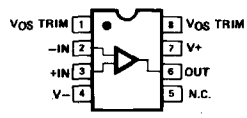




OP-07BRC/883
LCC
(RC-Suffix)



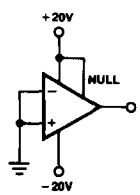
TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

3.2.4 Microcircuit Group Assignment. This microcircuit is covered by microcircuit group 49.

4.2 Life Test/Burn-In Circuit.



J AND Z PACKAGES