Click here for production status of specific part numbers.

MAX38907/MAX38908/ MAX38909

4A/2A High-Performance LDO Linear Regulators

General Description

The MAX38907/MAX38908/MAX38909 are fast transient response, high PSRR NMOS linear regulators that deliver up to 4A load current.

These regulators support a wide input supply range from 0.9V up to 5.5V, and BIAS voltage range from 2.7V to 20V to provide wider supply options in a variety of applications. ±1% output accuracy is maintained over line, load, and temperature variations, requiring only 300mV of input-to-output headroom at full load for a good PSRR. The output voltage can be adjusted to a value in the range of 0.6V to 5.0V to accommodate customers that desire to specify a single LDO in the BOM for multiple voltage rails.

The MAX38907 is configurable to one of 27 output voltages using three digital configuration pins. Additionally, each output voltage selection can be adjusted ±5% for margining. The output voltage on the MAX38908/MAX38909 can be adjusted to a value in the range of 0.6V to 5.0V by using two external feedback resistors. These LDOs are fully protected from damage by internal circuitry that provides programmable inrush current limiting, output overcurrent limiting, reverse-current limiting, and thermal overload protection.

The MAX38907 is offered in a 20-pin, 5mm x 5mm TQFN package, while the MAX38908/MAX38909 are offered in 14-pin, 3mm x 3mm TDFN and 5 x 3 bump, 0.4mm pitch WLP packages.

Applications

- FPGAs and DSPs
- Medical, Audio, and Instrumentation
- Server µPs
- Portable Cameras
- PLCs
- Base Stations

Benefits and Features

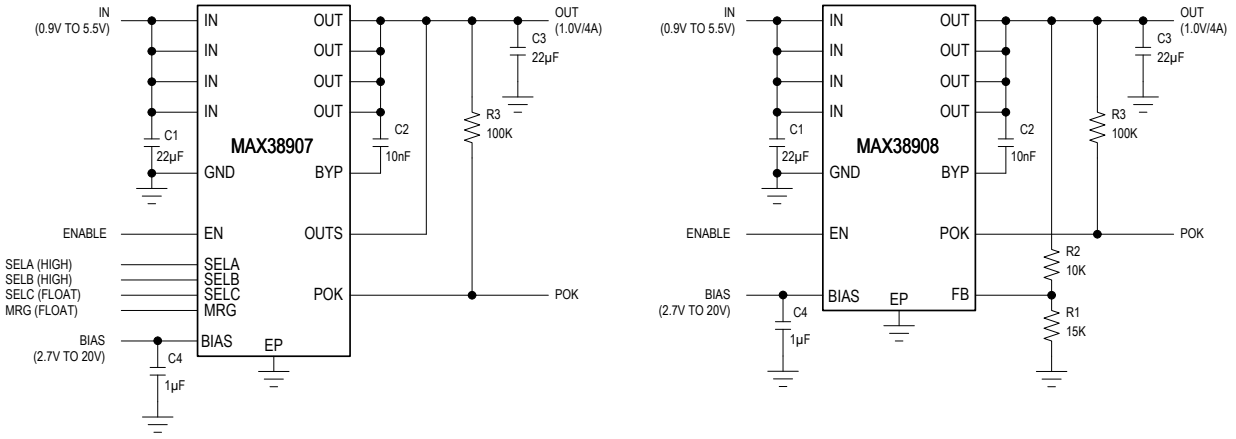
- Delivers Flexible Operating Range
  - 0.9V to 5.5V Input Voltage Range
  - 2.7V to 20V BIAS Voltage Range
  - 0.6V to 5.0V Programmable Output Voltage
  - 4A Maximum Output Current
  - 82mV Dropout at 4A Load Current
  - 1.6mA Operating BIAS Supply Current
- Reduces Noise and Improves Accuracy
  - ±1% DC Accuracy Over Load, Line, and Temperature
  - 28mV 4A Load Transient Excursion
  - 78dB BIAS PSRR at 10kHz
  - 52dB IN PSRR at 10kHz
- Enables Ease-of-Use and Robust Protection
  - Stable with 10µF (Minimum) Output Capacitance
  - Programmable Soft-Start Rate
  - Overcurrent and Overtemperature Protection
  - Output-to-Input Reverse Current Protection
  - Power-OK Status Pin
- Reduces Size, Improves Reliability
  - 14-pin (3mm x 3mm) TDFN, 20-pin (5mm x 5mm) TQFN, and 5 x 3 Bump, 0.4mm Pitch WLP Packages
  - -40°C to 125°C Operating Temperature

***Ordering Information* appears at end of data sheet.**

19-100604; Rev 0; 7/19

maxim integrated™

Typical Application Circuits



Absolute Maximum Ratings

IN, FB, OUT, OUTS, BYP, POK, MRG to GND..... -0.3V to +6V
BIAS to GND ..... -0.3V to +22V
EN, SELA, SELB, SELC to GND..... -0.3V to BIAS + 0.3V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C) .
TDFN (derate 24.4mW/°C, T_A = +70°C)..... 1951.2mW
TQFN (derate 33.3mW/°C, T_A = +70°C).....2666.7mW
WLP (derate 16.2mW/°C, T_A = +70°C).....1312mW
Operating Temperature Range.....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (Soldering, 10 second) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

14 TDFN

Package Code	T1433+2C
Outline Number	21-0137
Land Pattern Number	90-0063
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

20 TQFN

Package Code	T2055+4C
Outline Number	21-0140
Land Pattern Number	90-0009
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

WLP

Package Code	N151C2+1
Outline Number	21-100372
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θJA)	61.65°C/W
Junction-to-Case Thermal Resistance (θJC)	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 1.5V, V_{OUT} = 1.0V, V_{BIAS} = 10V, T_J = -40°C to +125°C, C_{IN} = 22µF, C_{OUT} = 22µF)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by Output Accuracy, $V_{OUT} < V_{IN} - V_{DO}$		0.9		5.5	V
Bias Voltage Range	V_{BIAS}			2.7		20	V
Input Undervoltage Lockout	V_{IN_UVLO}	V_{IN} rising, 60mV hysteresis		0.35	0.45	0.55	V
Bias Undervoltage Lockout	V_{BIAS_UVLO}	V_{BIAS} rising, 100mV hysteresis		2.45	2.55	2.65	V
Output Voltage Range	V_{OUT}	Guaranteed by Output Accuracy		0.6		5.0	V
Output Capacitance	C_{OUT}	For stability and proper operation		10	22		µF
Input Supply Current	I_Q	V_{EN} = 3.6V, V_{BIAS} = 5.0V, I_{OUT} = 0mA			70.5	150	µA
Input Shutdown Current	I_{SD}	V_{EN} = 0V	T_J = +25°C		0.001	1	µA
			T_J = +125°C		1		
Bias Supply Current	I_{BIAS}	V_{EN} = 3.3V, V_{BIAS} = 5.0V, I_{OUT} = 0mA			1.5	4	mA
		V_{EN} = 3.3V, V_{BIAS} = 5.0V, I_{OUT} = 4A			1.6		
	I_{BIAS_SD}	V_{EN} = 0V			0.75	4	µA
Output Accuracy (MAX38907)	ACC	I_{OUT} from 10mA to 4A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{BIAS} > 2.7V, V_{BIAS} from V_{OUT} + 2V to 20V, V_{OUT} from 0.6V to 5.0V		-1		+1	%
Feedback Voltage Accuracy (MAX38908 and MAX38909)	V_{FB}	I_{OUT} from 10mA to 4A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{BIAS} > 2.7V, V_{BIAS} from V_{OUT} + 2V to 20V, V_{OUT} from 0.6V to 5.0V		0.594	0.6	0.606	V
Load Regulation		I_{OUT} from 0.1mA to 4A			0.1		%
Load Transient		I_{OUT} = 40mA to 4A and 4A to 40mA, di/dt = 1A/µs, C_{OUT} = 3 x 10µF			28		mV
Line Regulation		V_{IN} from V_{OUT} + 0.3V to 5.5V, I_{OUT} = 1A			0.04		%/V
Line Transient		V_{IN} = 1.0V to 1.2V to 1.0V, 10V/ms V_{IN} Slew Rate, I_{OUT} = 4A, V_{OUT} = 0.8V			8.2		mV
Dropout Voltage (MAX38908) (Note 2)	V_{DO}	I_{OUT} = 4A, V_{OUT_NOM} = 1.2V	V_{BIAS} = 5.0V		85	150	mV
			V_{BIAS} = 3.3V		110	210	
		I_{OUT} = 4A, V_{OUT_NOM} = 2.5V	V_{BIAS} = 5.0V		97	180	
		I_{OUT} = 4A, V_{OUT_NOM} = 5.0V	V_{BIAS} = 12V		82	150	
Dropout Voltage (MAX38909) (Note 2)	V_{DO}	I_{OUT} = 2A, V_{OUT_NOM} = 1.2V	V_{BIAS} = 5.0V		42.5		mV
			V_{BIAS} = 3.3V		55		
Current Limit (MAX38907/MAX38908)	I_{LIM}	$V_{OUTS/OUT}$ = 0.9 x V_{OUT_NOM}, V_{IN} - V_{OUT} = 300mV		4.4	5.6	6.8	A

Electrical Characteristics (continued)

(V_{IN} = 1.5V, V_{OUT} = 1.0V, V_{BIAS} = 10V, T_J = -40°C to +125°C, C_{IN} = 22µF, C_{OUT} = 22µF)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit (MAX38909)	I_{LIM}	$V_{OUTS/OUT}$ = 0.9 x V_{OUT_NOM}, V_{IN} - V_{OUT} = 300mV			2.8		A
Output Noise		I_{OUT} = 0.5A, 10Hz to 100kHz, V_{OUT} = 1.2V	C_{BYP} = 47nF		25		μV_{RMS}
IN Power Supply Rejection Ratio	PSRR	V_{IN} - V_{OUT} = 0.3V, I_{OUT} = 1A, C_{OUT} = 4 x 10µF, V_{BIAS} > 2.7V, V_{BIAS} = V_{OUT} + 2V, T_A = +25°C	f = 1kHz		60		dB
			f = 10kHz		52		
			f = 100kHz		42		
BIAS Supply Rejection Ratio	PSRR	V_{IN} - V_{OUT} = 0.3V, I_{OUT} = 1A, C_{OUT} = 4 x 10µF, V_{BIAS} = V_{OUT} + 5V, T_A = +25°C	f = 1kHz		90		dB
			f = 10kHz		78		
			f = 100kHz		69		
BYP Capacitor Range	C_{BYP}	Regulator remains stable; guaranteed by design		0.001		0.1	µF
BYP Soft-Start Current	I_{BYP}	From BYP to GND during startup			50		µA
SELA/B/C Input Threshold (MAX38907)	V_{IH}	Rising			1.0		V
	V_{IL}	Falling			0.9		
SELA/B/C Input Leakage Current (MAX38907)	I_{SEL_LK}	V_{SEL} from 0V to 20V, V_{BIAS} = 20V	T_A = +25°C		0.001		µA
			T_J = +125°C		0.01		
Output Margin Adjust Threshold (MAX38907)		V_{MRG} = 1.8V			5		%
		V_{MRG} = 0V			-5		
MRG Input Threshold (MAX38907)	V_{IH}	MRG rising			1.25		V
	V_{IL}	MRG falling			0.5		
MRG Input Threshold Hysteresis (MAX38907)		MRG hysteresis			0.05		V
MRG Input Current (MAX38907)		V_{MRG} from 0V to 5.5V	V_{MRG} = 0V		-1		µA
			V_{MRG} = 5.5V		+1		
EN Input Threshold	V_{IH}	EN rising			1.0	1.6	V
	V_{IL}	EN falling		0.4	0.9		
EN Input Leakage Current	I_{EN_LK}	V_{EN} from 0V to 5.5V, V_{BIAS} from 8V to 20V	T_A = +25°C	-1	+0.001	+1	µA
			T_J = +125°C		0.01		
POK Threshold		V_{OUT} when POK switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		
POK Voltage, Low	V_{OL}	I_{POK} = 1mA			10	100	mV
POK Leakage Current	I_{POK_LK}	V_{POK} = 5.5V	T_A = +25°C	-1	+0.001	+1	µA
			T_J = +125°C		0.01		

Electrical Characteristics (continued)

(V_{IN} = 1.5V, V_{OUT} = 1.0V, V_{BIAS} = 10V, T_J = -40°C to +125°C, C_{IN} = 22µF, C_{OUT} = 22µF)

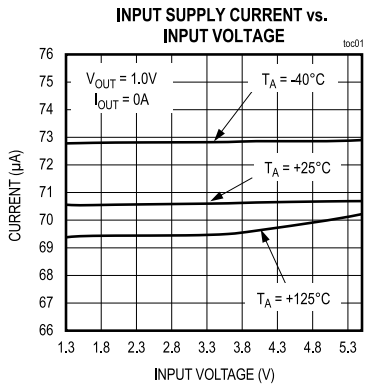
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Reverse-Current Threshold		V_{OUT} = 1.2V, V_{BIAS} = 10V			700		mA
Thermal Shutdown Threshold		TJ when output turns on/off	T_J rising		165		°C
		T_J when output turns on/off	T_J falling		150		

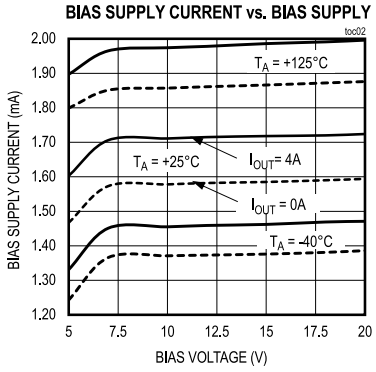
Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

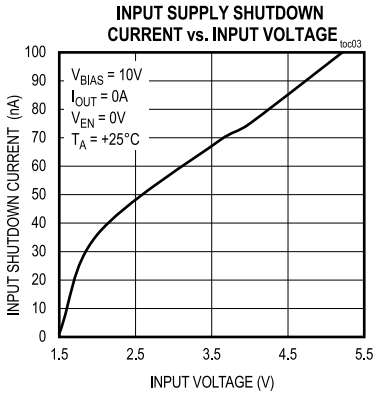
Note 2: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 95% of its nominal value. Dropout limits reflect performance in the 3mm x 3mm TDFN package.

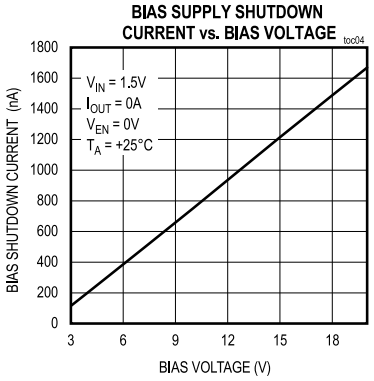
Typical Operating Characteristics

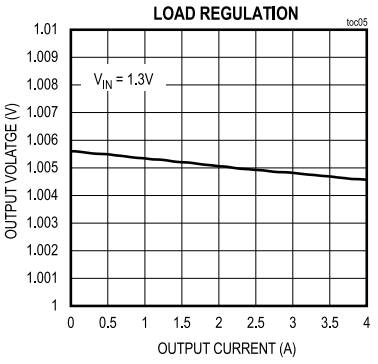
(V_{IN} = 1.5V, V_{BIAS} = 10V, V_{OUT} = 1.0V, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 47nF, T_A = 25ºC, unless otherwise noted)

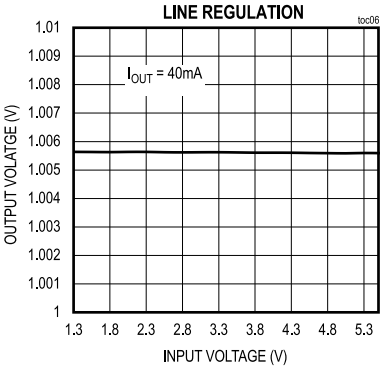


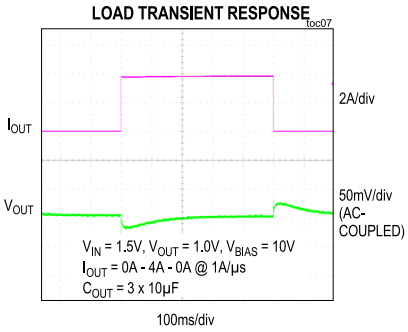


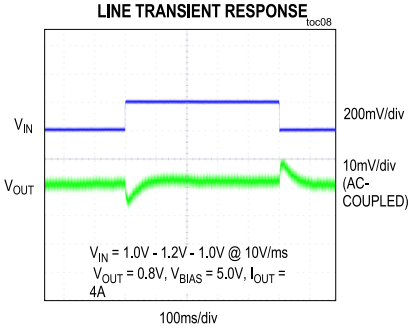


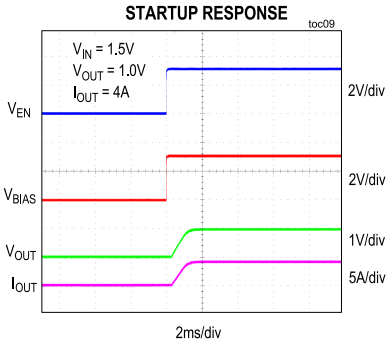






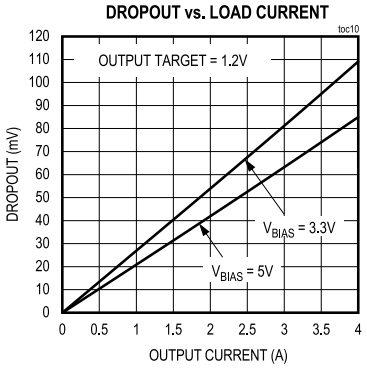


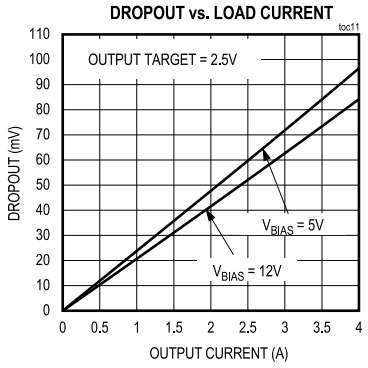


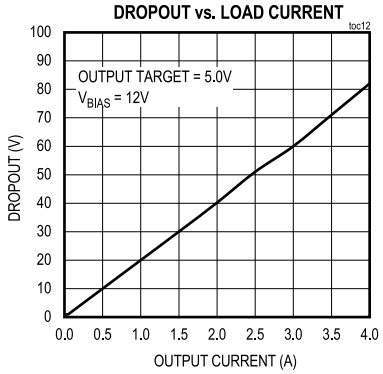


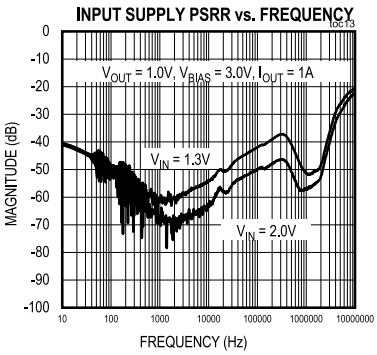
Typical Operating Characteristics (continued)

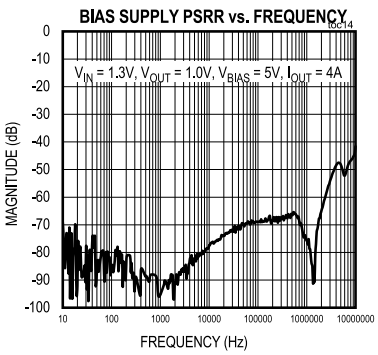
(V_{IN} = 1.5V, V_{BIAS} = 10V, V_{OUT} = 1.0V, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 47nF, T_A = 25ºC, unless otherwise noted)

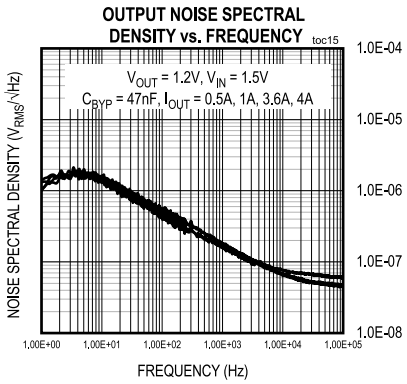


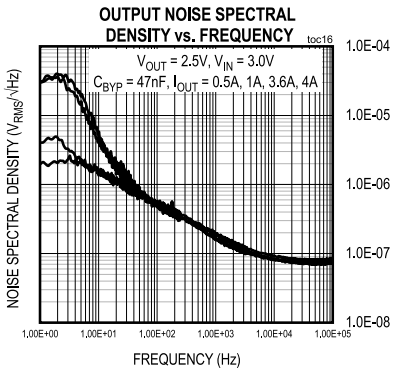


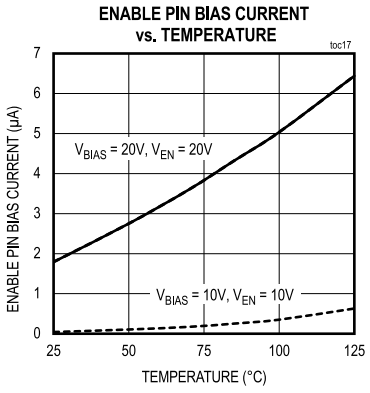






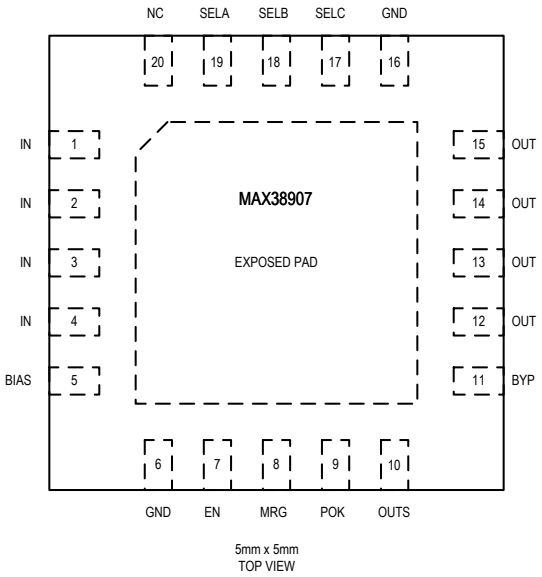




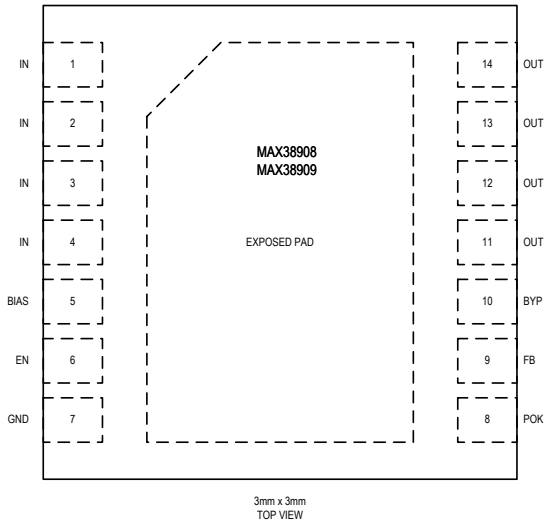


Pin Configurations

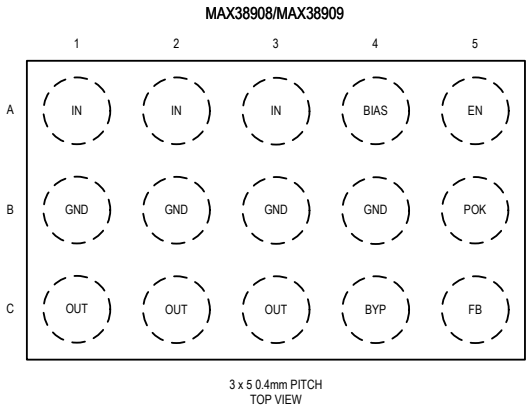
20 TQFN



14 TDFN



WLP



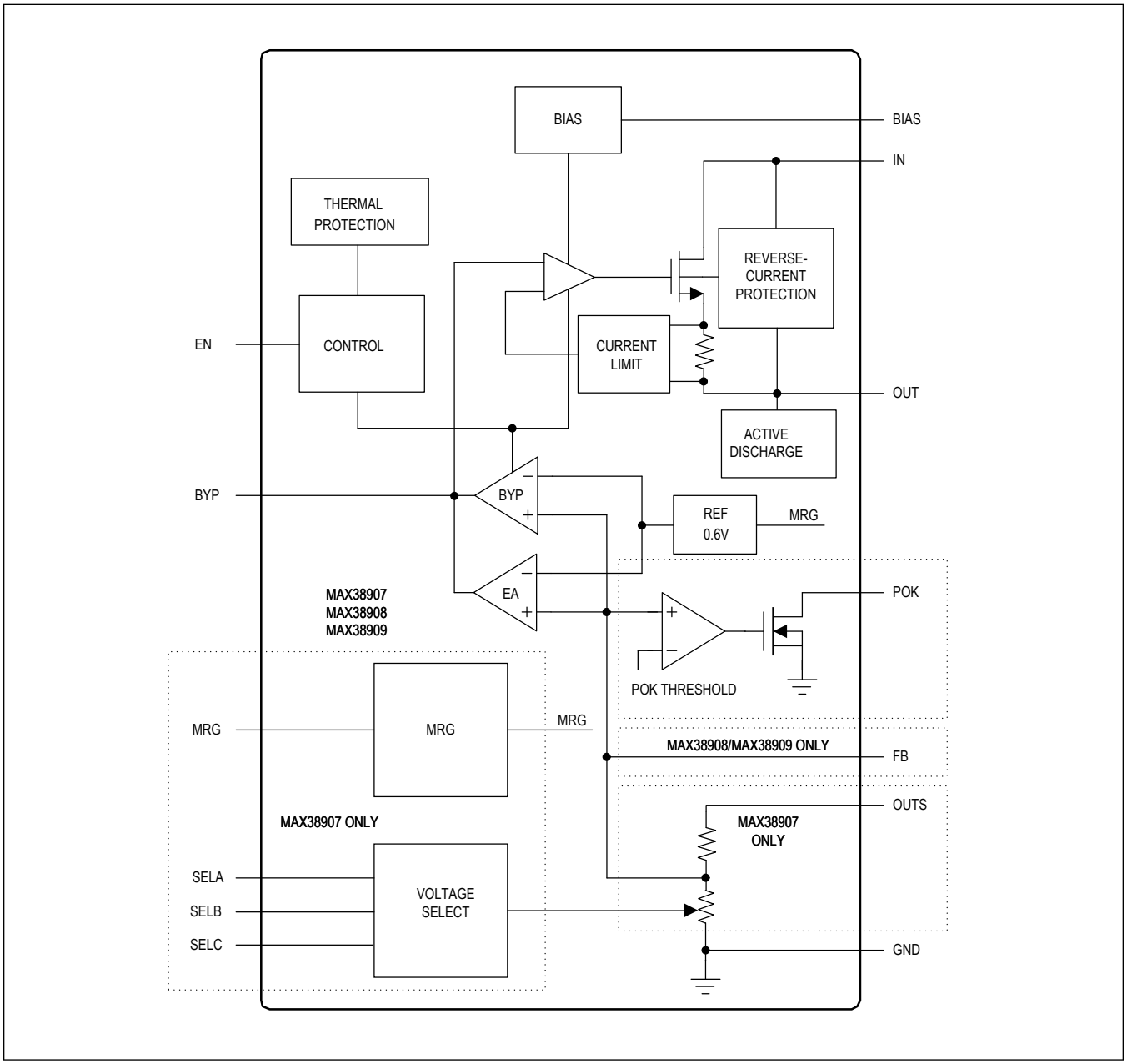
Pin Description

PIN			NAME	FUNCTION
20 TQFN	14 TDFN	WLP		
1, 2, 3, 4	1, 2, 3, 4	A1, A2, A3	IN	Regulator Supply Input. Connect to a voltage between 0.9V and 5.5V and bypass with a 22µF ceramic capacitor from IN to GND.
5	5	A4	BIAS	Bias Supply Input. Connect to a voltage between 2.7V and 20V and bypass with a 1µF capacitor from BIAS to GND. BIAS must be 2.0V or more above the V_{OUT} target.
6, 16	7	B1, B2, B3, B4	GND	Regulator Ground. Bring IN and OUT bypass capacitor GND connections to this pin for best performance.
7	6	A5	EN	Enable Pin. Connect this pin to a logic signal to enable (V_{EN} high) or disable (V_{EN} low) the regulator output. Connect to BIAS to keep the output enabled whenever a valid supply voltage is present.
8	—	—	MRG	±5% Output Voltage Margin Adjustment Input. Float for normal operation. Pull to 0V to cause the output to regulate 5% lower, or pull above 1.4V to cause the output to regulate 5% higher than nominal.
9	8	B5	POK	Power-On Reset Output. Connect a pullup resistor from this pin to a supply to create a reset signal that goes high after the regulator output has reached its regulation target voltage.
10	—	—	OUTS	Output Voltage Sense. Connect to OUT where tight voltage regulation is required.
11	10	C4	BYP	Bypass Capacitor Input. Connect a 0.001µF to 0.1µF capacitor between OUT and BYP to reduce output noise.
12, 13, 14, 15	11, 12, 13, 14	C1, C2, C3	OUT	Regulator Output. Sources up to 4A at the output regulation voltage. Bypass this pin with 22µF ceramic capacitor to GND. It is pulled low with a 70Ω resistance when the regulator is disabled.
17	—	—	SELC	Logic Input 3 Used to Set Output Voltage of the LDO. Connect to GND, BIAS, or float.
18	—	—	SELB	Logic Input 2 Used to Set Output Voltage of the LDO. Connect to GND, BIAS, or float.

Pin Description (continued)

PIN			NAME	FUNCTION
20 TQFN	14 TDFN	WLP		
19	—	—	SELA	Logic Input 1 Used to Set Output Voltage of the LDO. Connect to GND, BIAS, or float.
20	—	—	NC	No Connect Pins
EP	EP	—	EP	Exposed Pad. Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heat sinking.
—	9	C5	FB	Output Voltage Feedback Input. Connect resistor divider across OUT and GND with the center connected to this pin to set any output voltage between 0.6V and 5.0V.

Functional Diagram



Detailed Description

The MAX38907/MAX38908/MAX38909 are fast transient, high PSRR linear regulators that deliver up to 4A of load current. The regulators support a wide input supply (0.9V to 5.5V) and BIAS (2.7V to 20V) voltage ranges, making them suitable for variety of applications. The output voltage regulation accuracy of ±1% is maintained across load, line, and temperature variations, requiring only 300mV of input-to-output headroom at full load for good PSRR. The output voltage can be adjusted to a value in the range of 0.6V to 5.0V to accommodate customers that desire to specify a single LDO in the BOM for multiple voltage rails.

The MAX38907 is configurable to one of 27 output voltages using three digital configuration pins. In addition, each output voltage selection can be adjusted ±5% for margining. The output voltage on MAX38908/MAX38909 can be adjusted to a value in the range of 0.6V to 5.0V by using two external feedback resistors. These LDOs are fully protected from damage by internal circuitry that provides programmable inrush current limiting, output overcurrent limiting, reverse current-limiting, and thermal overload protection.

Enable

The MAX38907/MAX38908/MAX38909 includes an enable pin (EN). The enable signal is an active-high digital signal that enables the device when its voltage passes the rising threshold ($V_{EN} \geq V_{IH}$ (EN) and disables the device when its voltage is below the falling threshold ($V_{EN} \leq V_{IL}$ (EN)). If a separate shutdown signal is not available, connect EN to BIAS. When EN is driven by a host its bias current will vary with the BIAS supply level. See the *Typical Operating Characteristics* for more information.

Bypass

The capacitor connected from BYP to OUT filters noise at the reference, feedback resistors and regulator input stage. It provides a high-speed feedback path for improved transient response. A 10nF capacitor rolls off noise at around 32Hz.

The slew rate of the output voltage during startup is also determined by the BYP capacitor. The MAX38907/MAX38908/MAX38909 feature programmable, monotonic, soft-start set by this capacitor. Its use is highly recommended to minimize inrush current into the output capacitor. A 10nF capacitor sets the slew rate to 5V/ms. This startup rate results in a 110mA slew current drawn from the input at startup to charge 22µF output capacitance.

The BYP capacitor value can be adjusted from 1nF to 100nF to change the startup slew rate according to the following formula:

Startup Slew Rate = 5Vms x 10nF/C_{BYP}

where CBYP is in nF.

This slew rate applies until V_{OUT} reaches 75% of the target after which V_{OUT} slew rate is reduced.

Also, note that being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Power OK

The Power OK (POK) function monitors the voltage at the feedback pin to indicate the output voltage is in regulation. Its operation versus the output voltage is shown in Figure 1.

The POK pin is open-drain and requires a pullup resistor to an external supply in order to properly report the device regulation status to other devices so it can be used for sequencing. Check if the external pullup supply voltage results in a valid logic levels for the receiving device or devices.

The range of the pullup resistance is between 10kΩ and 100kΩ. Its lower limit comes from a pulldown strength of the POK transistor while the higher limit is determined by maximum leakage current at the POK pin.

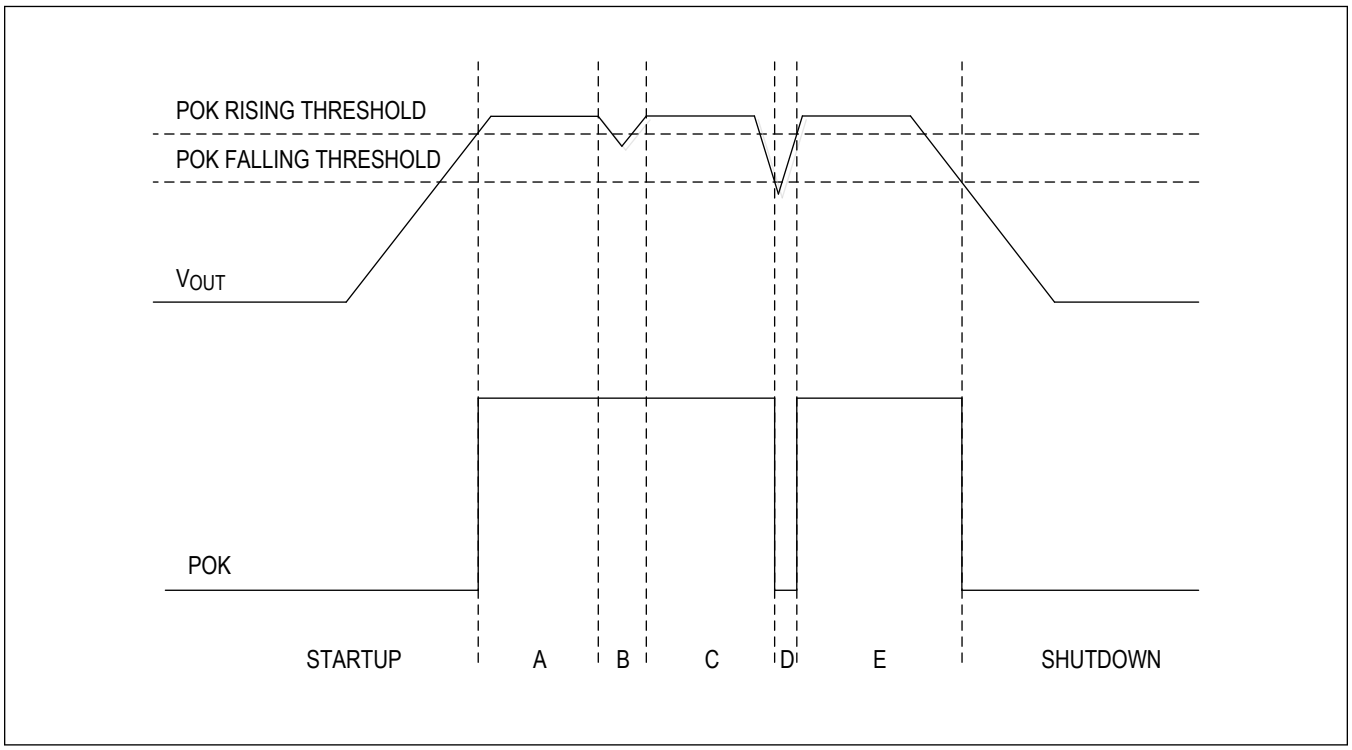


Figure 1. Typical POK Operation

The POK operation versus the output voltage is shown in the Figure 1 above. Different operating regions are:

- A - the device is in regulation.
- B - V_{OUT} sags but does not reach the POK falling threshold.
- C - the device is in regulation.
- D - V_{OUT} sags low enough to cross the POK falling threshold. The POK is driven low until V_{OUT} recovers above the POK rising threshold.
- E - the device is in regulation.

Protection

The MAX38907/MAX38908/MAX38909 is fully protected from an output short-circuit by a current-limiting and thermal overload protection circuit. If the output is shorted to GND, the output current is limited to 5.6A (MAX38907/MAX38908) and 2.8A (MAX38909) (typ). Under these conditions, the device quickly heats up. When the junction temperature reaches 165°C, a thermal limit circuit shuts the output device off. Once the device cools to 150°C, the output turns back on to reestablish regulation. If the fault persists, the output current cycles on and off as the junction temperature slews between 150°C and 165°C. Continuously operating in the fault conditions or above 125°C junction temperature is not recommended since long-term reliability may be reduced. In dropout, the current limit will trigger at 7.4A (typ). Once the limit is triggered, the device will limit the current to 5.6A (typ).

The thermal protection can also be triggered when the device is exposed to excessive heat in the system causing the die temperature to reach undesired levels.

The MAX38907/MAX38908/MAX38909 provides the reverse-current protection when the output voltage is higher than the input. If extra output capacitance is used at the output, a power down transient at the input would normally cause a large reverse-current through a conventional regulator. The MAX38907/MAX38908/MAX38909 include a reverse-voltage detector that trips when IN drops 6.5mV below OUT shutting off the regulator and opening the body diode connection preventing any reverse current. The reverse current is a current that flows through the body diode of the pass element and is undesired due to its impact on power dissipation and long-term reliability especially at higher current levels. The conditions where the reverse current can be flowing back to IN are:

- If the device has a large C_{OUT} and the input supply collapses quickly; OUT has little or no-load current,
- The output is biased when the input supply is not established, or
- The output is biased above the input supply.

The MAX38907/MAX38908/MAX38909 will block reverse currents that exceed about 0.7A by opening a switch in series with the pass device body diode.

Undervoltage Lockout (UVLO)

The MAX38907/MAX38908/MAX38909 Undervoltage Lockout (UVLO) circuits respond quickly to glitches on IN or BIAS and attempts to disable the output of the device if either of these rails collapse. The local input capacitance prevents transient brownouts in most applications.

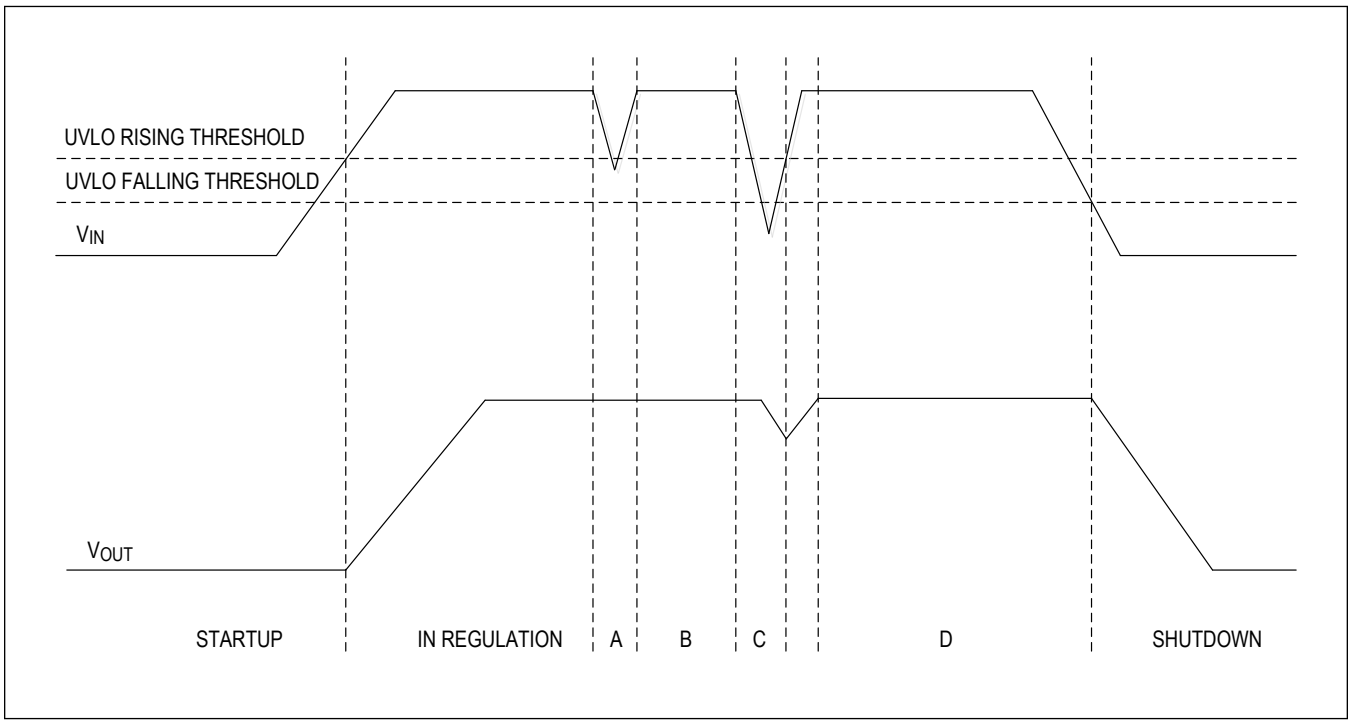


Figure 2. Typical IN UVLO Operation

The Figure 2 above reflects UVLO operation. The different operation regions are:

- A - A brownout condition where V_{IN} can sag below UVLO rising threshold but not below the falling threshold. The device is enabled.
- B - the device is in regulation.
- C - A brownout condition where V_{IN} sags below UVLO falling threshold. The device is disabled and V_{OUT} drops due to load current. It gets enabled again once V_{IN} recovers to the UVLO rising threshold.
- D - the device is in regulation.

During V_{IN} power-up, the MAX38907/MAX38908/MAX38909 will begin V_{OUT} soft start after V_{IN} crosses the V_{IN} UVLO rising threshold. This assures proper V_{OUT} ramp up and transition to regulation. V_{OUT} soft start rate should be kept as or slower than the V_{IN} slew rate to avoid entering the dropout. In some situations, V_{IN} transients can place the regulator into dropout. As V_{IN} starts climbing again and the device comes out of the dropout, the output can overshoot, as shown in Figure 3. This condition is avoided by using an enable signal or by increasing the soft-start time with larger C_{BYP}.

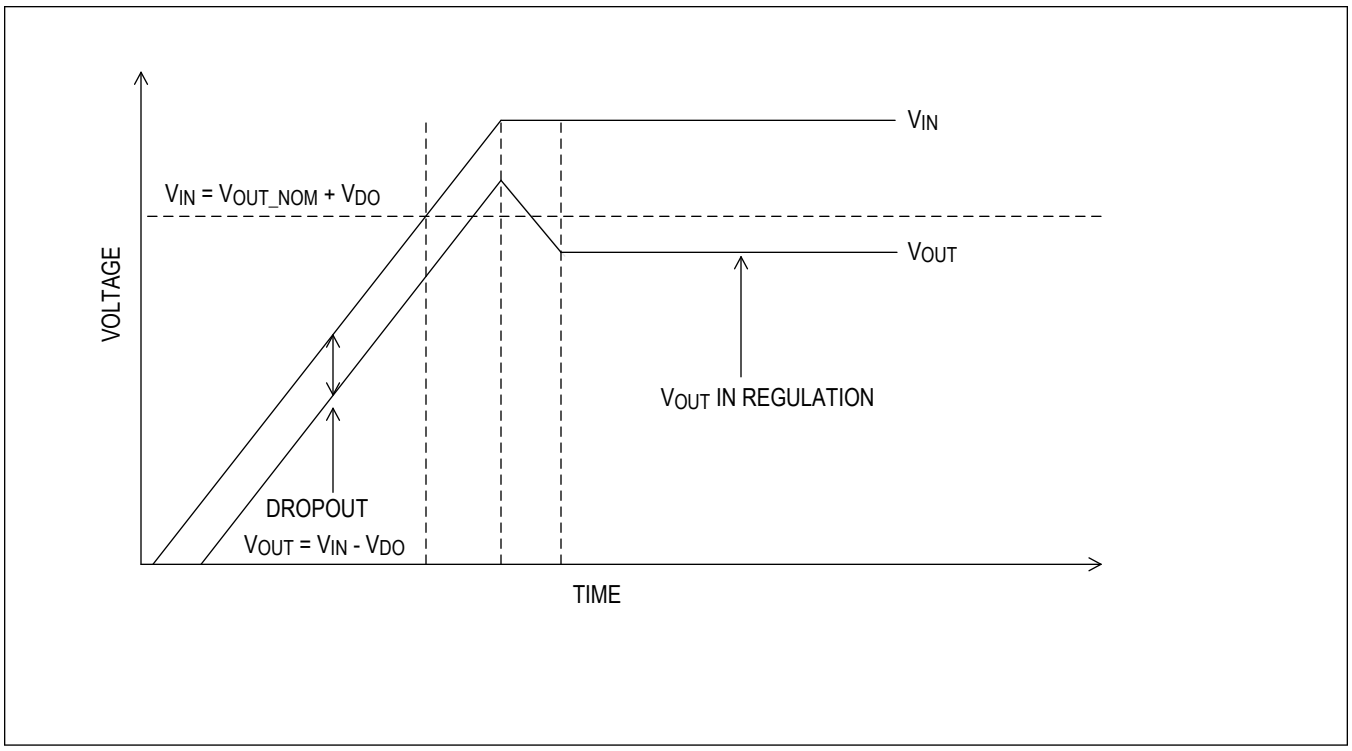


Figure 3. Startup Into Dropout

Active Discharge

When EN is low or BIAS supply is below its falling UVLO threshold, the MAX38907/MAX38908/MAX38909 connects a 70Ω resistor from V_{OUT} to GND in order to discharge the output capacitance.

Output Voltage Selection

Select Version

The MAX38907 includes configuration pins, SELA, SELB, and SELC, that are read during power-up to determine the output regulation voltage. 27 output voltage settings are available. The Table 1 lists the MAX38907 V_{OUT} configuration options.

In addition, the MAX38907 has an additional pin, MRG which allows the output voltage to be margined ±5% with respect to each selection option. The MRG pin is strapped low or high in the system, or it can be driven dynamically by the host. Note the MRG pin cannot be directly strapped to the BIAS supply if the supply is above 5.0V.

Table 1. MAX38907 Output Voltage Configuration

SELA	SELB	SELC	NOMINAL V_{OUT} (V)	V_{OUT} AT MRG LOW (V)	V_{OUT} AT MRG HIGH (V)
Float	Float	Float	0.6	0.57	0.63
GND	Float	Float	0.65	0.6175	0.6825
BIAS	Float	Float	0.7	0.665	0.735
Float	GND	Float	0.75	0.7125	0.7875
GND	GND	Float	0.8	0.76	0.84
BIAS	GND	Float	0.85	0.8075	0.8925
Float	BIAS	Float	0.9	0.855	0.945
GND	BIAS	Float	0.95	0.9025	0.9975
BIAS	BIAS	Float	1.0	0.95	1.05
Float	Float	GND	1.05	0.9975	1.1025
GND	Float	GND	1.1	1.045	1.155
BIAS	Float	GND	1.15	1.0925	1.2075
Float	GND	GND	1.2	1.14	1.26
GND	GND	GND	1.25	1.1875	1.3125
BIAS	GND	GND	1.3	1.235	1.365
Float	BIAS	GND	1.5	1.425	1.575
GND	BIAS	GND	1.8	1.71	1.89
BIAS	BIAS	GND	2.0	1.9	2.1
Float	Float	BIAS	2.2	2.09	2.31
GND	Float	BIAS	2.5	2.375	2.625
BIAS	Float	BIAS	2.7	2.565	2.835
Float	GND	BIAS	3.0	2.85	3.15
GND	GND	BIAS	3.3	3.135	3.465
BIAS	GND	BIAS	3.6	3.42	3.78
Float	BIAS	BIAS	4.0	3.8	4.2
GND	BIAS	BIAS	4.5	4.275	4.725
BIAS	BIAS	BIAS	5.0	4.75	5.25

Feedback Version

The MAX38908/MAX38909 use external feedback resistors to set the output regulation voltage. The output voltage can be set from 0.6V to 5.0V. Set the bottom feedback resistor R1 to less than 100kΩ to minimize FB input bias current error. Calculate the value of the top feedback resistor R2 as follows:

$R2 = R1 \times (V_{OUT}/V_{FB} - 1)$

where V_{FB} is the feedback regulation voltage of 0.6V.

To set the output to 1.0V, for example, R2 should be:

$R2 = 15k\Omega \times (1.0V/0.6V - 1) = 10k\Omega$

R1 of 15 kΩ is recommended to optimize noise performance.

Values of the resistor divider and its tolerance will have a direct impact to V_{OUT} accuracy. 1% resistors or better are recommended. The Table 2 shows recommended values for the feedback resistors.

Table 2. Recommended Feedback Resistor Values

TARGETED OUTPUT VOLTAGE (V)	TOP FEEDBACK RESISTOR VALUES (kΩ)	BOTTOM FEEDBACK RESISTOR VALUES (kΩ)	CALCULATED OUTPUT VOLTAGE (V)
0.8	4.99	15.0	0.799
0.9	7.50	15.0	0.900
1.0	10.0	15.0	1.0
1.2	15.0	15.0	1.2
1.5	22.6	15.0	1.504
1.8	30.1	15.0	1.804
2.5	47.5	15.0	2.5
2.7	52.3	15.0	2.692
3.0	59.0	14.7	3.008
3.3	68.1	15.0	3.324
3.6	75.0	15.0	3.6
4.5	97.6	15.0	4.504
5.0	110.0	15.0	5.0

Applications Information

Input and Output Capacitors

The MAX38907/MAX38908/MAX38909 are designed to have stable operation using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and bypass pin. Multilayer ceramic capacitors (MLCC) with X7R dialectic are commonly used for these types of applications and are recommended due to their relatively stable capacitance across temperature. Nevertheless, amount of equivalent capacitance will depend on operating DC voltage, AC voltage ripple, temperature, etc. Therefore, the capacitor data sheet needs to be properly examined.

The MAX38907/MAX38908/MAX38909 are designed and characterized for operation with X7R ceramic capacitors of 22µF or greater (10µF or greater of effective capacitance) both at the input and output. These capacitors shall be placed as close as possible to the respective input and output pins to minimize trace parasitics.

A combination of multiple output capacitors in parallel will boost the high-frequency PSRR.

Thermal Design

In order to optimize MAX38907/8/9 performance, special consideration is given to the device power dissipation and PCB thermal design. Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. It can be calculated by following equation:

$Loss\ (W) = (V_{IN} – V_{OUT}) \times I_{LOAD}$

The optimal power dissipation can be achieved by carefully choosing input voltage for a given output target rail voltage.

The main thermal conduction path for the device is through the exposed pad of the package. As a result, the thermal pad must be soldered to a copper pad area under the device. Thermal plated vias must be placed inside the thermal PCB pad to transfer heat to different GND layers in the system. The vias should be capped to minimize solder voids. The maximum power dissipation is determined by using thermal resistance from the device junction to ambient keeping the maximum junction temperature below 125°C. Thermal properties of the package are given in the Package Information section.

The first order power dissipation estimate for the 3.3V IN and 2.5V OUT with load current of 500mA condition is:

$Loss\ (W) = (V_{IN} – V_{OUT}) \times I_{LOAD} = (3.3V – 2.5V) \times 0.5A = 0.825W$

Assuming MAX38908ATD+, this power dissipation will raise the junction temperature to:

$T_J = (PD \times \theta_{JA}) + 25°C = (0.825W \times 38°C/W) + 25°C = 56.35°C$

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	FEATURE
MAX38907ATP+*	-40°C to +125°C	20-pin 5mm x 5mm TQFN	4A LDO, Enable Input, Digitally Programmable Output Voltage, Adjustable Margin, Low Noise Bypass
MAX38908ATD+	-40°C to +125°C	14-pin 3mm x 3mm TDFN	4A LDO, Enable Input, Externally Adjustable Output, Low Noise Bypass
MAX38908ANL+*	-40°C to +125°C	5 x 3 bump, 0.4mm Pitch WLP	4A LDO, Enable Input, Externally Adjustable Output, Low Noise Bypass
MAX38909ATD+*	-40°C to +125°C	14-pin 3mm x 3mm TDFN	2A LDO, Enable Input, Externally Adjustable Output, Low Noise Bypass
MAX38909ANL+*	-40°C to +125°C	5 x 3 bump, 0.4mm Pitch WLP	2A LDO, Enable Input, Externally Adjustable Output, Low Noise Bypass

+ Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—