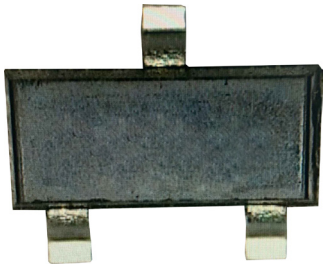
N Channel MOSFET

multicomp PRO

RoHS Compliant



Features

- High density cell design for extremely low RDS(on)
- Rugged and Reliable

Application

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories,Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

Absolute Maximum Ratings (TA = 25°C Unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	
Continuous Drain Current	V_{GS} =10V	I_D	0.36	A
Continuous Drain Current Tamb = 100°C*	V_{GS} =10V		0.23	
Peak Drain Current Tamb = 25°C; single pulse; tp ≤ 10µs		I_{DM}	1.2	
Total Power Dissipation**		P_{tot}	350	mW
Total Power Dissipation*			420	
Total Power Dissipation T_{SP} = 25°C			1140	
Junction temperature		T_J	-55 to +150	°C
Ambient temperature		T_{amb}	-55 to +150	
Storage temperature		T_{stg}	-65 to +150	
Source current		I_S	0.36	A
Electrostatic discharge voltage HBM		V_{ESD}	1500	V

Thermal Resistance

Parameter		Symbol	Typ.	Max.	Unit
Thermal resistance from junction to ambient*	in free air	$R_{th(j-a)}$	310	370	K/W
Thermal resistance from junction to ambient**			-	300	
Thermal resistance from junction to solder point		$R_{th(j-sp)}$	-	115	

Electrical Characteristics at (T_A = 25 °C Unless otherwise specified)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250µA; V_{GS} = 0V; T_J = 25°C	60	-	-	
Gate-Source Threshold Voltage	V_{GSth}	I_D = 250µA; V_{DS} = V_{GS}; T_J = 25°C	0.48	1.1	1.6	V
Drain Leakage Current	I_{DSS}	V_{DS} = 60V; V_{GS} = 0V; T_J = 25°C	-	-	1	µA
		V_{DS} = 60V; V_{GS} = 0V; T_J = 150°C	-	-	10	
Gate Leakage Current	I_{GSS}	V_{GS} = 20V; V_{DS} = 0V; T_J = 25°C	-	-	10	µA
		V_{GS} = -20V; V_{DS} = 0V; T_J = 25°C	-	-	10	
		V_{GS} = 10V; V_{DS} = 0V; T_J = 25°C	-	-	1.0	
		V_{GS} = -10V; V_{DS} = 0V; T_J = 25°C	-	-	1.0	
Drain-Source On-State Resistance	R_{DSon}	V_{GS} = 10V; I_D = 350mA; T_J = 25°C	-	1.1	1.6	Ω
		V_{GS} = 10V; I_D = 350mA; T_J = 150°C	-	2	3.2	
		V_{GS} = 4.5V; I_D = 200mA; T_J = 25°C	-	1.2	2.2	
		V_{GS} = 2.5V; I_D = 10mA; T_J = 25°C	-	1.9	6.5	
Forward Trans conductance	g_{fs}	V_{DS} = 10V; I_D = 200mA; T_J = 25°C	-	700	-	mS
Dynamic Characteristics						
Total Gate Charge	$Q_{G(tot)}$	V_{DS} = 30V; I_D = 300mA; V_{GS} = 4.5V; T_J = 25°C	-	0.6	0.7	nC
Gate-Source Charge	Q_{GS}		-	0.1	-	
Gate-Drain Charge	Q_{GD}		-	0.2	-	
Input Capacitance	C_{iss}	V_{DS} = 10V; f = 1MHz; V_{GS} = 0V; T_J = 25°C	-	42	56	pF
Output Capacitance	C_{oss}		-	7	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 40V; R_L = 250Ω; V_{GS} = 10V; $R_{G(ext)}$ = 6Ω; T_J = 25°C	-	5	10	ns
Rise Time	t_r		-	5	-	
Turn-off Delay Time	$t_{d(off)}$		-	38	76	
Fall time	t_f		-	20	-	
Source-Drain Diode						
Source-Drain Voltage	V_{SD}	I_S = 300mA; V_{GS} =0V; T_J = 25°C	0.47	0.8	1.2	V

Note:

*Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

**Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1cm^2.

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

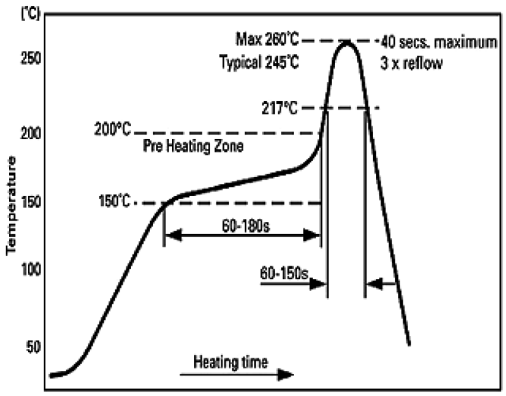
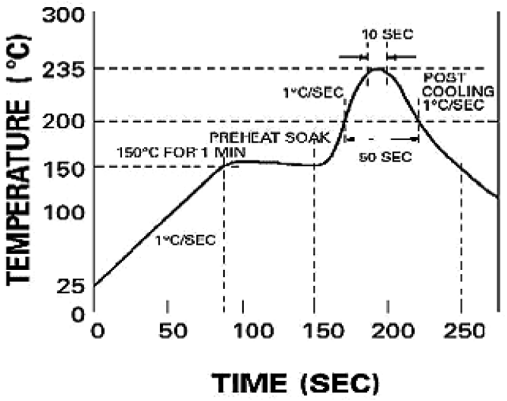


Figure 2

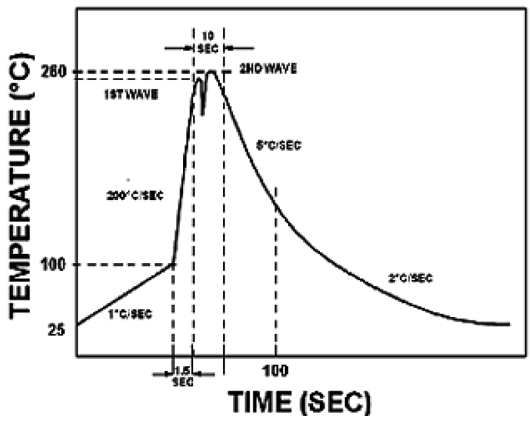


Reflow Profiles in Tabular Form

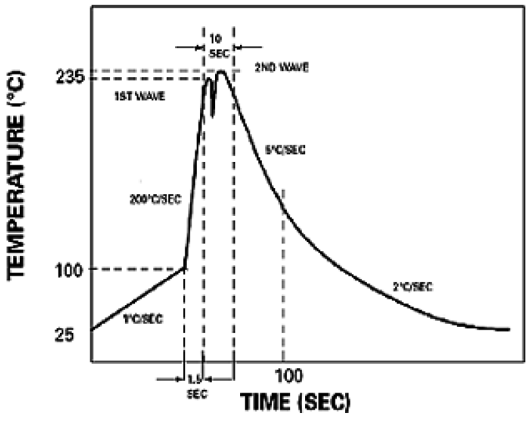
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat Temperature Range Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: Temperature Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder

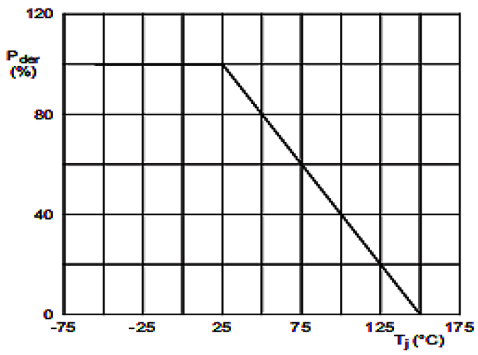


Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp.	Within 125°C of Solder Temp.
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

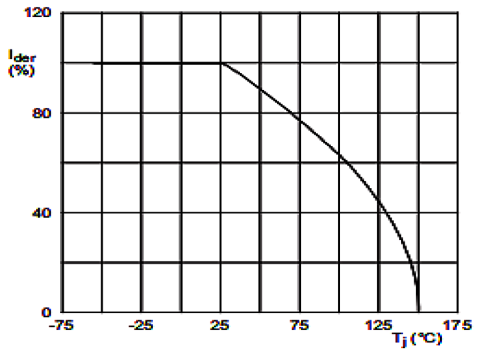
Typical Characteristics Curves

Fig 1: Normalized total power dissipation as a function of junction temperature



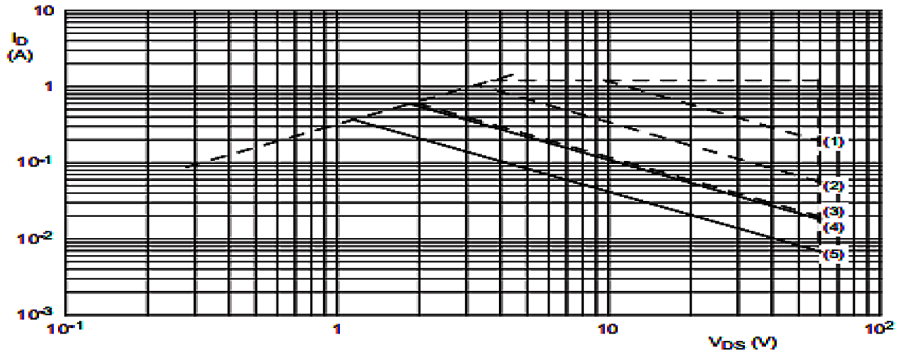
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2: Normalized continuous drain current as a function of junction temperature



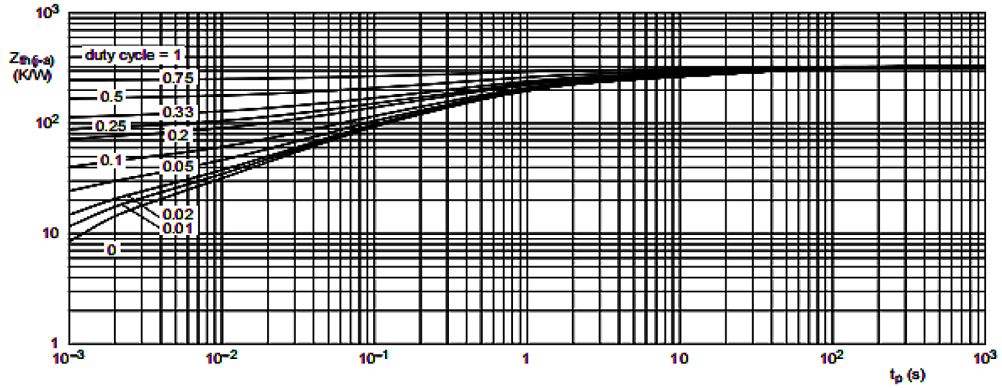
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 3: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



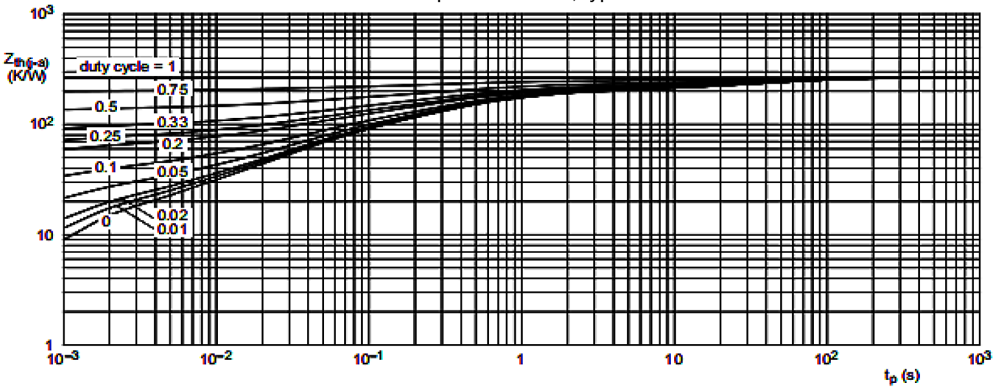
I_{DM} is a single pulse
(1) t_p = 1 ms
(2) t_p = 10 ms
(3) t_p = 100 ms
(4) DC; T_{sp} = 25 °C
(5) DC; T_{amb} = 25 °C; 1 cm^2 drain mounting pad

Fig 4: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



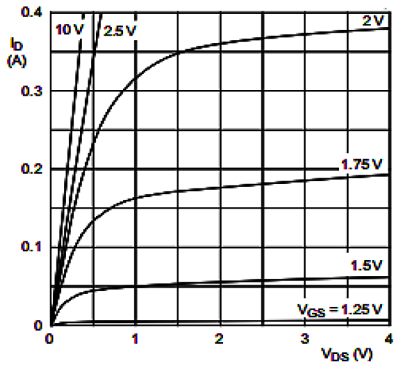
FR4 PCB, standard footprint

Fig 5: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



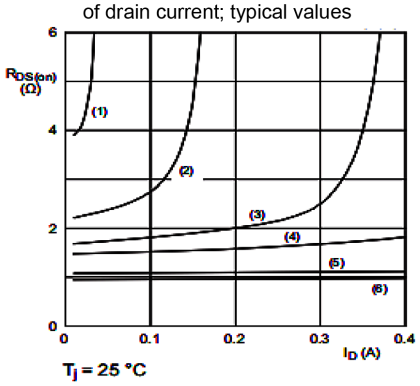
FR4 PCB, mounting pad for drain 1 cm^2

Fig 6: Output characteristics: drain current as a function of drain-source voltage; typical values



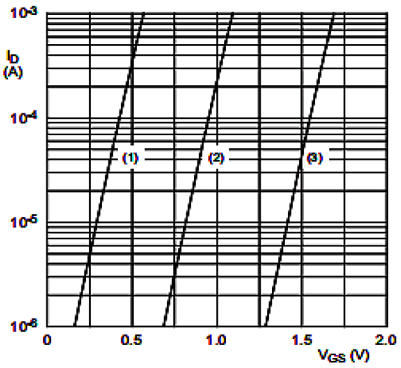
T_j = 25 °C

Fig 7: Drain-source on-state resistance as a function of drain current; typical values



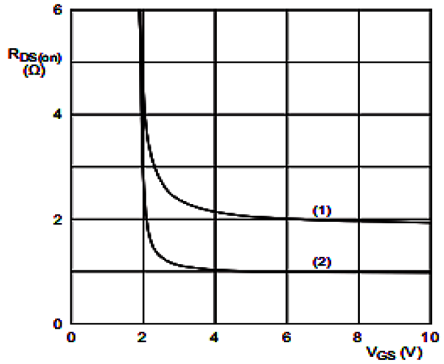
T_j = 25 °C
(1) V_{GS} = 1.5 V
(2) V_{GS} = 1.75 V
(3) V_{GS} = 2.0 V
(4) V_{GS} = 2.25 V
(5) V_{GS} = 4.5 V
(6) V_{GS} = 10 V

Fig 8: Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C; V_{DS} = 5 V
(1) minimum values
(2) typical values
(3) maximum values

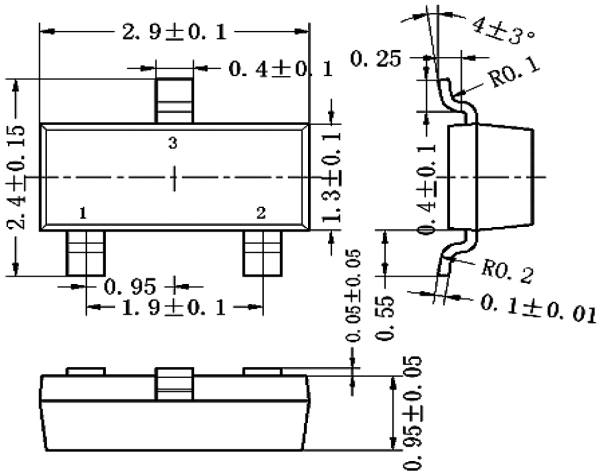
Fig 9: Drain-source on-state resistance as a function of gate-source voltage; typical values



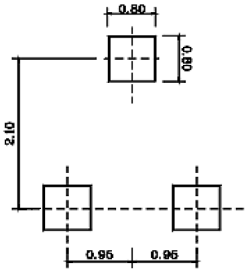
I_D = 300 mA
(1) T_j = 150 °C
(2) T_j = 25 °C

Diagram

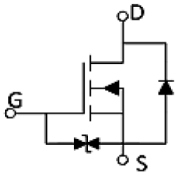
SOT-23 SMD Package



Suggested Pad Layout



Pin configuration



1. Gate
2. Source
3. Drain

Part Number Table

Description	Part Number
N Channel Plastic Encapsulate MOSFET, SOT 23	BSS138BK

Dimensions : Millimetres