ANALOG DEVICES

AD9166-FMC-EBZ User Guide
UG-1698

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Evaluation Board for the AD9166 DC to 9 GHz Vector Signal Generator

FEATURES

Simple evaluation of the AD9166 vector signal generator IC with only a single connection needed
Integrated on-board clocking, featuring the ADF4372
Integrated on-board power and power sequencer

EVALUATION KIT CONTENTS

AD9166-FMC-EBZ
Mini USB cable

RECOMMENDED EQUIPMENT LIST

ADS7-V2EBZ pattern generator and data capture board
Spectrum analyzer
Optional dual sinusoidal clock source (capable of sourcing 6 GHz, with <0.5 ps rms jitter)

GENERAL DESCRIPTION

This user guide is for the AD9166-FMC-EBZ evaluation board. The evaluation board connects to an ADS7-V2EBZ pattern generator for quick evaluation of the AD9166, a high speed, vector signal generator. The ADS7-V2EBZ automatically formats the signal data and sends it to the evaluation board across a JESD204B link, which simplifies evaluation of the device. The evaluation board is powered by the field-programmable gate array (FPGA) mezzanine card (FMC) power supply provided through the ADS7-V2EBZ.

Figure 1 shows the top side of the evaluation board. The evaluation board includes a clock buffer, the HMC7044, which provides a reference clock to the ADS7-V2EBZ and SYSREF± signals to both the ADS7-V2EBZ and the digital-to-analog converter (DAC) integrated inside the AD9166. The on-board ADF4372 generates a sampling clock for the DAC.

The reference and sampling clocks can be connected externally through the on-board Subminiature Version A (SMA) ports. SYSREF± can be connected from an external source, such as an FPGA development kit, across the FMC connector to the AD9166.

The various clock configurations are outlined in Figure 3. The clock paths can be selected by soldering 0 Ω resistors (jumpers) in the correct locations on the evaluation board and configuring the ADF4372 and HMC7044 as described in the On-Board Clocking section.

Complete specifications for the AD9166 can be found in the AD9166 data sheet available from Analog Devices, Inc., and must be consulted in conjunction with this user guide when using the evaluation board.

AD9166-FMC-EBZ EVALUATION BOARD PHOTOGRAPH

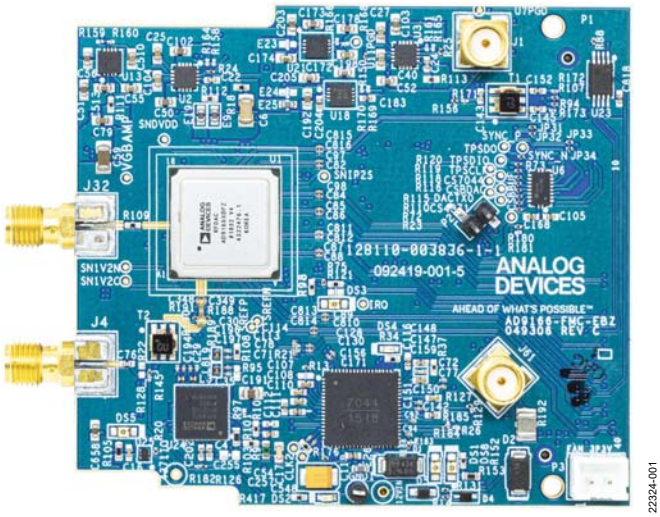

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

7/2020—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD9166-FMC-EBZ evaluation board integrates all necessary power supply rails, power supply sequencing, and on-board clock sources. The evaluation board can be powered by a single 12 V supply. The auxiliary cooling fan is powered from a 3.3 V rail. Both supplies are provided by the ADS7-V2EBZ.

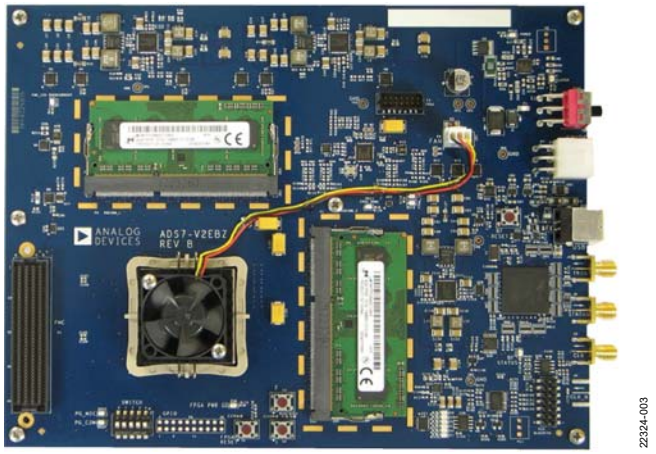

Figure 2. View of the Top of the ADS7-V2EBZ Pattern Generator Board

The evaluation board includes provisions to allow using either the on-board (internal) clocking or providing reference clocks from an external source. The user can choose. Generally, laboratory grade, high frequency clock sources can achieve best-in-class phase noise performance, which directly translates to the output of the AD9166. However the on-board clocking scheme, based on the HMC7044 and ADF4372 ICs, results in phase noise performance that is comparable or exceeds the performance of many laboratory grade clock sources, as shown in Figure 16.

A block diagram of the clock paths on the AD9166-FMC-EBZ evaluation board is shown in Figure 3.

ON-BOARD CLOCKING

Multiple on-board clock configurations are possible, based on the HMC7044 and ADF4372. For details on clocking configurations that require external clocking, refer to the External Clocking section.

The HMC7044 includes two phase-locked loops (PLLs): PLL1 and PLL2. Each loop can operate independently.

Aside from specific configurations where only PLL1 is used, the HMC7044 is only needed when an active JESD204B link provides the data samples to the AD9166 through the FMC connector. In this case, the HMC7044 generates a lane rate/40 (or bit rate/40) clock and a SYSREF± clock to the FPGA on board the ADS7-V2EBZ, and another SYSREF± clock to the AD9166, to support a JESD204B link in either Subclass 0 or Subclass 1. More details are available in the Hardware Setup section in this user guide, in the JESD204B specifications from JEDEC, and in the AD9166 data sheet.

PLL1 is a low bandwidth PLL that allows improving the phase noise (jitter) of an external reference, which typically results in improved phase noise in the 1/f region of downstream PLLs, a region that is within the pass band of most PLLs, at offset frequencies of 1 kHz and below. As a trade-off, the low loop bandwidth of PLL1 results in a longer lock time if the input reference frequency is considerably lower than the oscillator frequency to which the PLL attempts to lock. On the AD9166-FMC-EBZ evaluation board, PLL1 is used to lock an on-board 122.88 MHz voltage controlled crystal oscillator (VCXO) to an external reference connected to J61.

The VCXO operates at 122.88 MHz and can be either locked using PLL1 or left free running by keeping J61 disconnected. It is generally a good practice to reconfigure the HMC7044 via its serial peripheral interface (SPI) bus so that its charge pump is tristated. However, it may not always be necessary because when PLL1 loses its reference, it automatically enters holdover and maintains the VCXO control voltage at the last known level. This means that the input to J61 can be removed while the AD9166 is running, which may result in small variations in close in phase noise at the AD9166 output, depending on how the HMC7044 was configured. It may be good practice to reprogram the HMC7044 if the reference on J61 is removed.

PLL2 can lock a high frequency, internal voltage controlled oscillator (VCO) core inside the HMC7044 to the 122.88 MHz VCXO output. The VCO output is then fed the output fanout buffer inside the HMC7044 to generate the various clock rates. See the HMC7044 data sheet for more details.

Instead of PLL2, the user can choose to input a reference clock to FIN, the external VCO input on the CLKIN1/FIN pin of the HMC7044, and bypass PLL2 altogether. Using the CLKIN1/FIN pin is the default clocking scheme on the AD9166-FMC-EBZ evaluation board, as configured by solder jumpers or 0 Ω resistors. The input to the CLKIN1/FIN pin is derived from the ADF4372.

The ADF4372 provides a sample rate clock to the DAC core of the AD9166. The ADF4372 can also provide a copy of this clock to the CLKIN1/FIN pin of the HMC7044. Both clocks can be phase synchronized.

The fractional-N PLL inside the ADF4372 locks an internal VCO to the VCXO on the AD9166-FMC-EBZ evaluation board. This is the same VCXO that locks PLL2, when used. Locking both PLL2 and the ADF4372 to a common reference allows both to be frequency locked, whether in fractional-N or integer mode.

By default, the ADF4372 on the AD9166-FMC-EBZ evaluation board provides both the AD9166 sample rate clock (DAC clock) and the reference clock to the HMC7044 through the CLKIN1/FIN pin. PLL2 is not used, and PLL1 can be still used to lock the VCXO to an external reference from J61.

EXTERNAL CLOCKING

Nearly all the clocks that can be generated on the AD9166-FMC-EBZ evaluation board can be provided from external sources as well, using the J1, J4, and J61 SMA ports. One exception is the SYSREF± clock, which can be provided externally directly to the AD9166, through the FMC connector.

The J1 SMA port allows connecting a bit rate/40 clock to the FMC connector and downstream FPGA. The J4 SMA port allows connecting an external DAC clock. The J61 SMA port allows connecting an external reference to PLL1 of the HMC7044 to lock the on-board VCXO.

Various clocking schemes exist, using either on-board clocking or external clock sources, or both.

COMMON CLOCKING SCHEMES

The following four basic clocking schemes cover typical applications encountered by end users:

- All internal clocking with the option to lock the clock tree to an external reference connected to J61.
- All external clocking with an external DAC clock connected to J4 and an external bit rate/40 clock connected to J1. SYSREF± can be provided across the FMC connector from an FPGA development kit. The ADS7-V2EBZ cannot be configured to generate an external SYSREF± signal to the FMC connector.
- External DAC clock connected to J4 with a low frequency external reference connected to J61. The reference is then routed to PLL1 to lock the VCXO, and the VCXO is used as a reference to PLL2 of the HMC7044 to generate the bit rate/40 clock and both SYSREF± clocks to the AD9166 and ADS7-V2EBZ.
- External DAC clock connected to J4, from which a high frequency external reference is derived and connected to J61. The reference is then routed to the FIN path of the HMC7044 to generate the bit rate/40 clock and both SYSREF± clocks to the AD9166 and ADS7-V2EBZ. Typically, the input to J4 and J61 is optimally derived from a single clock source across a splitter.

Other less common schemes can be supported, and the end user is encouraged to customize the evaluation board as needed for evaluation.

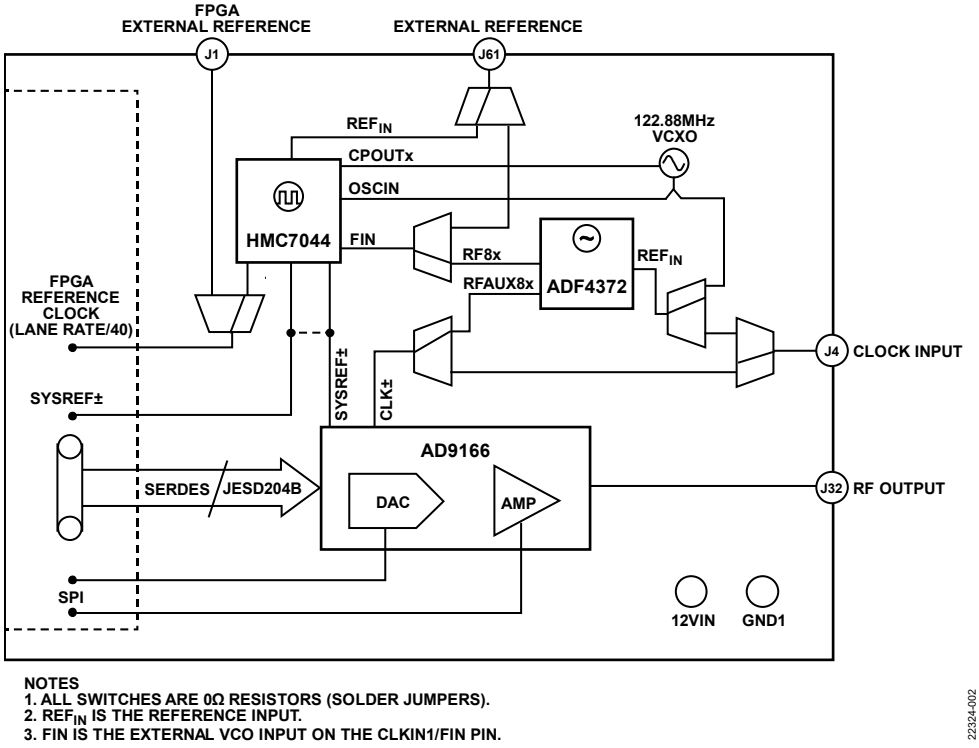

Figure 3. Block Diagram of the AD9166-FMC-EBZ Evaluation Board

EVALUATION BOARD SOFTWARE

The AD9166-FMC-EBZ evaluation board is configured using an easy to use graphical user interface called analysis, control, evaluation (ACE). ACE is available for download at www.analog.com/ACE.

The user can also install the AD9166 ACE serial peripheral interface (SPI) programmer application. The ACE SPI programmer application enables full access to the register map of the AD9166 and has additional functionality, such as the ability to record, load, and save macros or register sequences, to ease programming of the device.

Use the **DPGDownloader** program for loading signal vectors into the ADS7-V2EBZ, to be played by the AD9166 across a JESD204B link.

The ADF4372 and HMC7044 are also configured by ACE. Several macros or register sequences are included in this user guide to demonstrate how to set up these devices, based on the desired clock configuration. For some clock configurations, ACE reprograms the ADF4372 and HMC7044 without any physical changes to the AD9166-FMC-EBZ evaluation board.

HARDWARE SETUP

CONFIGURATION 1: EXTERNAL CLOCK

To use the external signal generator as the clock source, follow these steps:

1. Connect a low phase noise, high frequency clock source to the J4 connector.
2. Set the output level to 0 dBm. Higher clock power results in improved phase noise. Refer to the AD9166 data sheet.
3. Connect a second low phase noise, high frequency clock source (10 MHz to 250 MHz) with a 0 dBm output level as the reference clock to the HMC7044 to the J61 SMA connector.
4. To supply the bit rate/40 clock from an external source, connect the high frequency clock source to J1, and ensure the resistor jumpers are properly configured (R172, R107, R94, and R173).
5. Ensure the two clock sources are frequency locked to a common reference. A unit (such as the Rohde & Schwarz SMA100B) provides an option for a secondary signal source, where both outputs are derived from a common reference. Alternatively, the 10 MHz reference output of the signal generator can be directly connected to the reference input at J61.
6. Connect the spectrum analyzer to the J32 SMA connector.
7. Connect the AD9166-FMC-EBZ evaluation board to the FMC connector of the ADS7-V2EBZ. Ensure the FMC pins are properly aligned before connecting the evaluation board.
8. Connect the power switch on the ADS7-V2EBZ to apply power to both boards.

CONFIGURATION 2: ON-BOARD CLOCK

To use the on-board ADF4372 and HMC7044 ICs as the clock sources, follow these steps:

1. Connect the spectrum analyzer to the J32 SMA connector.
2. Connect the AD9166-FMC-EBZ evaluation board to the FMC connector of the ADS7-V2EBZ. Ensure the pins are properly aligned before connecting the board.
3. Connect the ac adapter to the ADS7-V2EBZ.
4. Press the power switch on the ADS7-V2EBZ to apply power to both boards.

CONFIGURATION 3: NCO ONLY

The AD9166 can operate in NCO only mode, which does not require a JESD204B link to supply data samples from an FPGA. The AD9166 operates as a direct digital synthesizer (DDS). However, the SPI bus to control the AD9166-FMC-EBZ is routed through the FMC connector, and either an ADS7-V2EBZ or an FPGA development kit must be connected to the evaluation board to send SPI commands.

As a workaround, short wires can be soldered to test points located near U6 (a SPI bus level shifter) and connected to a microcontroller or another device capable of sending SPI commands. In this case, do not connect the evaluation board to the FMC connector to avoid sending unintentional SPI commands to the ADS7-V2EBZ. The evaluation board can be powered from an external 12 V supply connected across 12VIN and GND1 test points.

To demonstrate the AD9166 can operate as a DDS, configure the evaluation board while it is connected to a data pattern generator such as the ADS7-V2EBZ. After the evaluation board is configured, apply an additional 12 V supply across the two test points, 12VIN and GND1, and then power down the ADS7-V2EBZ. At this point, the evaluation board can be carefully disconnected from the FMC connector while the board is still powered on. This approach demonstrates that the AD9166 can operate as a DDS without an active JESD204B link or a connection to an FPGA development kit.

Follow these steps:

1. Connect the spectrum analyzer to the J32 SMA connector.
2. If using an external clock source, connect a low phase noise, high frequency clock source to J4.
3. Connect the AD9166-FMC-EBZ evaluation board to the FMC connector of the ADS7-V2EBZ. Ensure the FMC pins are properly aligned before connecting the board.
4. Press the power switch on the ADS7-V2EBZ to apply power to both boards
5. Configure the evaluation board using the ACE software.
6. With power from the ADS7-V2EBZ applied and the evaluation board configured in NCO only mode, carefully connect an additional 12 V dc supply across 12VIN (red) and GND1. The external power supply must have capacity for 1.25 A of current.
7. Turn on power for the external 12 V supply. The current draw from the ADS7-V2EBZ drops, and the current draw from the external power supply increases.
8. Disconnect the evaluation board from the ADS7-V2EBZ.

Before reconnecting the evaluation board to the ADS7-V2EBZ, first power down both the 12 V supply and the ADS7-V2EBZ.

Consider using an FMC adapter to avoid wearing out the FMC connector.

GETTING STARTED

Software installation includes an updated version of the **DPGDownloader** software and the necessary files for the AD9166-FMC-EBZ evaluation board, including the schematic, board layout, and data sheet. Download the **DPGDownloader** software online from the DAC Software Suite, at wiki.analog.com/resources/eval/dpg/dacsoftwaresuite.

Also install the ACE software to configure the device. ACE is the software that is used to load the registers in the AD9166. The ACE software enables full access to the AD9166 register map and has several views and features that simplify its use. Many of the ACE software features are detailed in the ACE User Guide section.

Download this software online from the ACE software page. The ACE software package includes the required plugins for the AD9166-FMC-EBZ evaluation board.

INITIAL SETUP

Complete the following initial steps to get started with the evaluation of the device:

1. Install the **DPGDownloader** software on the PC. Analog Devices, Inc., recommends verifying the basic setup before making any modifications to the evaluation board.
2. Connect the PC to the ADS7-V2EBZ using the USB connector.
3. Connect the evaluation board to the ADS7-V2EBZ using the FMC connector.
4. Switch the power connector on the ADS7-V2EBZ to power up both the evaluation board and the ADS7-V2EBZ.

Several different configurations and scenarios are explained in this user guide with step by step instructions. Choose the configuration that meets the requirements. A summary of the ACE user guide is provided in the ACE User Guide section.

DC TEST/NCO MODE

CONFIGURE THE SPECTRUM ANALYZER

Configure the spectrum analyzer as follows:

- Start frequency = 50 MHz.
- Stop frequency = 5 GHz.
- Resolution bandwidth = 300 kHz. Use the average rms detector setting.
- Choose an input attenuation of 6 dB. This value can be adjusted later if there are indications that the analyzer is causing degradations (warnings on the analyzer itself, or third-order products appearing on the output spectrum).

CONFIGURE THE EVALUATION BOARD

Complete the following steps to configure the evaluation board to output a single tone at 1 GHz:

1. Ensure that the AD9166-FMC-EBZ evaluation board is configured and powered up according to the Hardware Setup section.
2. Open the ACE software from **Start** > **Programs** > **Analog Devices** > **ACE**. A window appears similar to Figure 5.
3. Open the evaluation board view by double clicking the AD9166-FMC-EBZ evaluation board icon, as shown in Figure 5.
4. In the **AD9166 STARTUP WIZARD**, under **Board Clocking Schemes**, select **All internal clocking** from the **Board Clock Scheme** dropdown box, as shown in Figure 4.

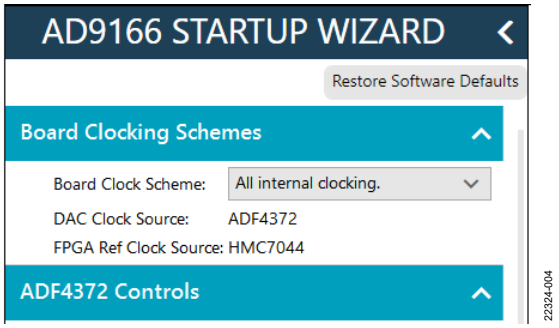

*Figure 4. Select **All internal clocking** as the Board Clock Scheme*

5. Using the **AD9166 STARTUP WIZARD** on the left side of the window, replace the default values shown in Figure 6 with the following:
   a. For **Operation Mode**, select **DC Test Mode**.
   b. Set **FDAC** to 4.9152 GHz.
   c. Select the **NCO Enable** box.
   d. Set the **Frequency Shift** to 1 GHz.
   e. Set **DC Back-Off(dB)** to −0.1 dB.
   f. Click the **Apply** button.

   A 1 GHz single tone appears on the spectrum analyzer, as shown in Figure 8.

After clicking **Apply**, the **Apply** button changes to **Change**. To change the parameters in Step 5, click the **Change** button and enter new values. The **Change** button reverts to **Apply** when new values are entered. Click **Apply** again after making all necessary changes.

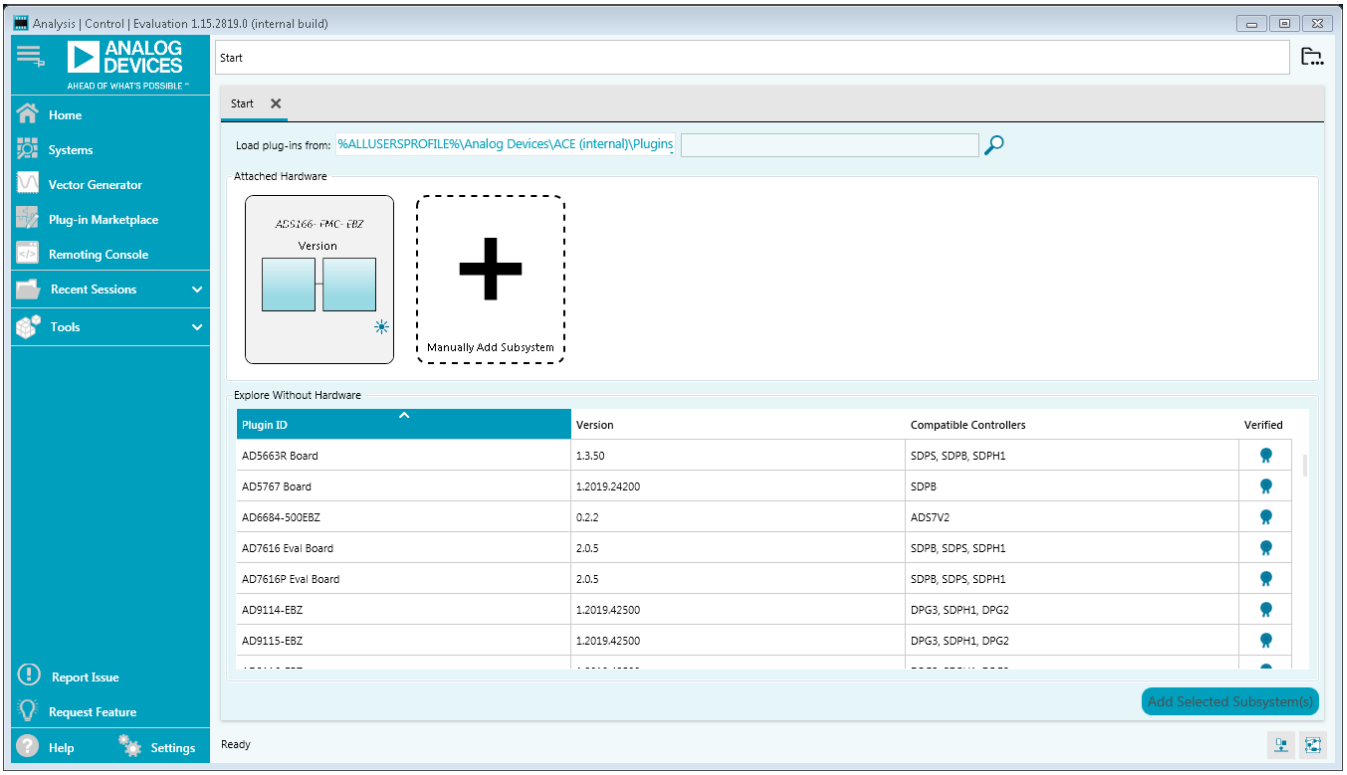

Figure 5. ACE Software Window

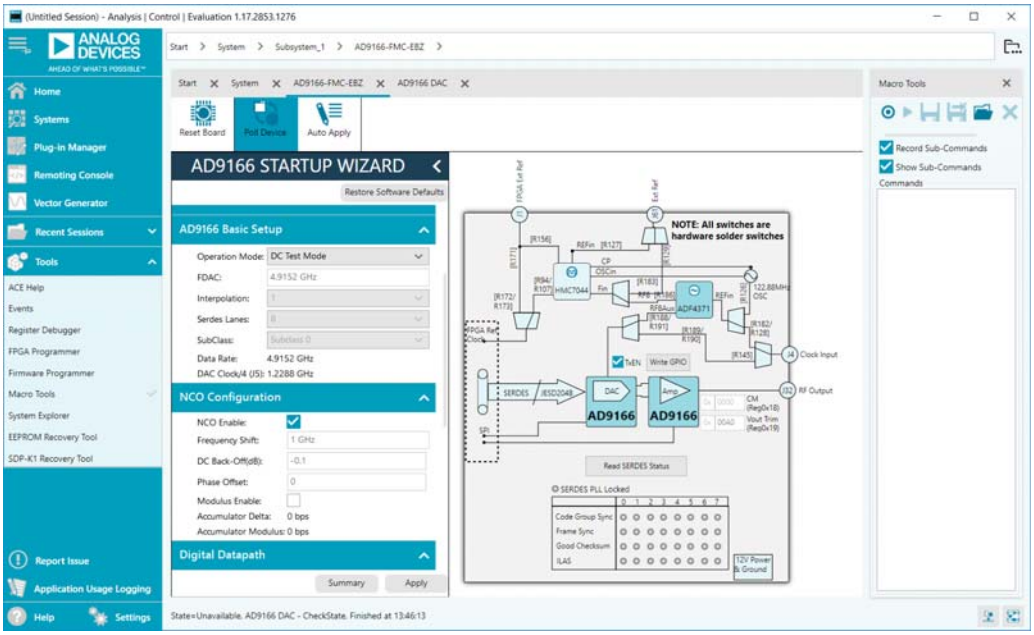

Figure 6. ACE—Initial Configuration

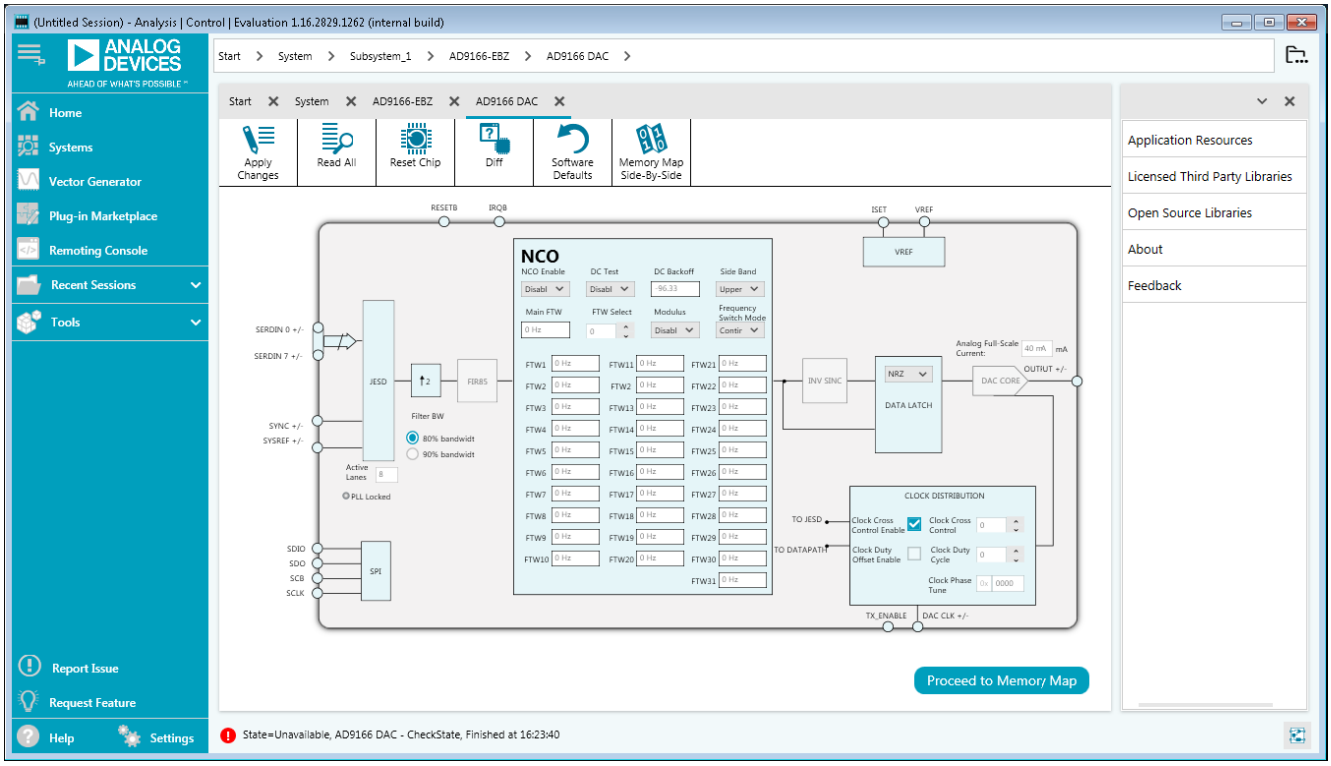

Figure 7. AD9166 Chip View and Clock Source Selection in ACE

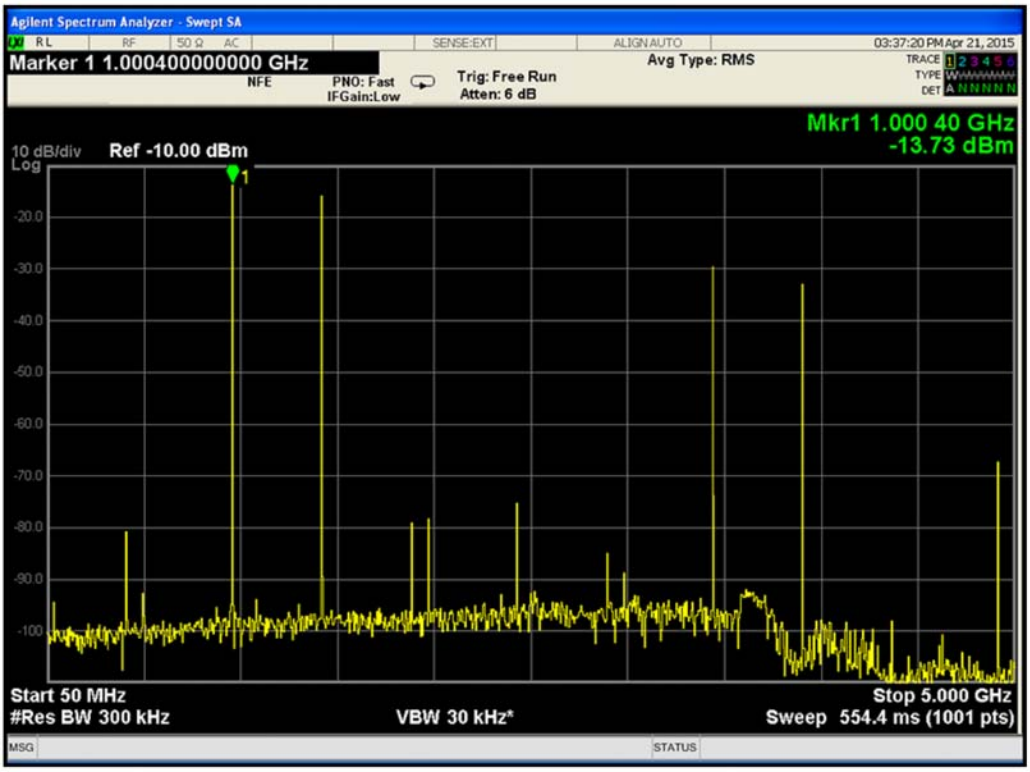

Figure 8. Spectrum Analyzer Plot of DAC Output in NCO Mode (Showing a Single Tone at 1 GHz)

USING THE ADS7-V2EBZ TO PLAY A PATTERN TO THE EVALUATION BOARD

CONFIGURE THE SPECTRUM ANALYZER

Configure the spectrum analyzer as follows:

- Start frequency = 50 MHz.
- Stop frequency = 5 GHz.
- Resolution bandwidth = 300 kHz.
- Use the average rms detector setting.
- Choose an input attenuation of 6 dB. This value can be adjusted later if there are indications that the analyzer is causing degradations (warnings on the analyzer itself, or third-order products appearing on the output spectrum).

LOAD AND PLAY PATTERN TO THE ADS7-V2EBZ

Configure the hardware according to the instructions provided in the Hardware Setup section.

Complete the following steps to configure the ADS7-V2EBZ board and load a single tone at 800 MHz to the on-board FPGA:

1. To load and play the pattern to the ADS7-V2EBZ, open **DPGDownloader** from **Start** > **Programs** > **Analog Devices** > **DPG** > **DPGDownloader**.
2. Ensure that the program detects the AD9166 and reflects the device name in the **Evaluation Board** dropdown list. For this evaluation board, **JESD204B.C** is the only valid option and it is selected automatically.
3. The **Line Rate** field may not immediately show a clock frequency.
4. In the lower portion of the window, choose **Subclass 0** from the **Subclass** dropdown menu (see Figure 9).

The **SYNC Status** indicator may show a green check mark, a red cross, or a yellow exclamation. If **SYNC Status** indicates a yellow exclamation, refer to the JESD204B Link Does Not Come Up section.

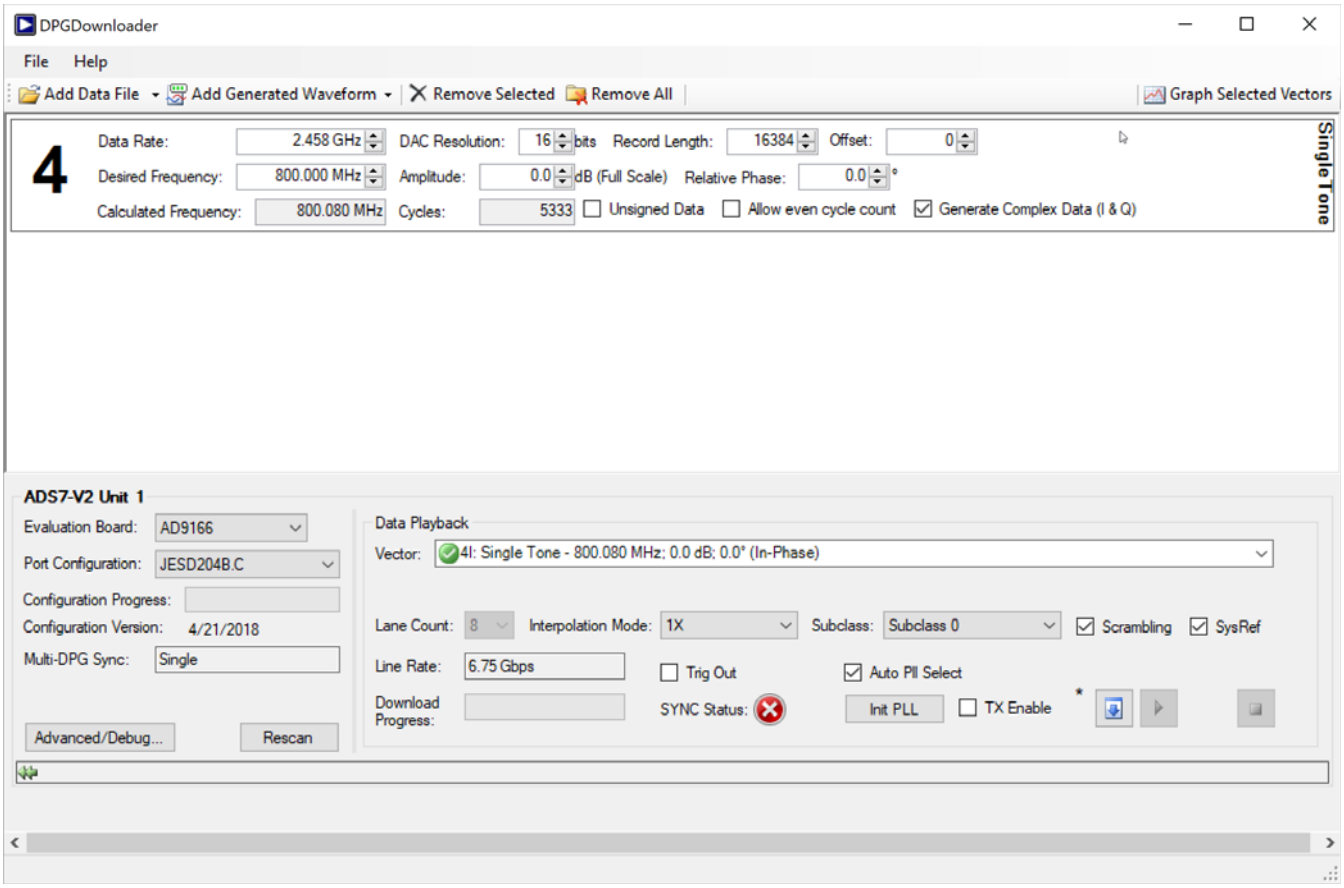

*Figure 9. **DPGDownloader** Configuration for the AD9166*

5. Select **Single Tone** from **Add Generated Waveform**, as shown in Figure 10. A single tone panel is added to the vector list.
6. Enter 2.458 GHz in **Data Rate** (or DAC clock frequency).
7. Enter 16 bits in **DAC Resolution**.
   The AD9166 resolution is 16 bits. The AD9166 can receive either 16-bit or 11-bit data because the JESD204B data packing engine packs data in 8-bit sizes. If 11-bit data is chosen, the **DPGDownloader** software appends zeros to the data-words to create 16-bit words for transfer to the data framer. Because the datapath is 16 bits, Analog Devices recommends sending 16-bit data to the device so that true 16-bit math is computed with truncation happening prior to the DAC decoder. Sending 16-bit data this way can improve spurious performance compared to sending 11-bit data.
8. Enter 800 MHz in **Desired Frequency**.
9. Keep 0.0 dB in **Amplitude**.
10. Clear the **Unsigned Data** box because the AD9166 only accepts twos complement data. Ensure that **Generate Complex Data (I & Q)** is not selected.
11. From the **Vector** dropdown list, select **4I: Single Tone – 800.080 MHz; 0.0 dB; 0.0° (In-Phase)** as the data vector.
12. Leave the other options at the default values. The **SYNC Status** indicator may show a red cross, as shown in Figure 11.
13. Click the download button to download the pattern from the computer to the ADS7-V2EBZ unit.
14. Wait for the play button to become active, and then click the play button to begin vector playback to the AD9166-FMC-EBZ evaluation board.

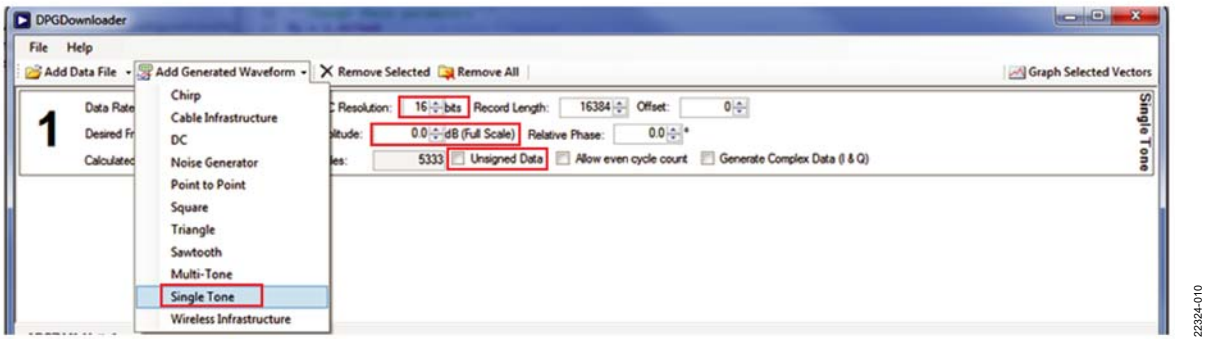

Figure 10. Choose Single Tone as the Vector Type

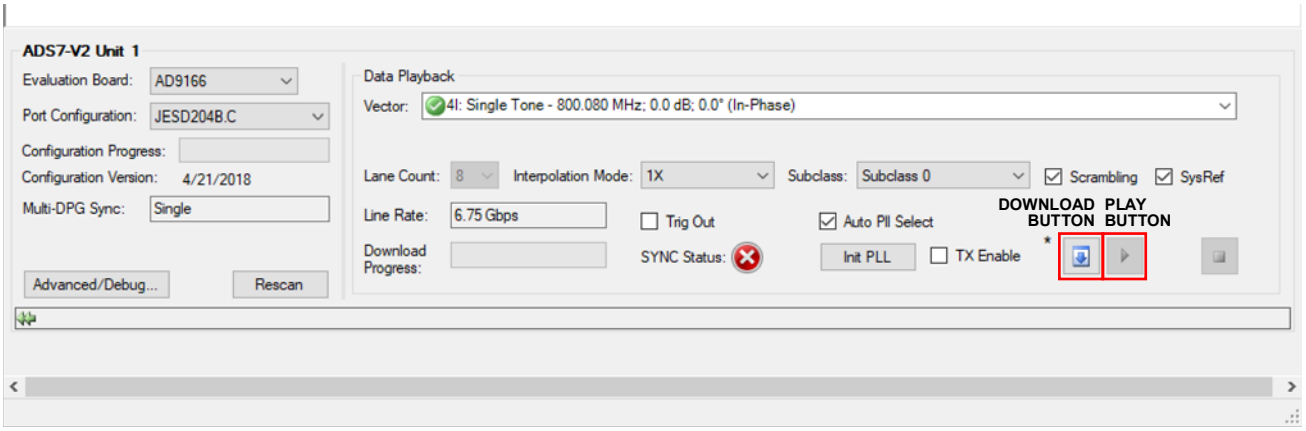

*Figure 11. **DPGDownloader**: Selected Vector and Downloaded to the ADS7-V2EBZ*

CONFIGURE THE EVALUATION BOARD

After configuring the FPGA board (ADS7-V2EBZ), configure the AD9166-FMC-EBZ evaluation board using the hardware. Perform the following steps:

1. Open the ACE software from **Start** > **Programs** > **Analog Devices** > **ACE)**. A window appears similar to Figure 5.
2. Open the evaluation board view by double clicking the AD9166-FMC-EBZ evaluation board icon, as shown in Figure 5.
3. Using the **AD9166 STARTUP WIZARD** on the left side of the window, follow these steps, as shown in Figure 12:
   a. Select **SERDES Mode** in the **Operation Mode** dropdown list.
   b. Select **ADF4372** from the **DAC Clock Source** dropdown box in the **AD9166 STARTUP WIZARD** (see Figure 4) .
   c. Set **FDAC** to 4.9152 GHz.
   d. Set **Interpolation** to 1.
   e. Set **Serdes Lanes** to 8. Note that 8 is the only supported lane number for 1× interpolation (bypass) mode. The minimum interpolation ratio is 1 for the AD9166.
   f. Click the **Apply** button at the bottom of the **AD9166 STARTUP WIZARD** window.

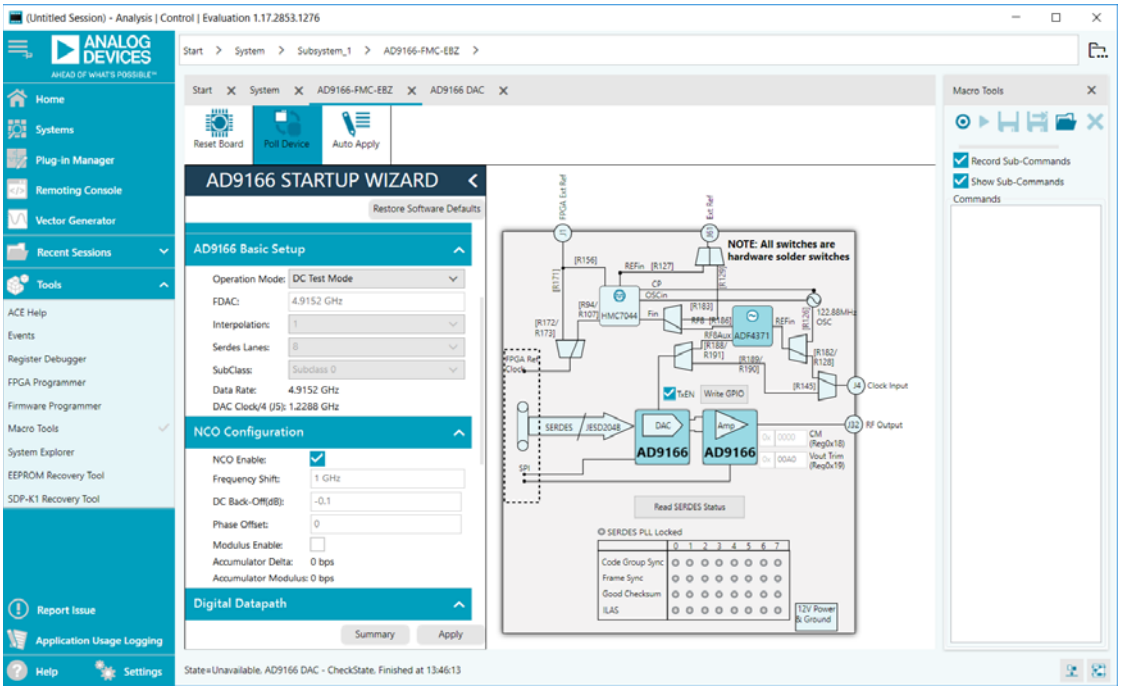

Figure 12. AD9166-FMC-EBZ Evaluation Board View and Clock Source Selection in ACE

4. Note the line rate frequency from the AD9166 in the **DPGDownloader** window as 6.75 Gbps, as shown in Figure 15. The **SYNC Status** indicator then changes to the green check mark (not shown in Figure 15). An 800 MHz single tone appears on the spectrum analyzer, as shown in Figure 14.
5. In the **NCO Configuration** section, select the **NCO Enable** box.
6. Set the **Frequency Shift** field to the desired shift frequency (in Hz).
7. Change the **DC Back-Off(dB)** box to 0 dB. This step causes the fundamental tone at 800 MHz to shift by the amount determined in the **Frequency Shift** field.
8. Click the download button in the bottom right of the **DPGDownloader** window (see Figure 11) to allow the **DPGDownloader** to create and redownload the new vector. The redownload may momentarily bring the JESD204B link down. However, the link recovers and resynchronizes, and the new output frequency displays on the spectrum analyzer.

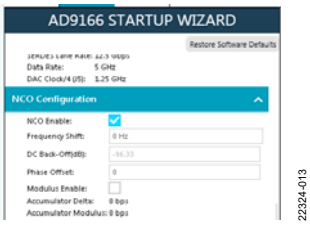

Figure 13. NCO Enabled

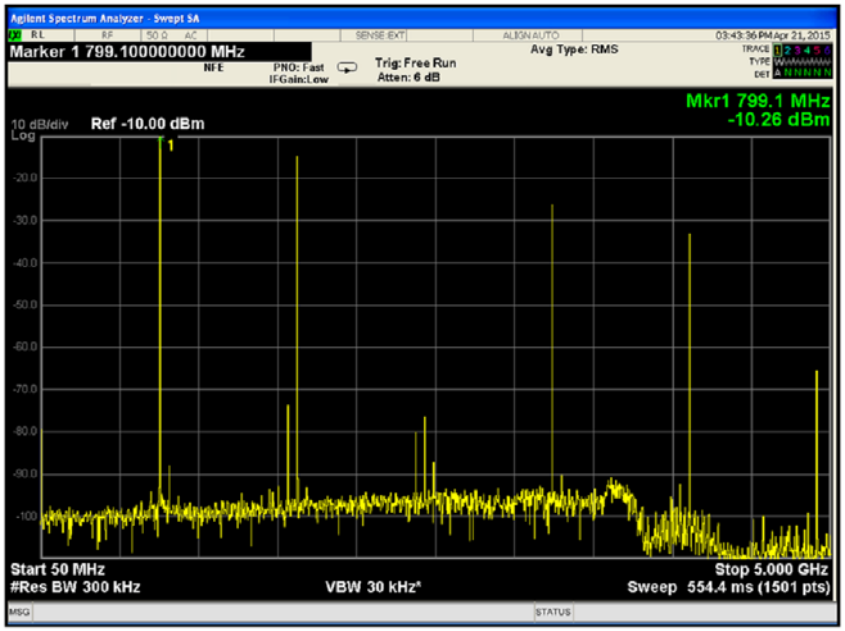

Figure 14. Spectrum Analyzer Plot of DAC Output in JESD204B Eight-lane, 1× Interpolation Mode, Showing Single Tone at 800 MHz

9. Generate and download other vectors after the JESD204B link is up.
10. Repeat Step 2 to Step 6 to run a new setting, such as a different clock rate, interpolation ratio, lanes, or reference clock.

See the Troubleshooting section for debug information (if the link disappears).

If the interpolation is equal to 1, the **DPGDownloader** software displays a single tone in the **Vector** dropdown box, as shown in Figure 15. The data type is real only (not complex) and **Interpolation Mode** is set to **1X**.

If the interpolation is greater than 1, two **Vector** dropdown boxes are displayed in the **Data Playback** section to allow downloading a complex data vector, comprising an inphase (I) and quadrature (Q) vector of equal length. The data type is complex, and **Interpolation Mode** is set to **>1X**.

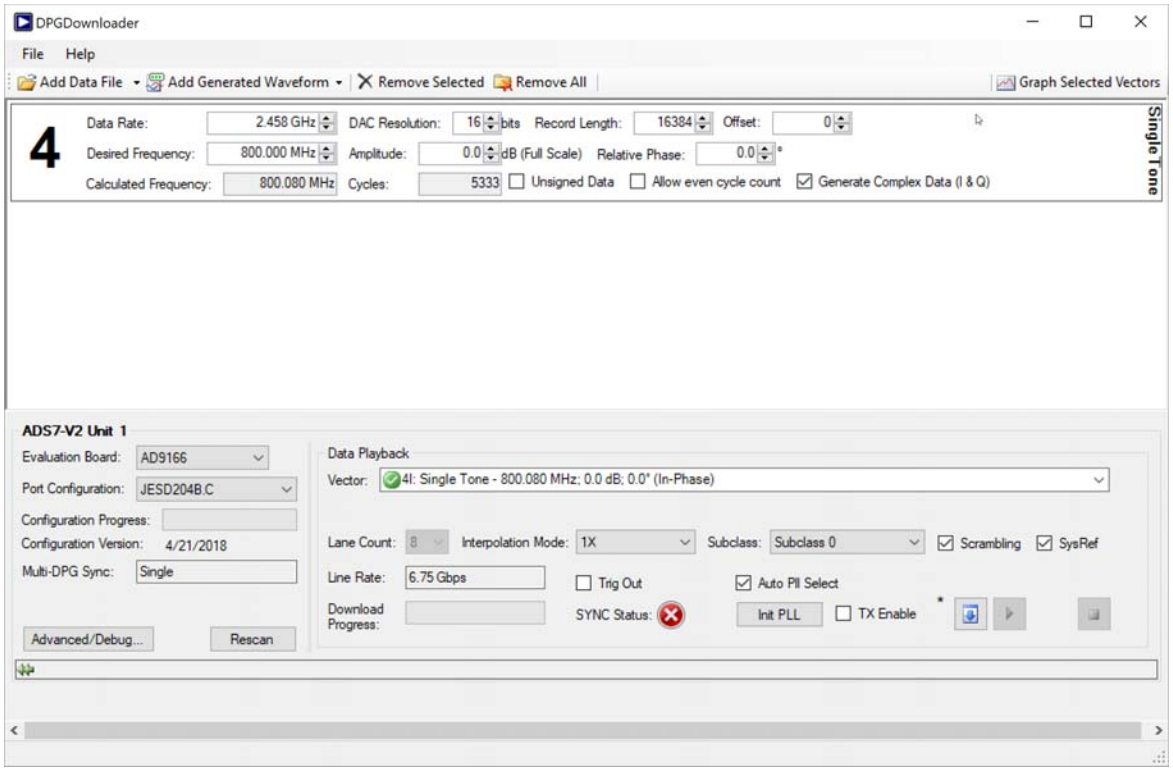

Figure 15. Download Single Tone and Play

USING EXTERNAL FILES

The **DPGDownloader** software allows users to import and use files generated outside the tool. Perform the following steps to import an external file:

1. Generate a file with the following criteria: text file signed integer, one value per line, minimum value = $-2^{(bits-1)} - 1$ (for a 16-bit DAC, this is $-(2^{15} - 1) = -32{,}767$), maximum value = $2^{(bits-1)} - 1$ (for a 16-bit DAC, this is $(2^{15} - 1) = 32{,}767$), and file length divisible by 256.
2. Import the file on **DPGDownloader** by clicking **Add Data File** (below the **File** menu).
3. Select the text file (see Figure 17).
4. Select and download this file like any other signal file. An I/Q file must be generated for any of the complex data modes.

CLOCK NETORK PERFORMANCE OPTIMIZATION

The user can measure the ADF4372 performance directly by routing the ADF4372 output to J4 and away from the AD9166 CLK± pins, by looping the RFAUX8x output toward J4 as shown in Figure 1. In this case, the AD9166 does not receive a DAC clock.

Alternatively, the ADF4372 phase noise can be inferred directly from the AD9166 output, as shown in Figure 16.

The on-board loop filter external to the ADF4372 is a standard Type II, third-order low-pass filter. The user can customize and optimize the filter by using ADIsimPLL.

The ADF4372 register settings generated by the **AD9166 STARTUP WIZARD** are typical, optimized for improved phase noise performance at the output of the ADF4372. The user can use the standalone ADF4372 tools (found in the zip file available at www.analog.com/adf4372) to regenerate new ADF4372 settings, and enter them into the register map view of the ADF4372 by selecting **ADF4372** from the **DAC Clock Source** dropdown box (see Figure 4). To simplify configuration and avoid entering commands manually into the register map one at a time, an ACE macro can be used to play a sequence. ACE macros can play a sequence of SPI commands, inserting delays to allow the PLL to lock where necessary.

The ADF4372 phase frequency detector (PFD) spur level is related to the PFD frequency. A lower PFD frequency can help reduce the PFD spur, while it also narrows the loop bandwidth and affects the PLL output phase noise. A higher PFD frequency increases the loop bandwidth and may improve the output phase noise of the PLL. Operating the ADF4372 PLL in fractional-N mode necessarily results in fractional spurs and a noticeably worse phase noise when compared to a similar frequency that allows operating the PLL in integer mode. Consult the ADF4372 data sheet for more details.

The PFD frequency typically used in the **AD9166 STARTUP WIZARD** is 245.76 MHz, generated from a 122.88 MHz VCXO, and multiplied 2× internally to the ADF4372. The user can choose the PFD frequency according to the phase noise and the PFD spur level requirements.

Optimal phase noise performance is achieved with a laboratory grade, external clock source. A comparison of various clock sources and the resulting phase noise measured at the AD9166 output is shown in Figure 16. Figure 16 compares different external clock sources with the on-board ADF4372. In this case, the AD9166 is clocked at 5898.24 MHz, a rate that is an integer multiple of 122.88 MHz. The AD9166 output is 900 MHz in NCO only mode.

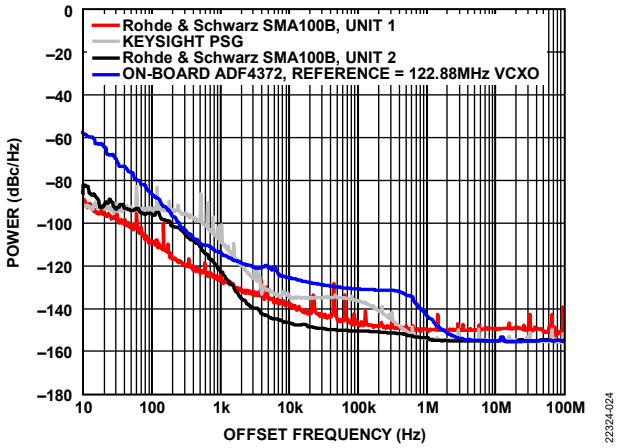

Figure 16. AD9166 Output Phase Noise

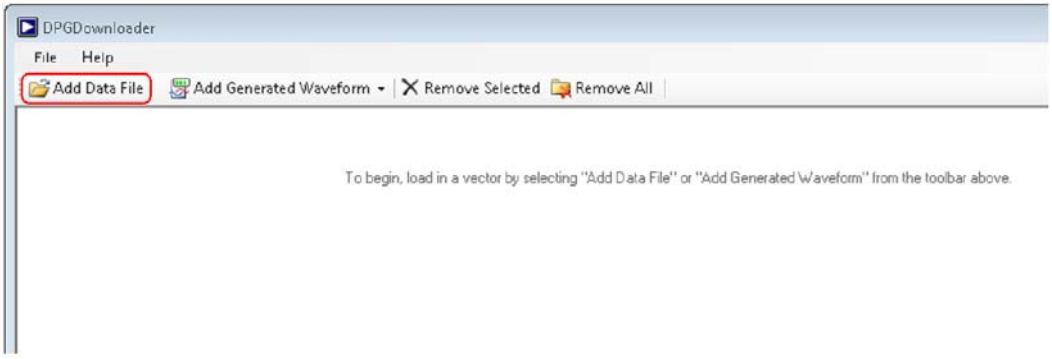

Figure 17. Choosing to Load an External File

ACE USER GUIDE

A comprehensive ACE user guide is available on the Analog Devices, Inc., website. For any general information relating to the ACE tool, refer to the ACE user guide on the Analog Devices website at https://wiki.analog.com/resources/tools-software/ace.

A typical ACE software window is shown in Figure 18. In this view, various tabs that allow control of the evaluation board hardware are shown below the red Label 1. The user can click each tab to navigate to the various windows.

In the **Select View** area (Label 2), the user can choose the memory map view as **Registers** or **Bit Fields**.

In the **Registers** view (Label 4), the full registers are shown. Some registers can be expanded to show the bit field names and descriptions that the user can view.

In the **Bit Fields** view, the bit fields are listed alphabetically and have widgets to control them and set bits, whereas in the **Registers** view, the control is by bit or hexadecimal word. Both views can program the registers and are based on user preference.

Because the AD9166 has a large register map, the **Functional Groups Filter** view (Label 3) allows the user to reduce the number of registers to view at a time.

By selecting this group and expanding the registers, the user can quickly find the registers and update their values. Click the **Apply Selected** or **Apply Changes** button above the **Select View** section (Label 2) after a register is changed to program the change to the device.

To open the **Macro Tools** section on the right (Label 5), select **Macro Tools** from the **Tools** dropdown menu to the left of the window. The **Macro Tools** section lists the macros that are currently open in the session. The user can click the name of the desired macro to make it active in the screen. Click the **Play** button (right pointing triangle) to play the selected macro.

The user can use **Search Bit Fields** (Label 6) to find a bit field.

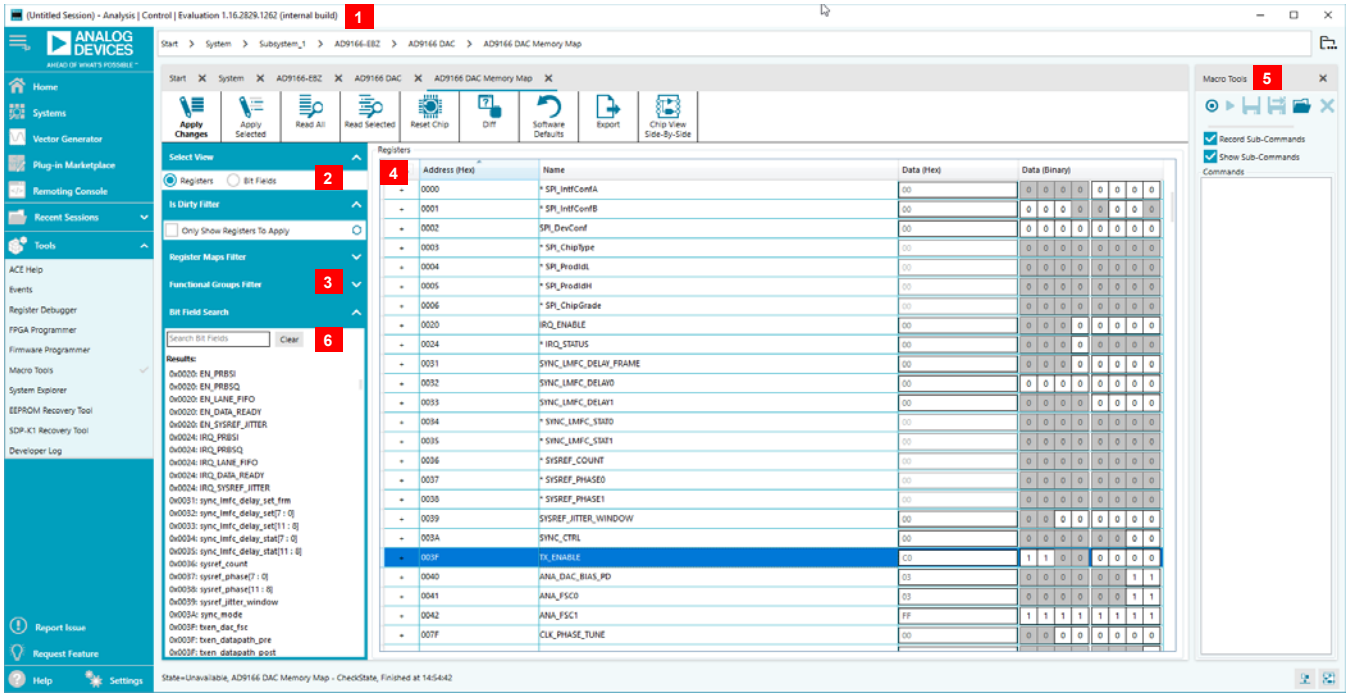

Figure 18. Functional Group View of the AD9166 in ACE

JESD204B LANE MAPPING OF THE AD9166-FMC-EBZ EVALUATION BOARD

The ADS7-V2EBZ is based on a Xilinx® Virtex®7 FPGA device. The user can configure another Xilinx Virtex7-based evaluation board to drive the AD9166-FMC-EBZ evaluation board. The JESD204B parameters are available in the AD9166 data sheet.

The physical lanes on the FMC connector are not necessarily connected to the same lane numbers as on the AD9166. The AD9166 has a crossbar switch that allows remapping the logical lanes of the JESD204B core to the correct physical lanes. However, in the case of the ADS7-V2EBZ and the AD9166, the adjustment is made using the crossbar in the Xilinx JESD204B transmitter.

The following list is the mapping between the FMC lanes and the AD9166 lanes on the AD9166-FMC-EBZ evaluation board. The mapping to the Xilinx JESD204B intellectual property (IP) is also provided in the following list for reference:

- Physical Lane 0 on the FMC connector (DP0_C2M) is also Lane 0 on the AD9166 (Lane 0 of the Xilinx JESD204B IP)
- Physical Lane 1 on the FMC connector (DP1_C2M) is also Lane 1 on the AD9166 (Lane 1 of the Xilinx JESD204B IP)
- Physical Lane 2 on the FMC connector (DP2_C2M) is also Lane 2 on the AD9166 (Lane 2 of the Xilinx JESD204B IP)
- Physical Lane 3 on the FMC connector (DP3_C2M) is also Lane 3 on the AD9166 (Lane 3 of the Xilinx JESD204B IP)
- Physical Lane 4 on the FMC connector (DP4_C2M) is Lane 5 on the AD9166 (Lane 5 of the Xilinx JESD204B IP)
- Physical Lane 5 on the FMC connector (DP5_C2M) is Lane 7 on the AD9166 (Lane 7 of the Xilinx JESD204B IP)
- Physical Lane 6 on the FMC connector (DP6_C2M) is also Lane 6 on the AD9166 (Lane 6 of the Xilinx JESD204B IP)
- Physical Lane 7 on the FMC connector (DP7_C2M) is Lane 4 on the AD9166 (Lane 4 of the Xilinx JESD204B IP)

There is also input data pin polarity (positive and negative) inversion between the transmitter and receiver on the evaluation board to ease layout. The polarity can easily be inverted in the Xilinx physical layer. Physical Lane 4 to Physical Lane 7 (DP4_C2M to DP7_C2M) on the FMC connector are inverted (positive and negative swapped).

When bringing the JESD204B link up, the user can monitor SYNCOUT± as indication of the link status.

- If SYNCOUT± stays high, as indicated by a green check mark next to **SYNC Status** (see Figure 19), the link is functional. However, if the signal spectrum appears to be incorrect, it is possible that the physical lanes were not mapped correctly.
- If SYNCOUT± toggles between states, as indicated by a yellow exclamation next to **SYNC Status**, the lane polarity (positive and negative) may be inverted.
- If SYNCOUT± remains low, as indicated by a red cross next to **SYNC Status**, there may be an issue with the reference clocks arriving to the JESD204B transmitter, the JESD204B receiver, or both.

Note that when selecting a **Lane Count** value of either 3 or 6, **Record Length** must be set to a value that is a multiple of 3. Otherwise, the spectrum does not output correctly. An example is shown in Figure 19.

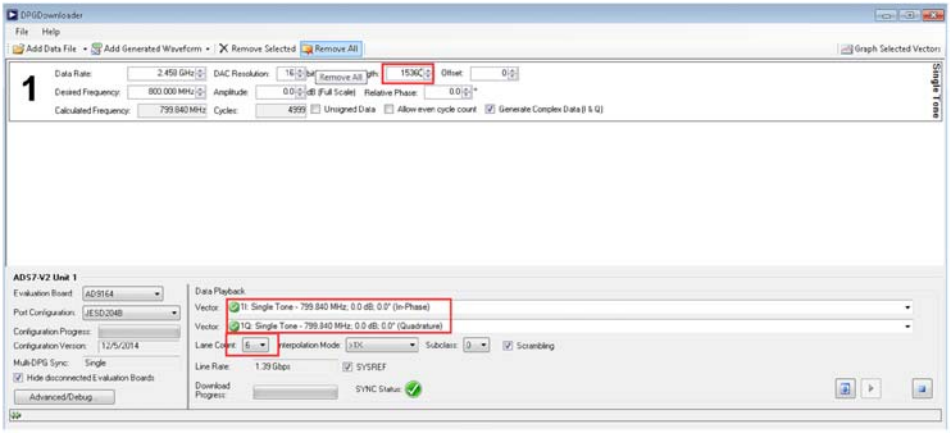

*Figure 19. **Record Length** When **Lane Count** = 3 or 6*

TROUBLESHOOTING

Debugging the Evaluation Board Using On-Board LEDs

There are six LEDs on the AD9166-FMC-EBZ evaluation board: DS1, DS2, DS3, DS4, DS5, and DS8.

- 12 V power LED: DS2 = on indicates that 12 V was applied to the evaluation board.
- LTC2928 power sequencer LEDs: DS8 = on and DS1 = off indicate that the AD9166 supplies have sequenced correctly and the monitored supplies are within the specified voltage range, according to the limits programmed in the LTC2928. DS1 = on indicates a power sequencing fault. For debugging, the response of the LTC2928 to a fault condition can be overridden by shorting the 2-pin header, P2. Shorting P2 signals to the LTC2928 to maintain power to the AD9166 despite a sequencing fault, which in turn may damage the AD9166.
- HMC7044 fault LED: DS4 = on indicates an issue with the HMC7044. When either PLL1 or PLL2 is used, an on state indicates that one of the PLLs did not lock. When PLL1 and PLL2 are not used, an on state indicates an issue with the output dividers. This LED is connected to a general-purpose input/output (GPIO) pin, and its function can be programmed by writing to the appropriate HMC7044 SPI register.
- ADF4372 fault LED: DS5 = on indicates the ADF4372 PLL locked correctly. This LED turns on only if the ADF4372 is used to generate a clock. This LED stays off by default. This LED is connected to the MUXOUT pin of the ADF4372, and its function can be programmed by writing to the appropriate ADF4372 SPI register.
- AD9166 interrupt request (IRQ) LED: DS3 is connected to the $\overline{\text{IRQ}}$ pin of the AD9166. DS3 = on may indicate an unreliable JESD204B link, or another fault as reported by the AD9166. The specific error can be read from the AD9166 registers. See the AD9166 data sheet for details. In a tested platform such as the AD9166-FMC-EBZ evaluation board, the majority of JESD204B link issues are due to improperly configured external clocking. Make sure all clocks are properly configured and are set to the correct frequencies.

When the AD9166-FMC-EBZ evaluation board is properly configured, the LEDs illuminate as follows:

- DS2 = on
- DS8 = on and DS1 = off
- DS4 = off
- DS5 = on (if the ADF4372 is used)
- DS3 = off

DPGDownloader Does Not Recognize the Evaluation Board

The AD9166-FMC-EBZ evaluation board can be run with or without an ADS7-V2EBZ, as long as it is connected across the FMC connector to a carrier board that supports the VITA 57.x standard.

When using the ADS7-V2EBZ, connect the evaluation board to its FMC connector. With a USB cable connecting the ADS7-V2EBZ to a PC, open the **DPGDownloader** software. When the **DPGDownloader** software recognizes the ADS7-V2EBZ, it attempts to read the evaluation board ID of the AD9166-FMC-EBZ through the FMC connector and across an I^2C bus. With a board recognized, the **DPGDownloader** uploads the image onto an FPGA on board the ADS7-V2EBZ. The image must correspond to the evaluation board that is connected to the ADS7-V2EBZ. With the image loaded, the ADS7 then applies power to the AD9166-FMC-EBZ evaluation board.

If the **DPGDownloader** software does not recognize the evaluation board, it does not load an FPGA image and does not apply power to the evaluation board. If no FPGA image is loaded and no power is applied to the evaluation board, confirm all hardware is properly connected. Close the **DPGDownloader** software, power down the ADS7-V2EBZ, unplug the USB cable, and gently unplug the evaluation board from the FMC connector. Inspect the FMC connector for bent pins or other damage. Then reconnect the hardware and reopen **DPGDownloader**.

If **DPGDownloader** still does not recognize the AD9166-FMC-EBZ evaluation board, make sure that it is the latest version available at wiki.analog.com/resources/eval/dpg/dacsoftwaresuite..

It is possible that the firmware on the ADS7-V2EBZ is outdated. The firmware can be updated from **DPGDownloader** if necessary. Refer to the ADS7-V2EBZ Firmware Update Needed section for more details.

DPGDownloader Does Not Recognize an ADS7-V2EBZ

To confirm that the **DPGDownloader** software recognizes a particular ADS7-V2EBZ board, connect the board to a PC using a USB cable. If the evaluation board is not connected to the FMC port of the ADS7-V2EBZ, the **DPGDownloader** software automatically loads a generic FPGA image onto the ADS7-V2EBZ. However, if the AD9166-FMC-EBZ evaluation board is connected to the FMC port, the DPG Downloader attempts to recognize the evaluation board and loads an FPGA image onto the ADS7-V2EBZ that is compatible with the AD9166-FMC-EBZ evaluation board.

JESD204B Link Does Not Come Up

The start-up sequences for the JESD204B link, as referenced in this user guide, are tested on the AD9166-FMC-EBZ evaluation board and are known to work. If the JESD204B link does not synchronize correctly (does not come up), an issue with the clocking configuration or settings is likely.

As an initial debug step, power cycle all hardware, reopen the ACE software, reopen the **DPGDownloader** software, and follow the evaluation board configuration instructions in the Hardware Setup section.

The following are some debugging suggestions for when the serializer/deserializer (SERDES) link does not come up:

- Check to ensure that the **DPGDownloader** software is configured to play a particular signal vector (sometimes called a pattern), the pattern is downloaded to the ADS7-V2EBZ memory, and the ADS7-V2EBZ is attempting to play this pattern to the evaluation board. The ADS7-V2EBZ attempts to establish a JESD204B link only after a pattern is selected and the AD9166 SYNCOUT± line is asserted. The ADS7-V2EBZ does not monitor the SYNCOUT± line if a pattern is not downloaded onto its memory.
- SYNCOUT± status is monitored by the **DPGDownloader** software through the ADS7-V2EBZ, and its status is indicated next to SYNC Status: a green check mark means the SYNCOUT± is high and the link is properly synchronized and that it is currently running. A red cross means the SYNCOUT± signal is low and the AD9166 is ready for the ADS7-V2EBZ to begin synchronization. A yellow exclamation means the SYNCOUT± signal is toggling, which indicates that an IRQ has occurred or that the link is unstable and synchronization cannot be reliably achieved. Typically, a yellow exclamation implies that either the data rate was not configured to match between ACE and the **DPGDownloader** software, or there is a bad connection on one of the used SERDES lanes. Check the FMC connector and make sure the **Data Rate** values in both ACE and **DPGDownloader** software match.
- Check that the correct JESD204B Subclass is selected. Only Subclass 0 or Subclass 1 is supported. Subclass 0 is selected by default. If Subclass 1 is selected for ADS7-V2EBZ while configuring the evaluation board for Subclass 0, the ADS7-V2EBZ waits indefinitely for a SYSREF± clock to be provided by the evaluation board. The evaluation board provides SYSREF± only when it is configured for Subclass 1, with SYSREF± generated by the HMC7044. SYSREF± cannot be provided to the ADS7-V2EBZ externally through an SMA connector on the evaluation board and without using the on-board HMC7044 clocking IC.
- Ensure that the JESD204B **Line Rate** displayed by the **DPGDownloader** is reflecting the line rate that ACE reports. The line rate, sometimes referred to as the lane rate or bit rate, is the rate at which encoded data is sampled across the SERDES lanes. This sampling clock must be generated at both the transmitter and receiver of the JESD204B link. The JESD204B transmitter of the ADS7-V2EBZ relies on an internal PLL that uses a reference at a rate equal to lane rate/40. The JESD204B receiver of the AD9166 relies on an internal PLL that uses the DAC clock as a reference. For more details, see the Evaluation Board Hardware section of this user guide and the AD9166 data sheet.

Before configuring the AD9166-FMC-EBZ evaluation board, it is a good practice to soft reset the evaluation board by clicking the **Reset Board** button in the evaluation board view of ACE (see Figure 12), or by clicking the **Reset Chip** button in the chip view (see Figure 20).

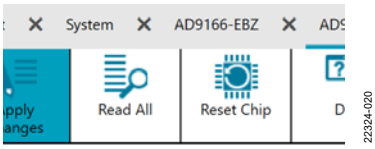

*Figure 20. **Reset Chip** in Chip View*

ACE Does Not Recognize the Evaluation Board

One of two possible errors can be generated, as shown in Figure 21 and Figure 22. Both error messages indicate that the ACE software did not recognize the AD9166-FMC-EBZ evaluation board.

ACE relies on the ADS7-V2EBZ to facilitate a connection (a bridge) to the SPI bus of the evaluation board. If the correct image was not uploaded onto the ADS7-V2EBZ by the **DPGDownloader** software, ACE is not able to communicate to the AD9166-FMC-EBZ evaluation board.

The sequence of events may matter. Some errors occur if the ACE software is started before powering up and connecting the evaluation board to the PC, or when the evaluation board is power cycled and ACE is not restarted. The simplest remedy is to power up all hardware, open **DPGDownloader**, allow the proper ADS7-V2EBZ to be loaded, and only then open ACE to configure the AD9166-FMC-EBZ.

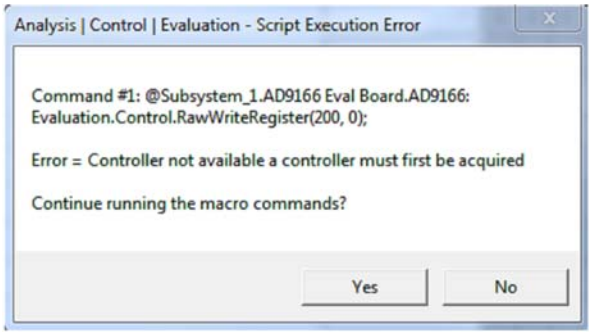

Figure 21. Script Error Window Indicating ACE Does Not Recognize the Evaluation Board

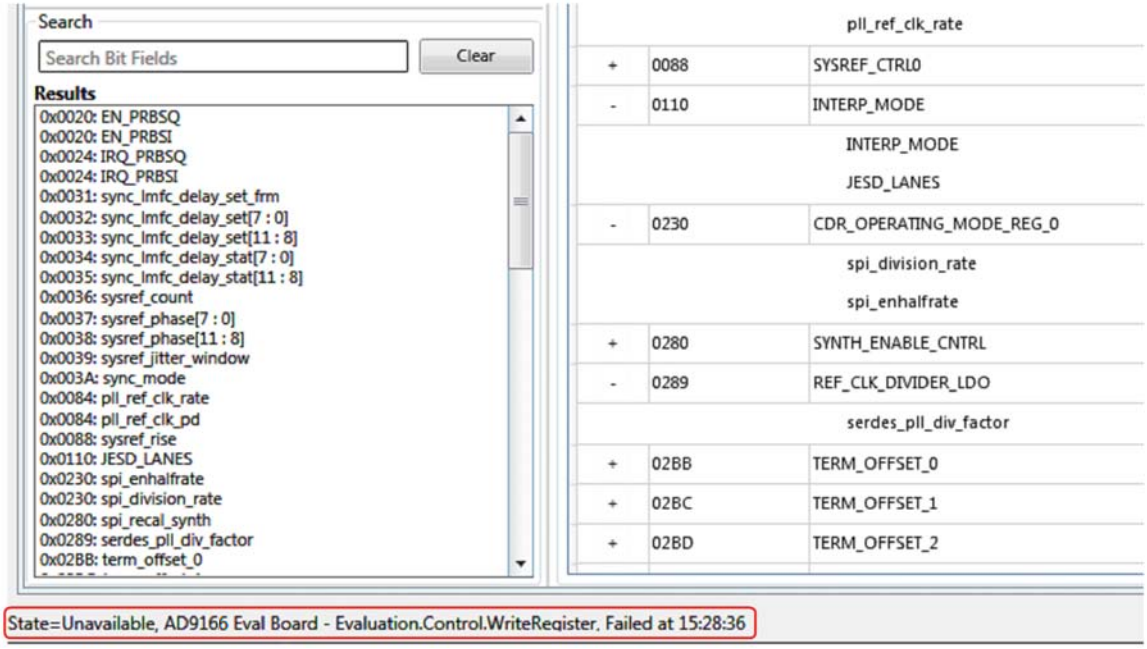

Figure 22. Register Write Error Indicating ACE Does Not Recognize the Evaluation Board

ADS7-V2EBZ Firmware Update Needed

Each ADS7-V2EBZ is loaded with the latest firmware available at the time of manufacturing. When connecting the ADS7-V2EBZ to a PC that has the latest version of **DPGDownloader** installed, **DPGDownloader** may prompt the user to update the firmware. It is a good practice to use the latest version of **DPGDownloader** and upload the latest firmware version to the ADS7-V2EBZ.

To manually update the ADS7-V2EBZ firmware, open the **DPGDownloader** application and click the **Advanced/Debug** button, as shown in Figure 23. Click the **Update** button. The updater then runs and installs the firmware update. After the firmware is updated, it may be necessary to power cycle the ADS7-V2EBZ board and to close and reopen the **DPGDownloader** to apply the update.

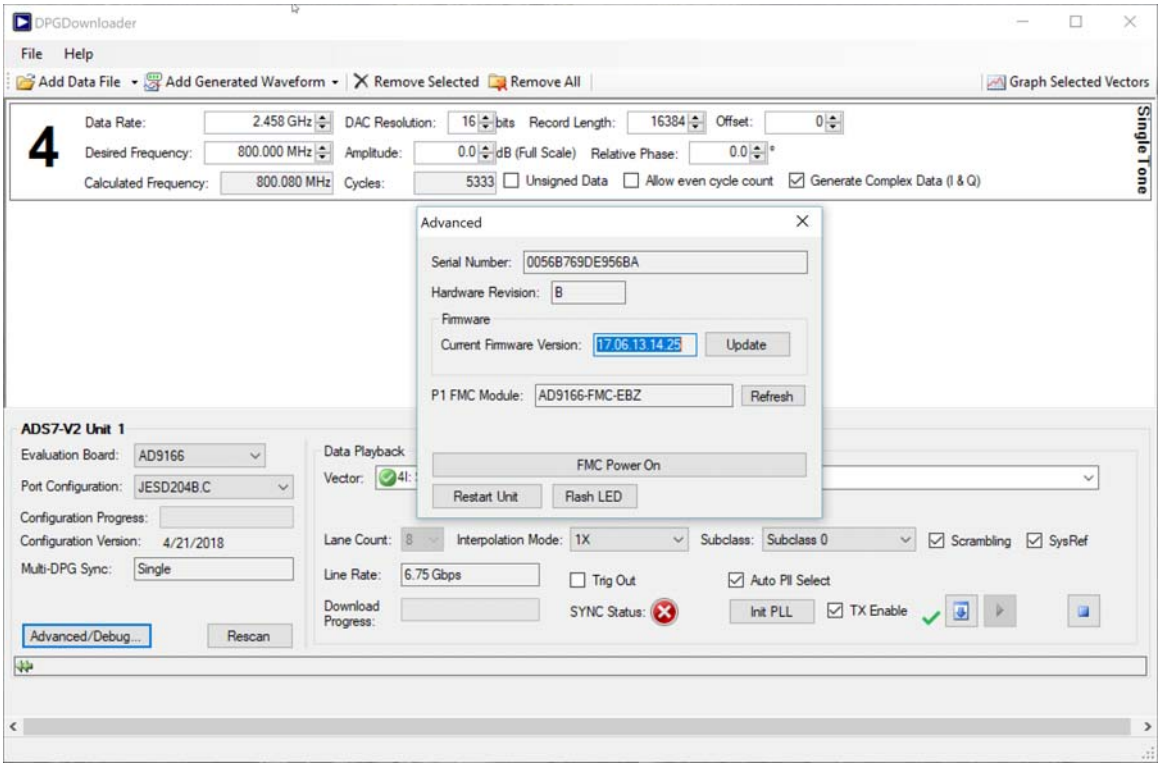

Figure 23. Updating the ADS7-V2EBZ Firmware Version

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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