DS2485 Advanced 1-Wire Master with Memory

General Description

The DS2485 is a 1-Wire® master that performs protocol conversion between the I²C master and any attached 1-Wire slaves. For 1-Wire line driving, internal user-adjustable timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. The 1-Wire master has selectable active or passive 1-Wire pullup. Strong pullup features support 1-Wire power delivery for 1-Wire devices that require this for EEPROMs and cryptographic computations.

Applications

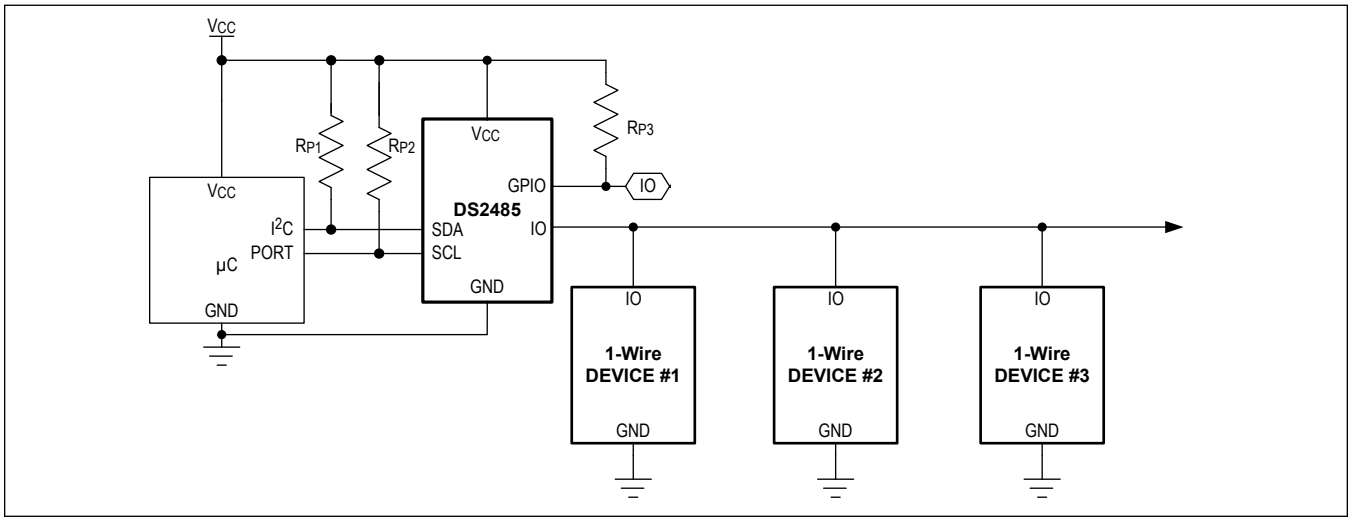
- Medical Instruments
- Industrial Sensors and Tools
- Limited-Use Consumables
- Printer Cartridge Identification

Benefits and Features

- I²C Communication, up to 1MHz
- 1-Wire Standard and Overdrive Timing Communication Speeds
- 1-Wire Command Scripting Capability
- Adjustable 1-Wire Timing for t_{RSTL}, t_{MSI}, t_{MSP}, t_{RSTH}, t_{W0L}, t_{W1L}, t_{MSR}, t_{REC}, RPUP, and PDSLEW
- 0.75Kb of EEPROM for User Data
- One Open-Drain GPIO Pin
- Large 1-Wire Block Buffer (126 Bytes) for Efficient Data Transfer
- Operating Range: 2.97V to 3.63V, -40°C to +85°C
- 3mm x 3mm, 6-Pin TDFN-EP Package

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to GND ..... -0.5V to 4.0V
Maximum Current into Any Pin..... -20mA to 20mA
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-40°C to +125°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 TDFN-EP

Package Code	T633+2
Outline Number	21-0137
Land Pattern Number	90-0058
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	55°C/W
Junction to Case (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	42°C/W
Junction to Case (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(*Note 1*)	2.97	3.3	3.63	V
Supply Current	I_{CC}	Standby			400	µA
		Communicating/active (*Note 2*)			10	mA
1-Wire Input High	V_{IH1}	Low configuration	0.6 x V_{CC}			V
		Medium configuration	0.6 x V_{CC}			
		High configuration	0.85 x V_{CC}			
Low-to-High Switching Threshold	V_{TH}	Low configuration (*Note 3*, *Note 4*)		0.25 x V_{CC}		V
		Medium configuration (*Note 3*, *Note 4*)		0.4V x V_{CC}		
		High configuration (*Note 3*, *Note 4*)		0.75 x V_{CC}		

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1-Wire Input Low	V_{IL1}	Low configuration			0.15 x V_{CC}	V
		Medium configuration			0.3 x V_{CC}	
		High configuration			0.3 x V_{CC}	
High-to-Low Switching Threshold	V_{TL}	(*Note 3*, *Note 5*)		0.65 x V_{CC}		V
Switching Hysteresis	V_{HY}	(*Note 3*, *Note 6*)		0.3		V
1-Wire Weak Pullup Resistor (Notes 3, 7)	R_{WPU}	Ultra-low range	250	333	675	Ω
		Low range	375	500	750	
		High range	750	1000	1400	
		External high impedance		10M		
1-Wire Output Low	V_{OL1}	V_{CC} = 2.97V, 4mA sink current			0.28	V
Active Pullup on Threshold	V_{IAPO}	Low configuration (*Note 3*)		0.25 x V_{CC}		V
		Medium configuration (*Note 3*)		0.4 x V_{CC}		
		High configuration (*Note 3*)		0.75 x V_{CC}		
Active Pullup on Time (Notes 3, 8)	t_{APU}	1-Wire standard speed (default value)		2.5		µs
		1-Wire overdrive speed (default value)		0.5		
Active Pullup Impedance	R_{APU}	V_{CC} = 2.97V, 10mA load (*Note 3*)			50	Ω
IO PIN: 1-Wire TIMING (*Note 9*)						
1-Wire Output Fall Time (*Note 3*)	t_F	Standard and overdrive		Settable		µs
Reset Low Time	t_{RSTL}	Standard and overdrive	-5%	Settable	+5%	µs
Reset High Time	t_{RSTH}	Standard and overdrive (*Note 10*)	-5%	Settable	+5%	µs
Presence-Detect Sample Time	t_{MSP}	Standard and overdrive	-5%	Settable	+5%	µs
Sampling for Short and Interrupt	t_{MSI}	Standard and overdrive	-5%	Settable	+5%	µs
Write-One/Read Low Time	t_{W1L}	Standard and overdrive	-5%	Settable	+5%	µs
Read Sample Time	t_{MSR}	Standard and overdrive	-5%	Settable	+5%	µs
Write-Zero Low Time	t_{W0L}	Standard and overdrive	-5%	Settable	+5%	µs
Recovery Time	t_{REC}	Standard and overdrive (*Note 10*)	-5%	Settable	+5%	µs
1-Wire Time Slot	t_{SLOT}	Standard and overdrive		t_{W0L} + t_{REC}		µs

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1-Wire FUNCTIONS						
Operation Time	t_{OP}	(*Note 3*)			400	µs
Sequence Time	t_{SEQ}	(*Note 3*)			10	µs
EEPROM						
Read Memory	t_{RM}				50	ms
Write Memory	t_{WM}				100	ms
Write State	t_{WS}				15	ms
Write/Erase Cycles (Endurance)	N_{CY}	T_A = +85°C (*Note 12*)	100K			
Data Retention	t_{DR}	T_A = +85°C (*Note 13*, *Note 14*)	10			years
GPIO PIN						
Output Low	GPIO V_{OL}	GPIOI_{OL} = 4mA (*Note 15*)			0.4	V
Input Low	GPIO V_{IL}		-0.3		0.2 x V_{CC}	V
Input High	GPIO V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Leakage Current	GPIO I_L		-1		+1	µA
I^2C SCL AND SDA PINS (*Note 16*)						
Low-Level Input Voltage	V_{IL}		-0.3		0.2 × V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 × V_{CC}		V_{CC} + 0.3V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	(*Note 3*)		0.05 × V_{CC}		V
Low-Level Output Voltage at 4mA Sink Current	V_{OL}	(*Note 15*)			0.4	V
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}	(*Note 3*)		30		ns
Pulse Width of Spikes That Are Suppressed by the Input Filter	t_{SP}	(*Note 3*)			50	ns
Input Current with an Input Voltage Between 0.1V_{CCMAX} and 0.9V_{CCMAX}	I_I	(*Note 3*, *Note 17*)	-1		+1	µA
Input Capacitance	C_I	(*Note 3*)		10		pF
SCL Clock Frequency	f_{SCL}	(*Note 1*)	0		1	MHz
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.45			µs

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Period of the SCL Clock	t_{LOW}	(*Note 18*)	0.65			µs
High Period of the SCL Clock	t_{HIGH}	(*Note 3*)	0.35			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	(*Note 3*)	0.35			µs
Data Hold Time	$t_{HD:DAT}$	(*Note 3*, *Note 18*, *Note 19*)			0.35	µs
Data Setup Time	$t_{SU:DAT}$	(*Note 3*, *Note 18*, *Note 20*)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(*Note 3*)	0.35			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	(*Note 3*)	0.6			µs
Capacitive Load for Each Bus Line	C_B	(*Note 1*, *Note 21*)			400	pF
Warmup Time	t_{OSCWUP}	(*Note 4*, *Note 22*)			1	ms

Note 1: System requirement.

Note 2: Operating current with a 1-Wire write byte sequence followed by continuous write/read of the 1-Wire Block command at 1MHz in overdrive.

Note 3: Guaranteed by design and/or characterization only. Not production tested.

Note 4: Voltage above which, during a rising edge on IO, a logic 1 is detected.

Note 5: Voltage below which, during a t_F on IO, a logic 0 is detected.

Note 6: After V_{TH} is crossed during a rising edge on IO for high configuration only, the voltage on IO must drop by at least V_{HY} to be detected as logic 0.

Note 7: Active pullup or resistive pullup and range are configurable.

Note 8: The active pullup does not apply to the rising edge of a presence pulse outside of a 1-Wire reset cycle or during the recovery after a short on the 1-Wire line.

Note 9: All 1-Wire timing specifications are derived from the same timing circuit.

Note 10: Up to an additional 10µs of idle high time may occur between a 1-Wire reset cycle and the first time slot, or between each 1-Wire byte during a command sequence.

Note 11: Current drawn from V_{CC} during the EEPROM programming interval or SHA-3 computation.

Note 12: Write-cycle endurance is tested in compliance with JESD47G.

Note 13: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 14: Data retention is tested in compliance with JESD47G.

Note 15: The I-V characteristic is linear for voltages less than 1V.

Note 16: All I^2C timing values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 17: The IO pins of the DS2485 do not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 18: t_{LOW} min = $t_{HD:DAT}$ max + 200ns for rise or fall time + $t_{SU:DAT}$ min. Values greater than these can be accommodated by extending t_{LOW} accordingly.

Note 19: The DS2485 provides a hold time of at least 100ns for the SDA signal (referenced to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

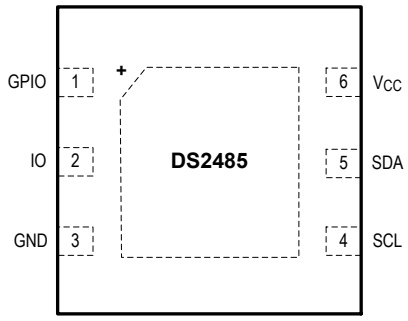
Note 20: The DS2485 can be used in a standard-mode I^2C-bus system, but the requirement of $t_{SU:DAT} \geq 250ns$ must then be met. Also, the acknowledge timing must meet this setup time (I^2C bus specification Rev. 03, 19 June 2007).

Note 21: C_B = total capacitance of one bus line in pF. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application (I^2C bus specification Rev. 03, 19 June 2007).

Note 22: I^2C communication should not take place for the max t_{OSCWUP} time following a power-on reset.

Pin Configuration

TOP VIEW



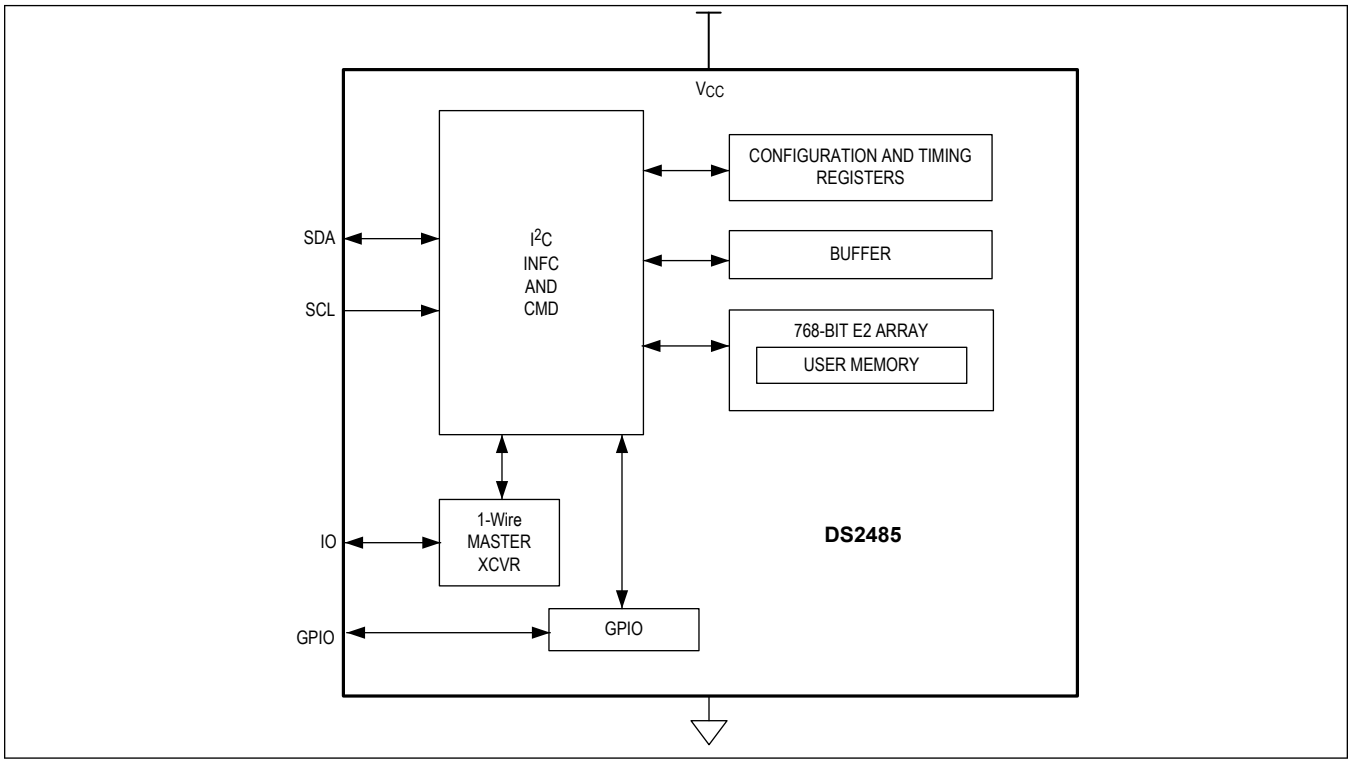
TDFN-EP
3mm x 3mm

Pin Description

PIN	NAME	FUNCTION
1	GPIO	Open-Drain, General-Purpose Input/Output. Requires external pullup resistor to V_{CC} when used as an output.
2	IO	1-Wire Input/Output Driver. The 1-Wire line can be pulled up by an internal weak pullup (R_{WPU}), an external pullup, or have both an external pullup and internal weak pullup.
3	GND	Ground
4	SCL	I^2C Serial Clock Input. Must be connected to V_{CC} through a pullup resistor.
5	SDA	Open-Drain, I^2C Serial Data Input/Output. Must be connected to V_{CC} through a pullup resistor.
6	V_{CC}	Power Supply Input
–	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.

Functional Diagrams

Simplified Block Diagram



Detailed Description

The DS2485 is a 1-Wire master that performs protocol conversion between the I^2C master and any attached 1-Wire slaves. For 1-Wire line driving, internal user-adjustable timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. The advanced self-timed 1-Wire master has selectable active or passive 1-Wire pullup. Strong pullup features support 1-Wire power delivery for 1-Wire devices that require this for EEPROMs and cryptographic computations. Once supplied with a command and data, the input/output controller of the DS2485 performs time-critical 1-Wire communication functions such as reset/presence-detect cycle, read-byte, write-byte, read-block, write-block, single-bit R/W, triplets for ROM Search, and full command sequences for 1-Wire authenticators without requiring interaction with the host processor. The GPIO pin can be independently operated under command control. Additionally, the DS2485 provides three pages of user memory. The DS2485 communicates with a host processor through its I^2C bus interface in standard mode or in fast mode up to 1MHz. The DS2485 is not compatible with the DS2482/DS2483/DS2484 devices.

Design Resource Overview

Operation of the DS2485 involves configuring the 1-Wire master and then performing individual 1-Wire commands or grouping them into a series of primitive 1-Wire commands.

Memory

The DS2485 has a 0.75Kb EEPROM array of general-purpose, user-programmable memory organized into three pages of 32-bytes with even-numbered addresses. Odd-numbered pages are not available for use and are write protected. Each even-numbered page has optional protection modes.

Table 1. User Memory Map with Default Protections

PAGE	REGION	MEMORY TYPE	DEFAULT PROTECTION	CONFIGURABLE PROTECTION
0	User Page	EE		WP, NONE
1	Reserved Page	—	WP	
2	User Page	EE		
3	Reserved Page	—	WP	
4	User Page	EE		
5	Reserved Page	—	WP	

PROTECTION MODE ABBREVIATION*	DESCRIPTION
WP	Write protect.
NONE	No protection on User Page. This locks the protection feature and does not allow any protection to be set.

**Protection mode restrictions: Protection for a page can only be set once.*

Open-Drain GPIO

A dedicated volatile memory region is used to control and/or read the open-drain GPIO pin. Upon power-up, the GPIO pin is high impedance.

1-Wire Master

The 1-Wire master reports data and status from the 1-Wire side to the host processor.

Transaction Sequence

The protocol for accessing a connected slave device through the 1-Wire master is as follows:

- Initialization

- ROM Function command
- Device Function command
- Transaction/data

Power-Up 1-Wire Bus

On power-up, the DS2485 1-Wire master defaults with the 1-Wire bus in the “float condition,” per Table 37. After power-up, this setting must be changed for correct 1-Wire operation. Set register RPUP/BUF for correct 1-Wire operation. For most applications with only one 1-Wire slave device, the recommendation is to set the RPUP/BUF register to 6h, per Table 34. After setting RPUP/BUF, a 1-Wire reset must be performed with any command that can perform that operation.

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the 1-Wire master, followed by a presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the slave is on the bus and is ready to operate. For more details, see the *1-Wire Signaling and Timing* section.

1-Wire Signaling and Timing

The 1-Wire protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the 1-Wire master initiates all falling edges. The 1-Wire master can communicate at two speeds: standard and overdrive. While in overdrive mode, the fast timing applies to all waveforms.

Figure 1 shows the initialization sequence required to begin any communication. A reset pulse followed by a presence pulse indicates that a slave is ready to receive data, given the correct ROM and device function command.

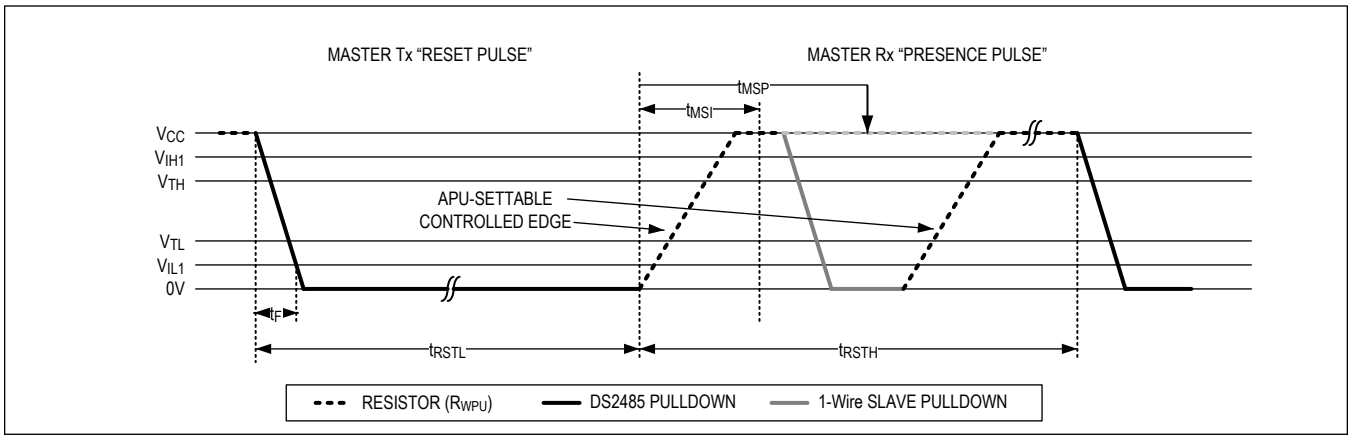


Figure 1. 1-Wire Reset/Presence-Detect Cycle

Read/Write Time Slots

Data communication on the 1-Wire bus takes place in time slots that carry a single bit each. Write time slots transport data from the 1-Wire master to a connected slave. Read time slots transfer data from the slave to the 1-Wire master. Figure 2 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the slave starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until

the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window required by the slave. After the V_{TH} threshold has been crossed, the DS2485 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time (t_{RL}) is expired. During the t_{RL} window, when responding with a 0, the slave starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the slave does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over. Note that the slave t_{RL} during a logic 1 is adequately an approximation of the 1-Wire master t_{W1L} setting.

The slave t_{RL} plus the bus rise time on the near end and the internal timing generator of the slave on the far end define the 1-Wire master sampling window in which the 1-Wire master performs a read from the data line. After reading from the data line, the 1-Wire master waits until t_{SLOT} is expired. This guarantees sufficient recovery time (t_{REC}) for the slave to get ready for the next time slot. Note that t_{REC} ;specified herein applies only to a single slave attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance.

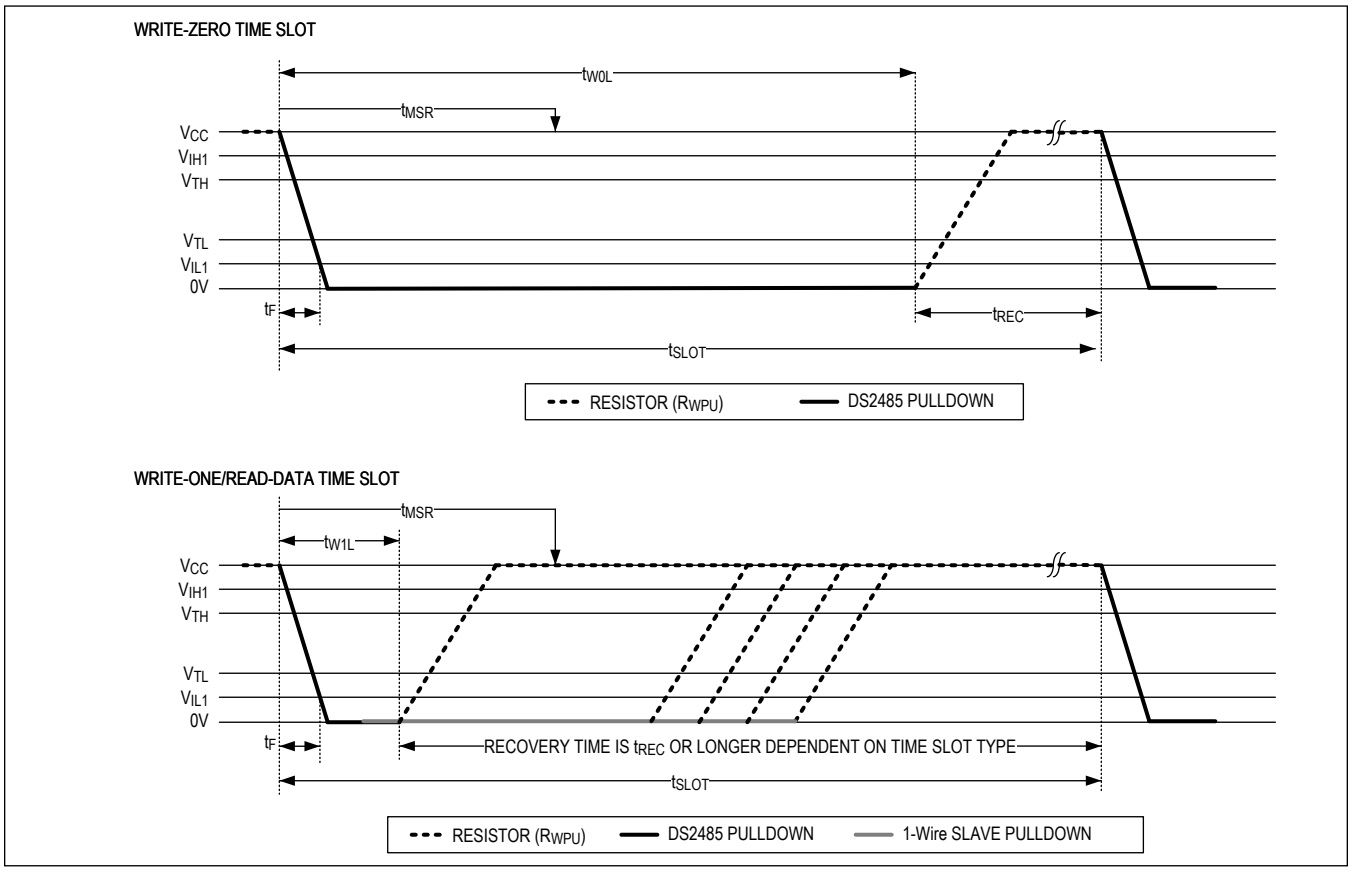


Figure 2. Read/Write Timing Diagrams

Strong Pullup

The strong pullup function can be activated prior to a 1-Wire Write Byte, 1-Wire Read Byte, 1-Wire Single Bit, 1-Wire Block, or 1-Wire Write Block command. Strong pullup is commonly used with 1-Wire EEPROM devices when copying buffer data to the main memory. The respective device data sheets specify the location in the communications protocol after which the strong pullup should be applied. The strong pullup can be enabled immediately prior to issuing the

command that puts the 1-Wire device into the state where it needs the extra power for primitive 1-Wire commands or as an integral part of advanced commands. The strong pullup uses the same internal pullup transistor as the active pullup feature. See the R_{APU} parameter in the *Electrical Characteristics* table to determine whether the voltage drop is low enough to maintain the required 1-Wire voltage at a given load current and supply voltage. If the strong pullup is enabled, the DS2485 treats the rising edge of the time slot in which the strong pullup starts as if the active pullup was activated. However, in contrast to the active pullup, the strong pullup (i.e., the internal pullup transistor) remains conducting, as shown in Figure 3, until the DS2485 receives a command that generates 1-Wire communication (the typical case), or until the strong pullup is disabled or the 1-Wire master is reset. When the strong pullup ends, it is automatically disabled. Using the strong pullup feature does not change the active pullup settings.

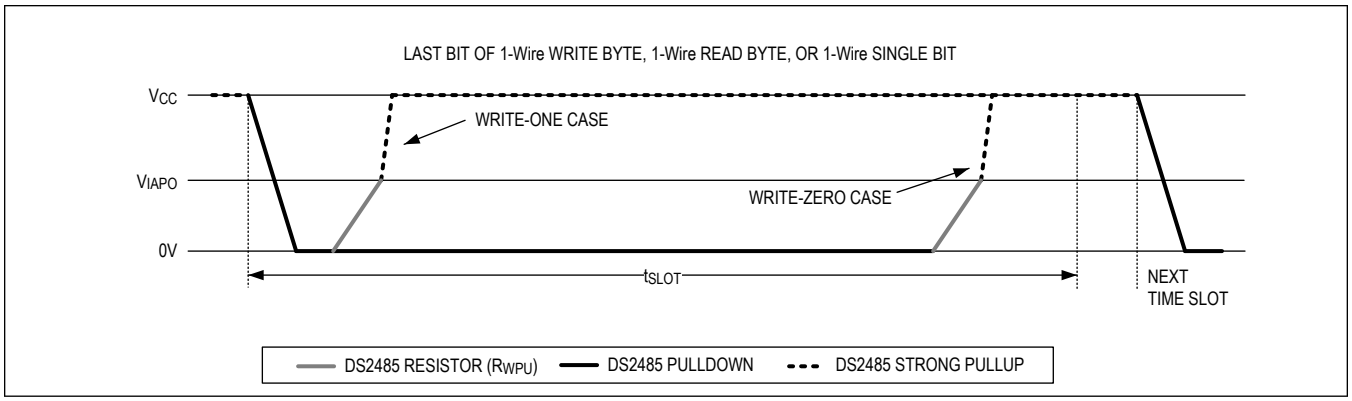


Figure 3. Strong Pullup Timing

Active Pullup (APU)

The APU is a function that accelerates the rise time during a 1-Wire reset cycle, write time slot, or read time slot. The 1-Wire master triggering mechanism is always ready after the initial low time of a 1-Wire reset cycle or time slot completes. This rise-time acceleration is accomplished by an active pullup impedance (R_{APU}) that begins driving once the active pullup on threshold (V_{IAPO}) is crossed from low to high. APU does not apply to the rising edge of a recovery from a short on the line, a power-up presence pulse of a slave, or any other event outside of a 1-Wire reset cycle or a time slot. Enabling APU is generally recommended for best 1-Wire performance.

Active Pullup for 1-Wire Reset Cycle

Figure 4 illustrates an active pullup for a 1-Wire reset cycle. A 1-Wire reset cycle begins by driving the line low for a t_{RSTL} period. When the t_{RSTL} expires, the APU triggering mechanism is on and triggers when the V_{IAPO} level is crossed from low to high. APU then remains on for a duration of t_{APU}. After the completion of t_{APU}, the APU trigger mechanism is reset to be on again and triggers when the V_{IAPO} level is crossed from low to high upon a presence pulse completing. APU then remains on until the duration of t_{RSTH} expires.

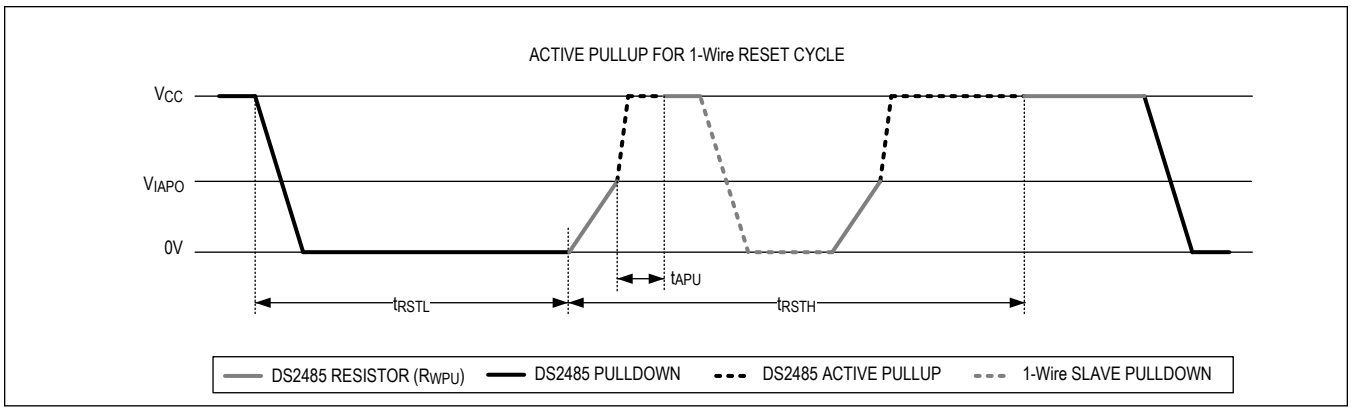


Figure 4. Active Pullup for a 1-Wire Reset Cycle

Active Pullup for Read/Write Time Slots

Figure 5 illustrates an active pullup for a 1-Wire write-zero or write-one time slot. A write-zero time slot begins by the 1-Wire master driving the line low for a t_{W0L} period. When the t_{W0L} expires, the APU triggering mechanism is on and triggers when the V_{IAPO} level is crossed from low to high. APU then remains on until t_{REC} expires. A write-one time slot begins by the 1-Wire master driving the line low for a t_{W1L} period. When the t_{W1L} expires, the APU triggering mechanism is on and triggers when the V_{IAPO} level is crossed from low to high. Unlike the write-zero time slot, the write-one time slot has APU for a much longer recovery duration defined by $(t_{W0L} - t_{W1L}) + t_{REC}$.

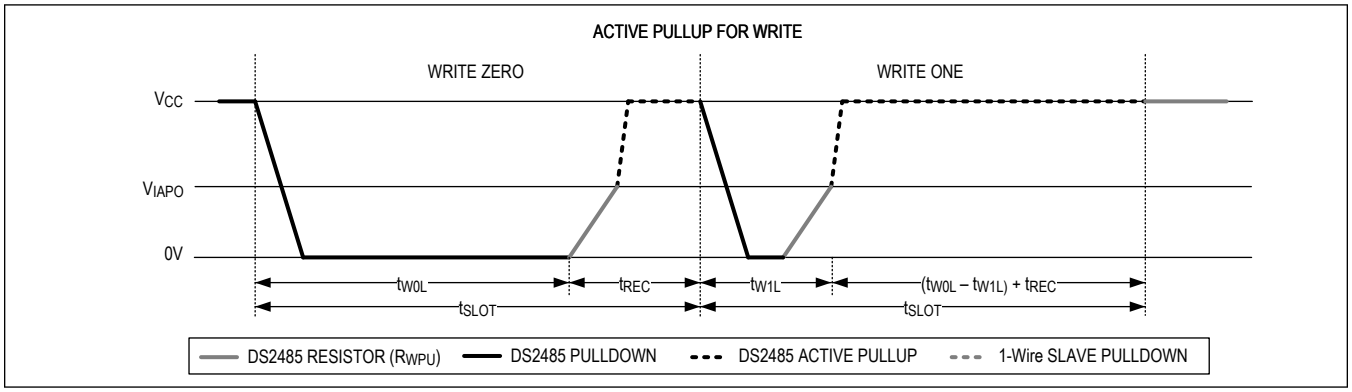


Figure 5. Active Pullup for 1-Wire Write Time Slot

Figure 6 illustrates an active pullup for 1-Wire read time slots. On a 1-Wire read-zero time slot, the master pulls the line low. The slave detects the low, and takes over driving the line. At that point, both the master and slave are driving the line low until t_{W1L} expires. After t_{W1L}, the master turns on the normal pullup (R_{WPU}), and enables the APU triggering mechanism. The master samples the read data at t_{MSR}. After the slave response time (t_{SPD}) expires, the slave releases the line. The APU triggers when the V_{IAPO} level is crossed from low to high. The APU remains on until the end of the slot as defined in Figure 6. On a 1-Wire read-one time slot, the master pulls the line low for t_{W1L}. The slave detects the low, but does not drive the line. When the t_{W1L} expires, the master turns on the normal pullup and enables the APU triggering mechanism. The APU triggers when the V_{IAPO} level is crossed from low to high. The APU remains on until the end of the slot as defined by $(t_{W0L} - t_{W1L}) + t_{REC}$. The read-one recovery time is longer than the read-zero case.

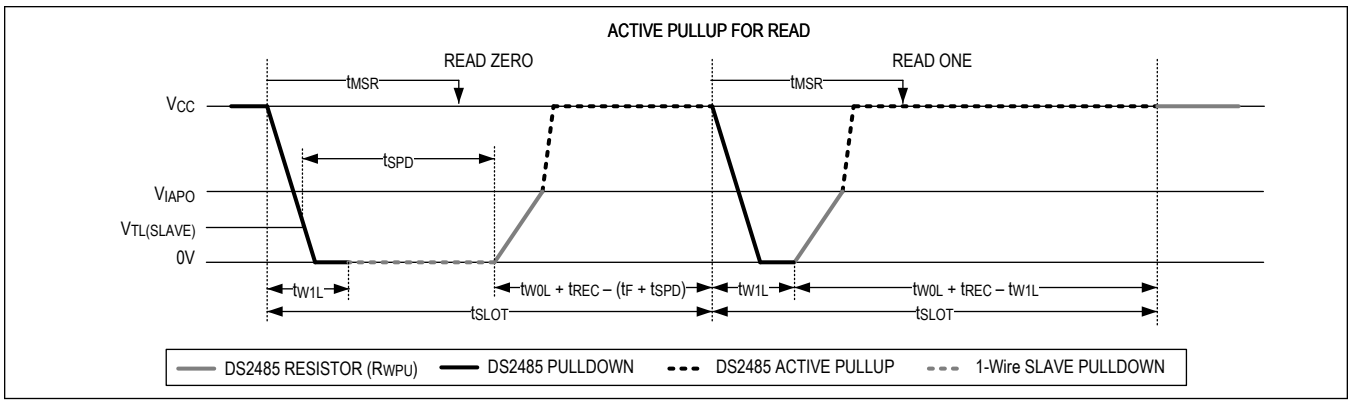


Figure 6. Active Pullup for 1-Wire Read Time Slot

I²C

General Characteristics

The I²C bus uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the I²C bus can be transferred at rates of up to 100kbps in standard mode and up to 400kbps in fast mode. The DS2485 works in both modes or up to a clock rate of 1MHz. A device that sends data on the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls the communication is called a master. The devices that are controlled by the master are slaves. To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus. Data transfers can be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP (Figure 7). Data is transferred in bytes, with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

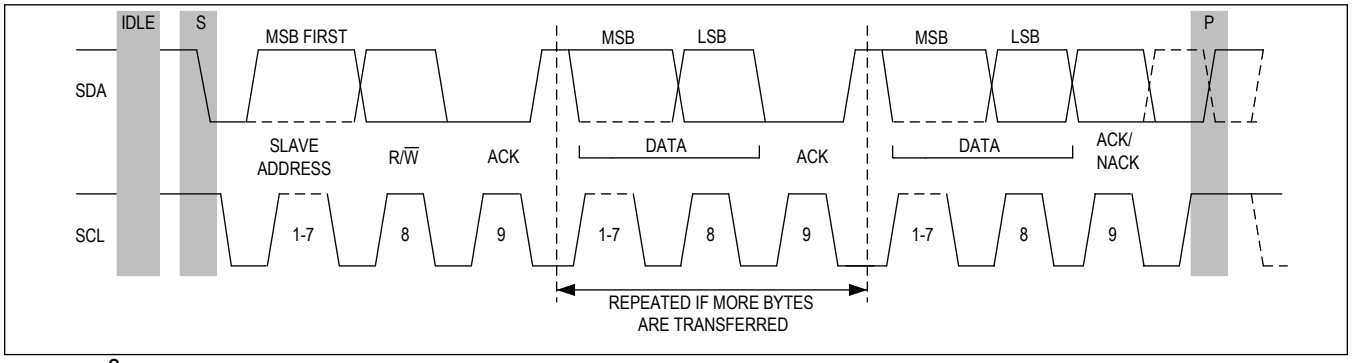


Figure 7. I²C Protocol Overview

Slave Address

The slave address to which the DS2485 responds is shown by default in Figure 8. The slave address is part of the slave address/control byte. The last bit of the slave address/control byte (R/W) defines the data direction. When set to 0, subsequent data flows from the master to the slave (write access); when set to 1, data flows from the slave to the master (read access). The default address can be changed with the Set I2C Address command.

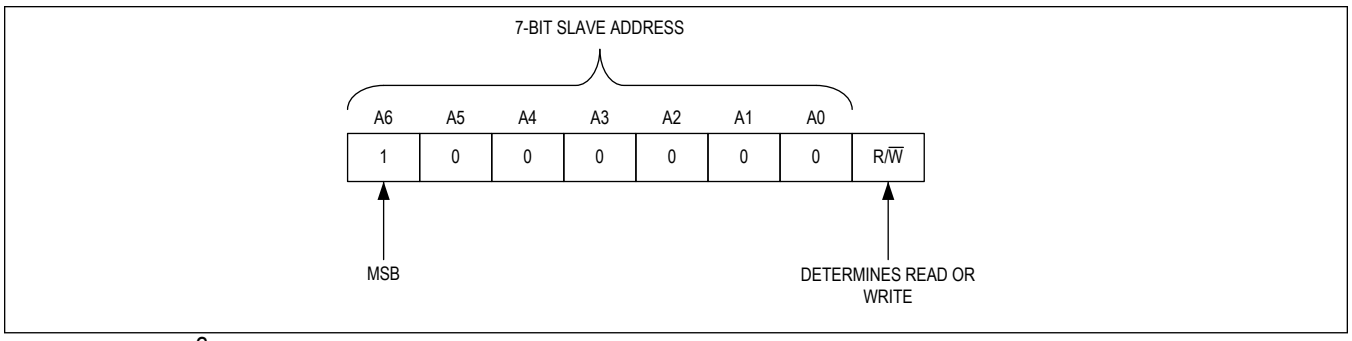


Figure 8. DS2485 I²C Slave Address

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. The timing references are defined in Figure 9.

Bus Idle or Not Busy

Both SDA and SCL are inactive and in their logic-high states.

START Condition

To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

STOP Condition

To end communication with a slave, the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

Repeated START Condition

Repeated STARTs are commonly used for read accesses after having specified a memory address to read from in a preceding write access. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid

With the exception of the START and STOP conditions, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see Figure 9). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL pulse.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT}$, + t_R in Figure 9) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse, and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

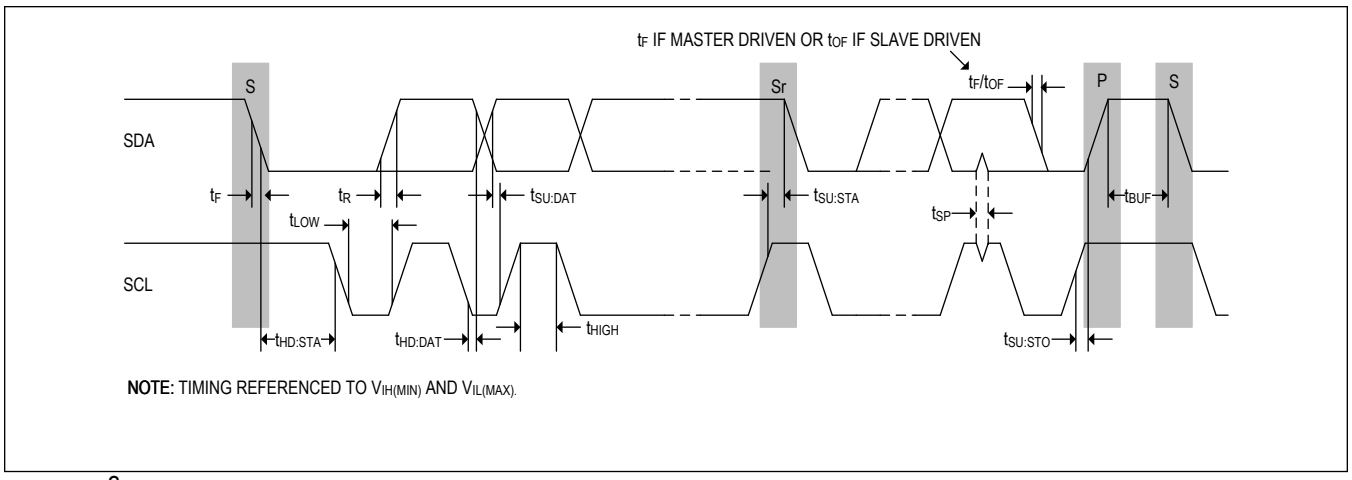


Figure 9. I²C Timing Diagram

Commands

Device Function Commands

The DS2485 has 15 commands with four memory commands, four configuration commands, seven 1-Wire master commands, and a CRC16 command. Table 2 lists these commands.

Table 2. Device Function Commands

COMMAND	CODE	DESCRIPTION	TYPE
Write Memory	96h	Write memory page	Memory
Read Memory	44h	Read memory page	Memory
Set Page Protection	C3h	Set page protection of a memory page	Memory
Read Status	AAh	Read the protection for a memory page	Memory
Set I2C Address	75h	Set the I2C address	Configuration
Read 1-Wire Port Config	52h	Read all or one port configuration registers	Configuration
Write 1-Wire Port Config	99h	Write to a 1-Wire port configuration register	Configuration
Master Reset	62h	Reset the 1-Wire master block and return to defaults	Configuration
1-Wire Script*	88h	Execute one or more 1-Wire primitive commands	1-Wire
1-Wire Block	ABh	Read and write 1-Wire data block (optional 1-Wire reset first and SPU at end)	1-Wire
1-Wire Read Block	50h	Read a block of 1-Wire data	1-Wire
1-Wire Write Block	68h	Write 1-Wire block of data (optional 1-Wire reset first and SPU at end)	1-Wire
1-Wire Search	11h	Perform 1-Wire search algorithm	1-Wire
Full Command Sequence	57h	Performs a complete 1-Wire authenticator communication sequence	1-Wire
Compute CRC16	CCh	Compute CRC16 over provided data	CRC16

**See Table 42 for the complete list of 1-Wire primitives including reset, read bit, write bit, read byte, and write byte, along with GPIO, 1-Wire speed, and pullup commands.*

I²C Communication Command Sequence

The generic command sequence is shown in Table 3. The write sequence begins with the master sending an I²C Start and write I²C address, then a command code from the listings in Table 5 is issued. Optionally, if the command requires it, a command parameter(s) and write data byte(s) might be sent followed by an I²C Stop. After the sequence writes, a delay might also be needed to allow the command process to complete.

Next, the read sequence begins by sending an I²C Start and read I²C address. The first byte read after the address is the length to set the number of data bytes to read. When receiving the read information, a Result Byte is provided that expresses if the sequence was successful (with an AAh) or if an error has occurred (with an unlike value). After the Result Byte, all the data can be read and should be followed by an I²C Stop.

Table 3. Generic I²C Command Sequence

<Start>
Tx: Master sends I²C address (WRITE)
Tx: Master sends Command Command
Tx: Master sends Write Length
Tx: Master sends Command Parameter(s)
Tx: Master sends Data Byte(s)
<Stop>
<Delay to allow command to complete>
<Start>
Tx: Master sends I²C address (READ)
Rx: Master receives Rx Read Length
Rx: Master receives Result Byte
Rx: Master receives Data Byte(s)
<Stop>

Table 4. Communication Legend

Tx <Start> <Stop>	Gray with white text denotes transmit, I²C start and stop
<Delay>	Orange with white text denotes delay waiting for completion of operation
Rx	Green denotes receiving data from DS2485

Write Memory (96h)

The Write Memory command is used to write a 32-byte page. The page can be any even-numbered user memory page (0 to 5). The page must not have WP protection (all odd-numbered pages have WP protection). If the page is protected, it fails with a 55h result byte. On success, the result byte is AAh. The 32-byte page data is provided after the parameter byte during the command sequence. All writes must be 32 bytes.

Table 5. Write Memory

Write Memory	
Command Code	96h
Parameter Byte(s)	See Table 6
Usage	A write is done by page number and always has a write size of 32 bytes.
Command Restrictions	Page must not have WP protection.
Device Operation	Verify that the destination page does not have WP protection set. Write the data. Set the result byte.
Command Duration	t_{WM}
Result Byte	AAh = Success 55h = The command failed because destination page is protected (WP). 77h = Invalid input or parameter

Table 6. Write Memory Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	PAGE#		

Bits 2:0: Memory Page Number (PAGE#). Page to write, 0 to 5 (odd values reference protected pages).

Table 7. Write Memory Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write Memory Command (96h)
Tx: Write Length Byte (33)
Tx: Parameter
Tx: Data to transmit (32 bytes)
<Stop>
<Delay t_{WM}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (1)
Rx: Result Byte
<Stop>

Read Memory (44h)

The Read Memory command is used to read a 32-byte page. The page can be any user memory page. All reads are the full 32 bytes. On success, the result byte is AAh. If an invalid page number is specified, 32 bytes of FFh are returned with a result byte of 77h. Odd-numbered pages return variable data with a result byte of AAh.

Table 8. Read Memory

Read Memory	
Command Code	44h
Parameter Byte(s)	Page number to read.
Usage	Read a page of memory. This function can also read the special purpose.
Command Restrictions	This command is applicable to user memory pages.
Device Operation	Read the data.
Command Duration	t_{RM}
Result Byte	AAh = Success 77h = Invalid input or parameter

Table 9. Read Memory Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	PAGE#		

Bits 2:0: Memory Page Number (PAGE#). These bits select the page number to be read. Acceptable values are User Page (Page 0 through Page 5).

Table 10. Read Memory Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Read Memory Command (44h)
Tx: Write Length Byte (1)
Tx: Parameter (page)
<Stop>
<Delay t_{RM}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (33)
Rx: Result Byte
Rx: Data (32 bytes)
<Stop>

Read Status (AAh)

Read the status of the protection settings of each of the six user pages, manufacturer ID (MANID), or device version.

Table 11. Read Status Command

Read Status	
Command Code	AAh
Parameter Byte(s)	See Table 12.
Usage	Read the page protection information for all pages Page 0 to Page 5 (6 bytes), MANID (2 bytes, MSB 1st), or device version (2 bytes).
Command Restrictions	None.
Device Operation	Read parameters. Read the page protection setting for all pages, MANID, or device version.
Command Duration	t_{RM}
Result Byte	AAh = Success 77h = Invalid parameter

Table 12. Read Status Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	OUTPUT_SELECT	

Bit 1:0: Output selection (OUTPUT_SELECT). (00b) return protection bytes of pages 0 to 5, 6 bytes; (01b) return MANID, 2 bytes; (10b) return device version, 2 bytes

Table 13. Read Status Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Read Status Command (AAh)
Tx: Write Length Byte (1)
Tx: Read Status parameter
<Stop>
<Delay t_{RM}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (7 or 3)
Rx: Result Byte
Rx: Result data [Protection Bytes (6 bytes), MANID (2 bytes, MSB 1st), or device version (2 bytes)]
<Stop>

Table 14. Read Status Page Protection Result for Each Page

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	NONE	0	0	0	WP	0

Bit 1: Write Protection (WP). (1b) permanently sets write protection; (0b) no write protection

Bit 5: None Protection (NONE). (1b) permanently sets no protection on page allowed and locks out any future attempts to add protection.

Set I2C Address (75h)

This command sets the I2C address. By default, the I2C address used is displayed in Figure 3. This command changes this default in a write-once event.

Table 15. Set I2C Address Command

Set I2C Address	
Command Code	75h
Parameter Byte(s)	New I2C address
Usage	Set the default I2C address.
Command Restrictions	Command can only be performed once.
Device Operation	Verify the I2C address has not been written. Write the default I2C address.
Command Duration	t_{WS}
Result Byte	AAh = Success 55h = Command failed because the I2C address has already been set.

Table 16. New I2C Address Parameter

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2C_ADDR							0

Bits 7:1: I2C Address (I2C_ADDR). I2C address parameter.

Table 17. Set I2C Address Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Set I2C Address Command (75h)
Tx: Write Length Byte (1)
Tx: New I2C Address
<Stop>
<Delay t_{WS}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (1)
Rx: Result Byte
<Stop>

Set Page Protection (C3h)

The Set Page Protection command sets the protection state of a single memory page. This is a one-time operation for each protection area. Attempting to set the protection of a page that is already protected (including all odd-numbered pages) results in an error 55h result byte. Attempting to set a protection combination on a protection area that is not valid results in a 77h error code. AAh is the result byte for a successful operation.

Table 18. Set Page Protection Command

Set Page Protection	
Command Code	C3h
Parameter Byte(s)	Two parameters. Byte 1: page to set protection. Byte 2: protection options.
Usage	Set protection. This is a one-time write of the page protection for each protection area. There are six protection areas: Page 0 to Page 5. All protection modes for the area needed must be set in one function call.
Command Restrictions	This command is applicable to pages that have not yet had protection set.
Device Operation	Verify that the destination page does not already have protection set. Verify that the protection requested is valid for the page. Write the protection.
Command Duration	t_{WS}
Result Byte	AAh = Success 77h = Invalid parameter 55h = Command failed because the protection for the page has already been set.

Table 19. Set Page Protection Parameter (Byte 1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	PAGE#		

Bits 3:0: Memory Page Number (PAGE#). These bits select the page number to be protected. Acceptable values are from Page 0 to Page 5, but odd-numbered pages are already protected.

Table 20. Set Page Protection Parameter (Byte 2)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	NONE	0	0	0	WP	0

Bit 1: Write Protection (WP). (1b) permanently sets write protection; (0b) no write protection

Bit 5: None Protection (NONE). (1b) permanently sets no protection on page allowed and locks out any future attempts to add protection.

Table 21. Set Page Protection Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Set Page Protection Command (C3h)
Tx: Write Length Byte (2)
Tx: Parameter (page)
Tx: Parameter (protection)
<Stop>
<Delay t_{WS}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (1)
Rx: Result Byte
<Stop>

Read 1-Wire Port Configuration (52h)

Read one or all of the 1-Wire port configuration settings.

Table 22. Read 1-Wire Port Configuration Command

Read 1-Wire Port Configuration	
Command Code	52h
Parameter Byte(s)	Register to read.
Usage	Read one or all configuration registers.
Command Restrictions	None.
Device Operation	Read configuration register(s). Set the result byte.
Command Duration	t_{OP}
Result Byte	AAh = Success

Table 23. 1-Wire Port Configuration Register Parameter

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REG							

Bits 7:0: Register (REG). Register number 0-13h; any value > 13h results in all registers read. If the value is 0-13h, then select the desired register from Table 24. The returned value is in the same format as the 1-Wire Write Port Config "1-Wire Master New Configuration Value."

Table 24. Port Configuration Registers

REGISTER #	CONFIGURATION REGISTER	DEFAULT
0h	Master Configuration	0000h
1h	Standard Speed t_{RSTL}	0006h
2h	Standard Speed t_{MSI}	0006h
3h	Standard Speed t_{MSP}	0006h
4h	Standard Speed t_{RSTH}	0006h
5h	Standard Speed t_{W0L}	0006h
6h	Standard Speed t_{W1L}	0006h
7h	Standard Speed t_{MSR}	0006h
8h	Standard Speed t_{REC}	0006h
9h	Overdrive Speed t_{RSTL}	0006h
Ah	Overdrive Speed t_{MSI}	0006h
Bh	Overdrive Speed t_{MSP}	0006h
Ch	Overdrive Speed t_{RSTH}	0006h
Dh	Overdrive Speed t_{W0L}	0006h
Eh	Overdrive Speed t_{W1L}	0006h
Fh	Overdrive Speed t_{MSR}	0006h
10h	Overdrive Speed t_{REC}	0006h
11h	RPUP/BUF	803Ch
12h	PDSLEW	0006h
13h	Reserved	5828h

Table 25. Read 1-Wire Port Configuration Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Read 1-Wire Port Configuration Command (52h)
Tx: Write Length Byte (1)
Tx: Parameter
<Stop>
<Delay t_{OP}>
<Start>
Tx: I2C address (READ)
Rx: Read Length Byte (3) or (41)
Rx: Result Byte
Rx: Register data (2 or 40 bytes)
<Stop>

Write 1-Wire Port Configuration (99h)

Write a 1-Wire port configuration register to change 1-Wire timing.

Table 26. Write 1-Wire Port Configuration Command

Write 1-Wire Port Configuration	
Command Code	99h
Parameter Byte(s)	Parameter indicating which register to set (1 byte) and the new value (2 byte, LSB first).
Usage	Write a 1-Wire configuration register.
Command Restrictions	If writing "custom timing" for 1-Wire timing, values shorter than the shortest predefined timings (Table 32 and Table 33) might not work as expected and can require adjusting RPUP and PDSLEW.
Device Operation	Verify the register. Write the register. Set the result byte.
Command Duration	t_{OP}
Result Byte	AAh = Success 77h = Invalid parameter

Table 27. 1-Wire Port Configuration Register Parameter

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	REG#				

Bits 5:0: Resister (REG#). Register number 0-13h. Select the desired register from Table 24.

Table 28. Port Configuration Registers

REGISTER #	CONFIGURATION REGISTER
0h	Master Configuration
1h	Standard Speed t_{RSTL}
2h	Standard Speed t_{MSI}
3h	Standard Speed t_{MSP}
4h	Standard Speed t_{RSTH}
5h	Standard Speed t_{W0L}
6h	Standard Speed t_{W1L}
7h	Standard Speed t_{MSR}
8h	Standard Speed t_{REC}
9h	Overdrive Speed t_{RSTL}
Ah	Overdrive Speed t_{MSI}
Bh	Overdrive Speed t_{MSP}
Ch	Overdrive Speed t_{RSTH}
Dh	Overdrive Speed t_{W0L}
Eh	Overdrive Speed t_{W1L}
Fh	Overdrive Speed t_{MSR}
10h	Overdrive Speed t_{REC}
11h	RPUP/BUF
12h	PDSLEW
13h	*Reserved

*Reserved must not be written to.

Table 29. 1-Wire Master Configuration Bit Assignment (Register 0)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
1WS	PDN	SPU	APU	X	X	X	X
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
X	X	X	X	X	X	X	X

Bit 12: Active Pullup (APU). The APU bit controls whether an active pullup (low-impedance transistor) or a passive pullup (RWPU resistor) is used to drive a 1-Wire line from low to high. When APU = 0, active pullup is disabled (resistor mode). Enabling active pullup is generally recommended for best 1-Wire performance. The active pullup does not apply to the rising edge of a recovery after a short on the 1 Wire line. (Default 0)

Bit 13: Strong Pullup (SPU). The SPU bit, when set to 1, is used to activate the strong pullup function prior to a 1-Wire Write Byte, 1-Wire Read Byte, or 1-Wire Write Bit, 1-Wire Read Bit command. When 0, the strong pullup function is disabled. (Default 0)

Bit 14: Power-Down (PDN). The PDN bit is used to remove power from the 1-Wire port, e.g., to force a 1-Wire slave to perform a power-on reset. The default state of PDN is 0, enabling normal operation. When PDN is changed to 1, no 1-Wire communication is possible. To end the 1-Wire power-down state, the PDN bit must be changed to 0. (Default 0)

Bit 15: 1-Wire Speed (1WS). The 1WS bit determines the timing of any 1-Wire communication generated by the master. Writing to the 1-Wire Master Configuration register with the 1WS bit as 0 sets the speed to standard speed (default). 1WS = 1 sets the speed to overdrive. (Default 0)

Table 30. 1-Wire Master New Configuration Value Bit Assignment (Registers 1 to 18)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
CUSTOM	X	VALUE[13:8]					
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
VALUE[7:0]							

Bits 13:0: Value Assignment (VALUE). Predefined register value 0–Fh or custom timing value.

Warning: When using custom timing values, 1-Wire communication failure can occur if the value chosen is outside the specification of the 1-Wire slave.

Bit 15: Custom Timing (CUSTOM). (1b) custom timing value used for the port configuration register in 62.5ns ticks times the value; (0b) predefined value used for the port configuration register (only the lower 4 bits of VALUE used). See Table 16 to Table 20 for the meaning of the predefined values for the selected register.

Table 31. Write 1-Wire Port Configuration Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write 1-Wire Port Configuration Command (99h)
Tx: Write Length Byte (3)
Tx: Register # Parameter (1)
Tx: 1-Wire Master New Configuration Value (2 bytes, LSB first)
<Stop>
<Delay t_{OP}>
<Start>
Tx: I2C address (READ)
Rx: Read Length Byte (1)
Rx: Result Byte
<Stop>

Table 32. Predefined Register Values for Standard Speed Timing

VALUE (h)	t_{RSTL} (µs)	t_{MSI} (µs)	t_{MSP} (µs)	t_{RSTH} (µs)	t_{W0L} (µs)	t_{W1L} (µs)	t_{MSR} (µs)	t_{REC} (µs)
0	440	3	58	440	52	1	5	0.5
1	460	3	60	460	56	3	7	1.5
2	480	3	62	480	60	5	9	2
3	500	5	64	500	62	6.5	10.5	3
4	520	6	66	520	64	7	11	4
5	540	7	67	540	66	7.5	11.5	5
6*	560	7.5	68	560	68	8	12	6
7	580	8	69	580	70	9	13	7.5
8	600	8.5	70	600	72	10	14	12
9	620	9	71	620	74	11	15	17.5
A	640	10	72	640	76	12	16	28.5
B	660	11	74	660	80	13	17	34
C	680	12	76	680	90	14	18	45
D	720	13	78	700	100	15	19	56.5
E	800	14	80	720	110	15.5	19.5	112
F	960	15	82	740	120	16	20	223

*Default

Table 33. Predefined Register Values for Overdrive Speed Timing

VALUE (h)	t_{RSTL} (µs)	t_{MSI} (µs)	t_{MSP} (µs)	t_{RSTH} (µs)	t_{W0L} (µs)	t_{W1L} (µs)	t_{MSR} (µs)	t_{REC} (µs)
0	44	0.75	5	44	5	0.0625	1	0.5
1	46	0.75	5.5	46	5.5	0.125	1.125	1.5
2	48	0.75	6	48	6	0.25	1.25	2
3	50	0.75	6.5	50	6.5	0.375	1.375	3
4	52	1	7	52	7	0.5	1.5	4
5	54	1.25	7.5	54	7.5	0.625	1.625	5
6*	56	1.5	8	56	8	0.75	1.75	6
7	58	1.625	8.5	58	8.5	0.875	1.875	7.5
8	60	1.75	9	60	9	1	2	12
9	62	1.875	9.5	62	9.5	1.125	2.125	17.5
A	64	2	10	64	10	1.25	2.25	28.5
B	66	2.125	10.5	66	11	1.375	2.375	34
C	68	2.25	11	68	12	1.5	2.5	45
D	72	2.375	12	70	13	1.625	2.625	56.5
E	74	2.5	13	72	14	1.75	2.75	112
F	80	2.625	14	74	15.5	1.875	2.875	223

*Default

Table 34. Predefined Register Values for RWPU and VTH/VIAPO

RPUP/BUF (h)*	VTH	VIAPO	RWPU (Ω)
0	Medium	Low	333
1	Medium	Medium	333
2	High	High	333
3	Medium	Low	500
4	Medium	Medium	500
5	High	High	500
6	Medium	Low	1000
7	Low	Low	1000
8	High	Medium	1000
9	Medium	Medium	1000
A	High	High	1000
B	Medium	Low	External
C	Low	Low	External
D	High	Medium	External
E	Medium	Medium	External
F	High	High	External

*Upon power-up, the default setting is per Table 30. Set for correct 1-Wire operation.

For most applications with only one slave device, the recommendation is to set RPUP/BUF to 6h.

Table 35. Predefined Register Values for PDSLEW

PDSLEW (h)	STANDARD SLEW (ns)**	OVERDRIVE SLEW (ns)**
0	50	50
1	50	50
2	50	150
3	50	150
4	150	50
5	150	50
6*	150	50
7	150	150
8	150	150
9	150	150
A	1300	50
B	1300	50
C	1300	150
D	1300	150
E	1300	150
F	1300	1300 (do not use)

*Default

**Typical values

Table 36. Custom Timing Maximum Values Allowed

REGISTERS # (h)	CONFIGURATION REGISTER	MAXIMUM TIME ALLOWED (µs)
1	Standard Speed t_{RSTL}	1020
2	Standard Speed t_{MSI}	15.5
3	Standard Speed t_{MSP}	127
4	Standard Speed t_{RSTH}	1020
5	Standard Speed t_{W0L}	126
6	Standard Speed t_{W1L}	31.5
7	Standard Speed t_{MSR}	31.5
8	Standard Speed t_{REC}	255.5
9	Overdrive Speed t_{RSTL}	126
A	Overdrive Speed t_{MSI}	3.875
B	Overdrive Speed t_{MSP}	15.5
C	Overdrive Speed t_{RSTH}	126
D	Overdrive Speed t_{W0L}	31.5
E	Overdrive Speed t_{W1L}	1.9375
F	Overdrive Speed t_{MSR}	3.875
10	Overdrive Speed t_{REC}	255.5

Table 37. Custom Settings for RPUP/BUF Register

PARAMETER	CUSTOM	VALUE				DESCRIPTION
	(15)	(14:6)	(5:4)	(3:2)	(1:0)	
RWPU	1	0	X	X	00b	Ext
	1	0	X	X	01b	500
	1	0	X	X	10b	1000
	1	0	X	X	11b	333
VIAPO (active pullup buffer)	1	0	X	00b	X	Low
	1	0	X	01b	X	Medium
	1	0	X	10b	X	High
	1	0	X	11b	X	Off
VTH (data input buffer)	1	0	00b	X	X	Low (0.2V, no hysteresis)
	1	0	01b	X	X	Medium (0.4V, no hysteresis)
	1	0	10b	X	X	High (0.7V, with hysteresis)
	1	0	11b	X	X	Off
*Default	1	0	11b	11b	00b	Custom, Off, Off, Ext. (803Ch)

*This is the "float condition." After power-up, this setting must be changed for correct 1-Wire operation. Additionally, a 1-Wire reset must be performed. This can be accomplished with the 1-Wire Command (1-Wire Reset). Furthermore, the float condition can be re-entered by setting this register back to 803Ch.

Table 38. Custom Timing Values for PDSLEW Register

PARAMETER*	CUSTOM (15)	VALUE (14:6)	VALUE (5:3)	VALUE (2:0)	NOMINAL t_F (ns)**
Overdrive Slew	1	0	X	001b	50
	1	0	X	010b	150
	1	0	X	100b	1300 (do not use)
Standard Slew	1	0	001b	X	50
	1	0	010b	X	150
	1	0	100b	X	1300

*Do not use other bit values for the slew settings.

**Typical values

Master Reset (62h)

Reset the 1-Wire master.

Table 39. Master Reset Command

Master Reset	
Command Code	62h
Parameter Byte(s)	None
Usage	Reset the 1-Wire master and return all configuration registers to the default values.
Command Restrictions	None
Device Operation	Reset 1-Wire master to power-on reset. Set result byte.
Command Duration	t_{OP}
Result Byte	AAh = Success 22h = Master reset fail

Table 40. Master Reset Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Master Reset Command (62h)
<Stop>
<Delay t_{OP}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (1)
Rx: Result Byte
<Stop>

1-Wire Script (88h)

Execute one or more 1-Wire primitive commands and return results.

Table 41. 1-Wire Script Command

1-Write Script	
Command Code	88h
Parameter Byte(s)	Parameter indicating one or more primitive 1-Wire commands. If the command requires data, this is also a parameter.
Usage	1-Wire primitive communication command
Command Restrictions	Input script and result size limited to 126 bytes
Device Operation	Sequence through each primitive command and construct the result buffer.
Command Duration	t_{OP} + t_{SEQ} x Commands + "1-Wire time"
Result Byte	AAh = Success 77h = Invalid parameter 22h = Communication failure, script stopped

Table 42. 1-Wire Primitive Commands

COMMAND NAME	COMMAND FORMAT (hex)	RESPONSE FORMAT (hex)	COMMAND DESCRIPTION
OW_RESET	00, RP	00, ST	Perform 1-Wire reset with optional verification of result. RP – 1-Wire Reset Parameter ST – 1-Wire Master Status Result If IGNORE = 0 and presence not detected, stop script with 22h result code.
OW_WRITE_BIT	01, WB	01, ST	Write 1-Wire bit. WB – 1-Wire Write Bit Parameter ST – 1-Wire Master Status Result
OW_READ_BIT	02	02, ST	Read 1-Wire bit. ST – 1-Wire Master Status Result
OW_WRITE_BYTE	03, TX	03, RX	Write 1-Wire byte. TX – Byte to write RX – Response byte result. Under normal conditions for a 1-Wire write byte, RX should equal TX.
OW_READ_BYTE	04	04, RX	Read 1-Wire byte. RX – 1-Wire read byte result.
OW_TRIPLET	05, TP	05, ST	1-Wire search triplet, used for custom 1-Wire Search algorithms TP – 1-Wire Triplet Parameter ST – 1-Wire Master Status Result
OW_OV_SKIP*	06	06, ST	1-Wire Overdrive Skip ROM sequence ST – 1-Wire Master Status Result
OW_SKIP	07	07, ST	1-Wire Skip ROM sequence (standard speed reset, presence detect) ST – 1-Wire Master Status Result
OW_READ_BLOCK	08, NN	08, NN, XX, …	Read 1-Wire bytes. NN – Length indicates the number of bytes to read. XX – 1-Wire Bytes read
OW_WRITE_BLOCK	09, NN, XX, …	09, RR	Send the following hex byte values to the 1-Wire bus and sample the result. Verify that the result sample matches what was sent. RR – Result flag indicates if the sample result matches what was sent AA or does not match FF.

Table 42. 1-Wire Primitive Commands (continued)

DELAY	0A, LL	--	Delay for LL milliseconds, no response byte
PRIME_SPU	0B	--	Prime 1-Wire power delivery (strong pullup) to occur after the next 1-Wire byte (read or write) or 1-Wire bit (read or write), no response byte
SPU_OFF	0C	--	Restore normal pullup, no response byte
SPEED	0D, RP	--	Change the 1-Wire speed. RP – 1-Wire Reset Parameter
VERIFY_TOGGLE	0E	0E, RR	Verify 1-Wire toggle response. Read a byte from the 1-Wire and verify that the 1-Wire is toggling. Ignores the first bit. RR – Result flag. AA indicates toggle, FF indicates that there was no toggle. The 1-Wire script processing will stop with result code 22h if the toggle is not detected.
VERIFY_BYTE	0F, RX	0F, RR	Read a 1-Wire byte and verify that it matches the RX parameter. RX – Byte value to verify RR – Result flag. AA if they match, FF if they did not. If it does not match, then stop the script with result code 22h.
CRC16_START	10	--	Start the CRC16 calculation by first setting the CRC16 to all zeros. All following 1-Wire bytes will be included in the calculation until the CRC16_VERIFY command is found. No response byte. In the case of OW_WRITE_BYTE and OW_WRITE_BLOCK, the value of the bytes transmitted is used in the calculation.
VERIFY_CRC16	11, VALUE	11, RR	Check the CRC16 calculated value to make sure it equals the provided hex "VALUE." VALUE – 2-byte hex number (LS byte, MS byte). RR – Result flag. AA if it matches, FF if it does not match. The 1-Wire script processing will stop with result code 22h if the check fails.
SET_GPIO	12, PIOAC	12, PIOAL	Set GPIO to conducting state. PIOAC – (AAh) set to conducting; (55h) set to non-conducting high impedance state; (A5h) set to conducting, no level read; (5Ah) set to non-conducting, no read PIOAL – (AAh) level detection low; (55h) level detection is high; (FFh) level cannot be read because of PIOAC state
READ_GPIO	13	13, PIOAL	Read GPIO level. PIOAL – (AAh) level detection low, (55h) level detection is high, (FFh) level cannot be read because of PIOAC state
VERIFY_GPIO	14, PIOAL	14, RR	Verify GPIO level. PIOAL – (AAh) verify level detection low, (55h) verify level detection is high RR – Result flag If the level does not match the PIOAL state, the script will stop with result code 22h.
CONFIG_RPUP_BUF	15, RPUP	--	Set the RPUP/BUF Configuration register. The default "float condition" can be entered by setting to 8030Ch. No response byte. RPUP – 2-byte hex number (LS byte, MS byte)
FAIL	--	1BBBBBBBb	Script failure. Failure code is BBBBBBBb. The script terminates and returns result code 22h. 0000000 – Unknown command 0000001 – Out of room in buffer

*Overdrive Skip ROM sequence:

1. Standard speed reset
2. Standard speed presence detected (if no presence, clear 1-Wire Master Status [RST] and return "Master Reset fail")
3. Transmit Overdrive Skip Command (3Ch)

4. 2ms delay
5. Overdrive speed reset
6. Overdrive speed presence detect
7. Update 1-Wire Master Status [RST] and return success

Table 43. 1-Wire Reset Parameter (RP)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1WS_INV	0	0	0	1WS	0	IGNORE	0

Bit 7: 1-Wire Speed Inverted (1WS_INV). Same as bit 3, but inverted.

Bit 3: 1-Wire Speed (1WS). The 1WS bit determines the timing of any 1-Wire communication generated by the master. Writing to the 1-Wire Master Configuration register with the 1WS bit as 0 sets the speed to standard speed (default). 1WS = 1 sets the speed to overdrive. (Note this is just the 1WS portion of the 1-Wire Master Configuration.)

Bit 1: Ignore Presence (IGNORE). 1b to ignore the presence result when continuing to process the script. 0b to verify that the presence pulse is detected. If not detected, then stop the script.

Table 44. 1-Wire Write Bit Parameter (WB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	BIT_VALUE

Bit 0: Bit Value (BIT_VALUE). Bit value to write.

Table 45. 1-Wire Write Byte Parameter (TX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BYTE_VALUE							

Bits 7:0: Byte Value (BYTE_VALUE). Byte value to write.

Table 46. 1-Wire Triplet Parameter (TP)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	T_VALUE

Bit 0: 1-Wire Triplet Branch Direction (T_VALUE). This bit specifies the branch direction to be taken if both the first and the second read time slot read a 0. (0b) a write-zero time slot is generated; (1b) a write-one time slot is generated.

Table 47. 1-Wire Script Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write 1-Wire Script Command (88h)
Tx: Write Length Byte (variable, at least 1)
Tx: 1-Wire Primitive commands and parameters (variable)
<Stop>
<Delay t_{OP} + t_{SEQ} x Commands + "1-Wire time">
<Start>
Tx: I2C address (READ)
Rx: Length Byte (variable, at least 1)
Rx: Result Byte
Rx: Response data (variable)
<Stop>

Table 48. 1-Wire Master Status Result (ST)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR	TSB	SBR	1WSS	LL	SD	PPD	IGNORES

Bit 7: Branch Direction Taken (DIR). When a 1-Wire Triplet command is executed, this bit reports to the host processor the search direction that was chosen by the third bit of the triplet. The power-on default of DIR is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands. For additional information, see the description of the 1-Wire Triplet command and *Application Note 187: 1-Wire Search Algorithm*.

Bit 6: Triplet Second Bit (TSB). The TSB bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of the second bit of a 1-Wire Triplet command. The power-on default of TSB is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands.

Bit 5: Single-Bit Result (SBR). The SBR bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of a 1-Wire Read/Write Bit command or the first bit of a 1-Wire Triplet command. The power-on default of SBR is 0. If the 1-Wire Write Bit command sends a 0 bit, SBR should be 0. With a 1-Wire Triplet command, SBR could be 0 as well as 1, depending on the response of the 1-Wire devices connected. The same result applies to a 1-Wire Read Bit command that sends a 1 bit, as it could be 0 as well as 1.

Bit 4: 1-Wire Speed Status (1WSS). The 1WSS bit is read-only and reports the timing of any 1-Wire communication generated by the master. 1WS = 0 standard speed, 1WS = 1 overdrive speed.

Bit 3: Logic Level (LL). The LL bit is a read only value that reports the logic state of the active 1-Wire line without initiating any 1-Wire communication. The 1 Wire line is sampled for this purpose every time the 1-Wire Master Status register is read. The sampling and updating of the LL bit takes place when the host processor has addressed the DS2485 in read mode (during the acknowledge cycle), provided that the read pointer is positioned at the 1-Wire Master Status register.

Bit 2: Short Detected (SD). The SD bit is updated with every 1-Wire Reset command. If the DS2485 detects a logic 0 on the 1-Wire line at t_{MSI} during the presence-detect cycle, the SD bit is set to 1. This bit returns to its default 0 with a subsequent 1-Wire Reset command provided that the short has been removed.

Bit 1: Presence-Pulse Detect (PPD). The PPD bit is updated with every 1-Wire Reset command. If the DS2485 detects a presence pulse from a 1-Wire device at t_{MSP} during the presence-detect cycle, the PPD bit is set to 1. This bit returns to its default 0 if there is no presence pulse or if the 1-Wire line is shorted during a subsequent 1-Wire Reset command.

Bit 0: Ignore Presence Status (IGNORES). This IGNORES bit is read-only and indicates what value was set in the 1-Wire Reset Parameter (RP) bit IGNORE. 0b to verify that the presence pulse is detected, 1b to not verify the presence pulse detect.

Table 49. 1-Wire Byte Result (RX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BYTE_VALUE							

Bits 7:0: Byte Value Result (BYTE_VALUE). Byte value read.

1-Wire Block (ABh)

Perform a mixture of read and write 1-Wire data block. Read bytes in the input block must be FFh. Optionally, reset 1-Wire first.

Table 50. 1-Wire Block

1-Wire Block	
Command Code	ABh
Parameter Byte(s)	Parameter indicating optional 1-Wire reset
Usage	1-Wire block
Command Restrictions	None
Device Operation	Optional: 1-Wire reset. Transmit 1-Wire data, read the results. Optional: SPU enable. Optional: GPIO conducting enable on AAh success. Disable SPU if the result is not AAh success. Set result byte.
Command Duration	t_{OP} + t_{SEQ} x (data bytes + OW_RST) + "1-Wire time"
Result Byte	AAh = Success 77h = Invalid parameter 22h = Communication failure 33h = 1-Wire presence pulse not detected

Table 51. 1-Wire Block Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	PE	SPU	IGNORE	OW_RST

Bit 0: 1-Wire Reset (OW_RST). (1b) transmit a 1-Wire reset before the block and verify presence pulse—if presence is not detected and IGNORE = 0b then stop operation; (0b) no 1-Wire reset

Bit 1: Ignore Presence Pulse (IGNORE). (1b) ignore the presence pulse result from OW_RST; (0b) do not ignore presence on optional 1-Wire reset.

Bit 2: Strong Pullup (SPU). (1b) enable SPU at the end of the block (must be manually turned off through the 1-Wire Master Configuration register); (0b) do not enable SPU at the end of the block.

Bit 3: P-Channel Enable (PE). (1b) enable GPIO to conduction state at the end of a successful block—this occurs within 10µs of the strong pullup activation, allowing an external P-channel MOSFET to be used as strong pullup (must be manually turned off through the 1-Wire Master Configuration register); (0b) do not change the GPIO state.

Table 52. 1-Wire Block Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write 1-Wire Block Command (ABh)
Tx: Write Length Byte (variable)
Tx: Parameter
Tx: Data to transmit (0 to 126 bytes)
<Stop>
<Delay t_{OP} + t_{SEQ} x (data bytes + OW_RST) + "1-Wire time">
<Start>
Tx: I2C address (READ)
Rx: Length Byte (variable)
Rx: Result Byte
Rx: 1-Wire Data (1 to 126 bytes)
<Stop>

1-Wire Write Block (68h)

Write 1-Wire block of data with optional 1-Wire reset first. The readback of each 1-Write byte written is verified. An error code indicates if the readback did not match the byte written.

Table 53. 1-Wire Write Block

1-Wire Write Block	
Command Code	68h
Parameter Byte(s)	Parameter indicating optional 1-Wire reset
Usage	1-Wire write block
Command Restrictions	None
Device Operation	Optional: 1-Wire reset. Transmit 1-Wire data. Optional: SPU on last byte of block. Set result byte.
Command Duration	t_{OP} + t_{SEQ} x (write bytes + OW_RST) + "1-Wire time"
Result Byte	AAh = Success 22h = Communication failure 33h = 1-Wire presence pulse not detected 00h = Non-matching 1-Wire writes 77h = Invalid parameter

Table 54. 1-Wire Write Block Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	SPU	IGNORE	OW_RST

Bit 0: 1-Wire Reset (OW_RST): (1b) transmit a 1-Wire reset before the block and verify presence pulse—if presence is not detected and IGNORE = 0b then stop operation; (0b) no 1-Wire reset.

Bit 1: Ignore Presence Pulse (IGNORE). (1b) ignore the presence pulse result from OW_RST; (0b) do not ignore presence on optional 1-Wire reset.

Bit 2: Strong Pullup (SPU). (1b) enable SPU at the end of the block (must be manually turned off through the 1-Wire Master Configuration register); (0b) do not enable SPU at the end of the block.

Table 55. 1-Wire Write Block Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write 1-Wire Write Block Command (68h)
Tx: Write Length Byte (variable)
Tx: Parameter
Tx: Data to transmit (0 to 126 bytes)
<Stop>
<Delay t_{OP} + t_{SEQ} x (write bytes + OW_RST) + "1-Wire time">
<Start>
Tx: I2C address (READ)
Rx: Length Byte (1)
Rx: Result Byte
<Stop>

1-Wire Read Block (50h)

Read a block of 1-Wire data.

Table 56. 1-Wire Read Block

1-Wire Read Block	
Command Code	50h
Parameter Byte(s)	Parameter indicating the number of bytes to read (max 126)
Usage	1-Wire read block
Command Restrictions	None
Device Operation	Read 1-Wire bus READ_LEN bytes. Set result byte.
Command Duration	t_{OP} + t_{SEQ} x read bytes + "1-Wire time"
Result Byte	AAh = Success 77h = Invalid parameter 22h = Communication failure

Table 57. 1-Wire Write Block Parameter Byte

BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
READ_LEN							

Bit 7:0: Read Length (READ_LEN): Number of bytes to read from 1-Wire (standard or overdrive depending on state).

Table 58. 1-Wire Read Block Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write 1-Wire Block Command (50h)
Tx: Write Length Byte (1)
Tx: Parameter Byte Length
<Stop>
<Delay t_{OP} + t_{SEQ} x read bytes + "1-Wire time">
<Start>
Tx: I2C address (READ)
Rx: Length Byte (variable)
Rx: Result Byte
Rx: 1-Wire Data (1 to 126 bytes)
<Stop>

1-Wire Search (11h)

Perform 1-Wire Search algorithm and return one device ROMID.

Table 59. 1-Wire Search

1-Wire Search	
Command Code	11h
Parameter Byte(s)	Parameter to indicate if the search is being reset. Optionally, perform a 1-Wire Reset pulse prior to the search command. Parameter also provides the command code to use for the search sequence.
Usage	1-Wire search
Command Restrictions	Repeated calls to 1-Wire Search results in finding the next device on the 1-Wire using the search algorithm. The 1-Wire Search functions must be called without other DS2485 command calls in between to keep the search state.
Device Operation	Optionally, reset search status. Optionally, perform 1-Wire Reset. Transmit 1-Wire Search command. Complete search, return ROMID. Set result byte. If the last device, set the last device flag to true; otherwise the last device flag is set false.
Command Duration	t_{OP} + t_{SEQ} x (64 + OW_RST) + "1-Wire time"
Result Byte	AAh = Success 33h = 1-Wire presence pulse not detected 00h = Device not detected in search 77h = Invalid parameter

Table 60. 1-Wire Search Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	SEARCH_RST	IGNORE	OW_RST

Bit 0: 1-Wire Reset (OW_RST). (1b) transmit a 1-Wire reset before the block and verify presence pulse—if presence is not detected, and IGNORE = 0b then stop operation; (0b) no 1-Wire reset.

Bit 1: Ignore Presence Pulse (IGNORE). (1b) ignore the presence pulse result from OW_RST; (0b) do not ignore presence on optional 1-Wire reset.

Bit 2: Search Reset (SEARCH_RST). (1b) reset the search state to find the "first" device ROMID; (0b) do not reset the search state, find the "next" device ROMID.

Table 61. 1-Wire Search Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write 1-Wire Search Command (11h)
Tx: Write Length Byte (2)
Tx: Parameter
Tx: Search Command code for device (usually F0h)
<Stop>
<Delay t_{OP} + t_{SEQ} x (64 + OW_RST) + "1-Wire time">
<Start>
Tx: I2C address (READ)
Rx: Length Byte (10 on success, 1 on failure)
Rx: Result Byte
Rx: (optional on success) 8-byte ROMID
Rx: (optional on success) last device flag
<Stop>

Table 62. 1-Wire Search Last Device Result

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	LAST_DEV

Bit 0: Last Device Flag (LAST_DEV): (1b) indicates that the ROMID returned is the last device in the search on the 1-Wire bus; (0b) indicates more devices are on the 1-Wire bus, additional calls to 1-Wire Search with SEARCH_RST = 0 result in the "NEXT" device.

Full Command Sequence (57h)

Perform a standard "Command Start" 1-Wire command sequence at the selected speed, strong pullup delay, and read result. The CRC16 from the slave is verified before the release byte is sent and on read result.

Table 63. Full Command Sequence

Full Command Sequence	
Command Code	57h
Parameter Byte(s)	Parameter indicating delay for slave during sequence. 8-byte parameter for ROMID to be used to select the slave with MATCH ROM. Data payload to send for slave command and parameters.
Usage	Perform a full standard sequence for slave devices with the "Command Start" 66h command.
Command Restrictions	None
Device Operation	TX: 1-Wire Reset (ignore presence) TX: Match ROM TX: ROMID TX: Command Start 66h TX: Length of OW_DATA TX: OW_DATA RX: CRC16 (verify) TX: Release Byte AAh with SPU Delay (OW_CMD_DELAY × 2ms) RX: Dummy RX: Result Length (OW_RSLT_LEN) RX: Result Data (OW_RSLT_DATA) RX: CRC16 (verify) Set result byte and values
Command Duration	t_{OP} + t_{SEQ} x (17 + length of OW_DATA + OW_RSLT_LEN) + "1-Wire time" + OW_CMD_DELAY × 2ms
Result Byte	AAh = Success 00h = CRC16 incorrect

Table 64. Full Command Sequence Parameter Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OW_CMD_DELAY							

Bit 7:0: 1-Wire Command Delay (OW_CMD_DELAY). Delay for strong pullup during standard command sequence in increments of 2ms.

Table 65. Full Command Sequence Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Write Full Command Sequence Command (57h)
Tx: Write Length Byte (variable)
Tx: Parameter - Delay
Tx: ROMID (8 bytes)
Tx: 1-Wire data for sequence OW_DATA (1 to 116 bytes)
<Stop>
<Delay t_{OP} + t_{SEQ} x (17 + length of OW_DATA + OW_RSLT_LEN) + "1-Wire time" + OW_CMD_DELAY × 2ms>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (variable)
Rx: Result Byte
Rx: 1-Wire Result Length (OW_RSLT_LEN)
Rx: 1-Wire Result Data (OW_RSLT_DATA) (1 to 124 bytes)
<Stop>

Table 66. 1-Wire Communication Generated from Full Command Sequence

1-Wire Reset
Presence Pulse (ignore)
Tx: MATCH ROM Command (55h)
Tx: ROMID (8 bytes)
Tx: Command Start (66h)
Tx: Length Byte (variable)
Tx: OW_DATA (1 to 116 bytes)
Rx: CRC16 (inverted of command start, length, parameter, and command)
Tx: Release Byte
<Delay OW_CMD_DELAY × 2ms>
Rx: Dummy Byte
Rx: Length (variable) - OW_RSLT_LEN
Rx: Result Byte - OW_RSULT_DATA
Rx: CRC16 (inverted, OW_RSLT_LEN, OW_RSLT_DATA)

Compute CRC16 (CCh)

Compute CRC16 on provided data (1 to 126 bytes).

Table 67. Compute CRC16 Command

Compute CRC16	
Command Code	CCh
Parameter Byte(s)	Data
Usage	Compute CRC16 on provided data (1 to 126 bytes)
Command Restrictions	None.
Device Operation	Verify there is at least 1 byte of data. Compute CRC16 over data. Set result byte and return inverted CRC16.
Command Duration	t_{OP}
Result Byte	AAh = Success 77h = Invalid length of data (0) FFh = Length byte does not match actual length of data. (Rx Length Byte will be 0.)

Table 68. Compute CRC16 Command Communication Sequence

<Start>
Tx: I2C address (WRITE)
Tx: Compute CRC16 Command (CCh)
Tx: Write Length Byte (variable)
Tx: Data to compute CRC16 (1 to 126 bytes)
<Stop>
<Delay t_{OP}>
<Start>
Tx: I2C address (READ)
Rx: Length Byte (0 to 3)
Rx: Result Byte
Rx: CRC16 (2 bytes)
<Stop>

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2485Q+T	-40°C to +85°C	6 TDFN (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/21	Initial release	—