Click here to ask about the production status of specific part numbers.

MAX20404/MAX20405/ MAX20406

Automotive 36V, 4A/5A/6A Fully Integrated Synchronous Buck Converter

General Description

The MAX20404/MAX20405/MAX20406 ICs are tiny synchronous buck converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 6A with wide input voltages range from 3V to 36V. Voltage quality can be monitored by observing the PGOOD signal. The MAX20404/MAX20405/MAX20406 can operate in dropout by running at 99% duty cycle, making it ideal for automotive and industrial applications.

The MAX20404/MAX20405/MAX20406 offers programmable or fixed output voltages of 5V and 3.3V. Frequency is internally fixed at 2.1MHz (or 400KHz or 3MHz) which allows for small external components, reduced output ripple, and guarantees no AM interference. MAX20404/5/6 automatically enters skip mode at light loads with ultra-low quiescent current of 10µA at no load. This family of products (including MAX20408/10) offers a pin-to-pin compatible offering from 4A to 10A in a single-phase configuration, and up to 20A in a dual-phase configuration. This device has also been optimized for dual-phase operation with very high current sharing accuracy. The devices can be ordered with spread-spectrum frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX20404/MAX20405/MAX20406 is available in a small 3.5mm x 3.75mm 17-pin FC2QFN package and uses very few external components.

Applications

- Automotive
  - Infotainment systems
  - ADAS and other safety critical applications
- Industrial
- High-Voltage DC-DC Converters

Benefits and Features

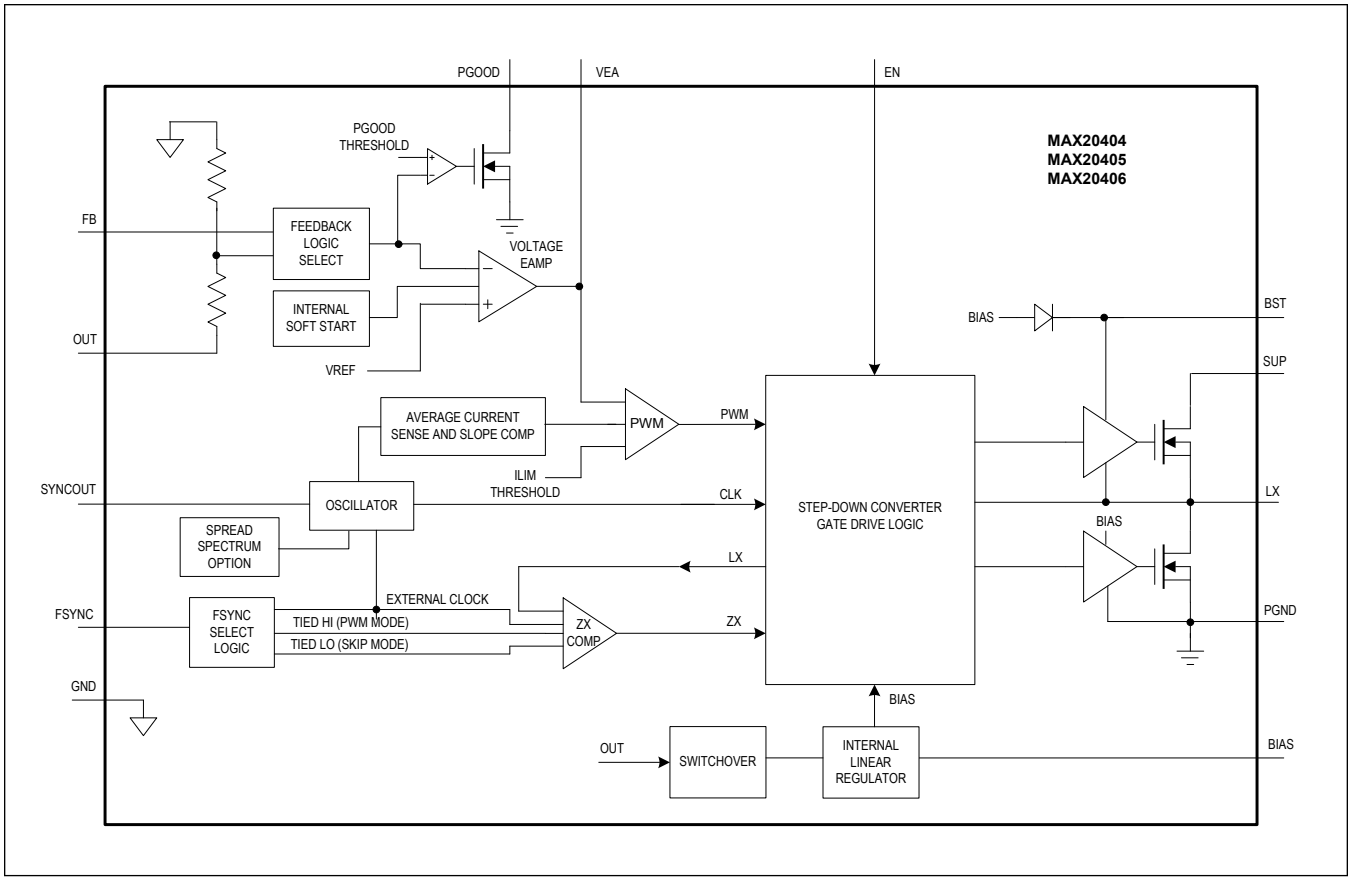
- Multiple Functions for Small Size
  - Operating V_{IN} Range of 3V to 36V
  - 10µA Quiescent Current in Skip Mode
  - Synchronous DC-DC Converter with Integrated FETs
  - 400kHz, 2.1MHz, and 3MHz Fixed-Frequency Options
  - Fixed 2.5ms Internal Soft-Start
  - Programmable 0.8V to 10V Output, or 3.3V and 5.0V Fixed-Output Options Available
  - 3.5mm x 3.75mm 17-Pin FC2QFN
  - Symmetrical Package Offers Superior EMI Performance
- Dual-Phase Capability
  - Can Be Used in Dual-Phase Configuration for High-Power Design
  - Dynamic Current Sharing via Shared VEA Pin
  - Low-Iq Operation Capability in Dual Phase
- High Precision
  - ±1% Output-Voltage Accuracy in FPWM Mode at No Load
  - Precise Output Voltage Monitoring with PGOOD
- Robust for the Automotive Environment
  - Forced-PWM and Skip-Mode Operation
  - 99% Duty-Cycle Operation with Low Dropout
  - Overtemperature and Short-Circuit Protection
  - -40°C to +125°C Operating Temperature Range
  - 42V Load-Dump Tolerant
  - AEC-Q100 Qualified

Ordering Information appears at end of data sheet.

19-100996; Rev 0; 2/21

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

SUP ..... -0.3V to +42V
EN..... -0.3V to +42V
BST to LX ..... -0.3V to 2.2V
BST..... -0.3V to 44V
LX ..... -0.3V to SUP+0.3V
SYNCOUT ..... -0.3V to 6V
SYNC..... -0.3V to 6V
VEA ..... -0.3V to BIAS+0.3V
FB ..... -0.3V to BIAS+0.3V
OUT ..... -0.3V to 16V
PGOOD ..... -0.3V to 6V
BIAS..... -0.3V to +2.2V
PGND to AGND ..... -0.3V to +0.3V
LX Continuous RMS current 6A
ESD Protection
Human Body Model.....±2kV
Charged Device Model.....±750V
Continuous Power Dissipation (T_A = +70°C, derate 34.48 mW/°C above +70°C.).....2758mW
Operating Temperature Range .....-40°C to 150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (Soldering 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to 125	ºC

Note: These limits are not guaranteed.

Package Information

FC2QFN

Package Code	F173A3FY+6
Outline Number	21-100343
Land Pattern Number	90-100129
THERMAL RESISTANCE, FOUR-LAYER EVKIT BOARD	
Junction-to-Ambient (θ_{JA})	29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	10.51°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the Evaluation Kit, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150 °C, unless otherwise noted. Typical values are at T_A = 25 °C under normal conditions unless otherwise noted. Note 1 and Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3		36	V
Supply Current	I_{SUP_SHDN}	V_{EN} = 0, T_A = 25°C		4	6	µA
	I_{SUP}	V_{EN} = High, V_{OUT} = 3.3V, V_{FB} = V_{BIAS}, no load, no switching, T_A = 25°C		10		

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150 °C, unless otherwise noted. Typical values are at T_A = 25 °C under normal conditions unless otherwise noted. Note 1 and Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUP Undervoltage Lockout	$V_{SUP_UVLO_RISE}$	SUP voltage rising	2.945	3.025	3.175	V
	$V_{SUP_UVLO_FALL}$	SUP voltage falling	2.655	2.725	2.870	
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	BIAS voltage falling	1.53	1.58	1.63	V
BIAS Undervoltage Lock	$V_{BIAS_UVLO_HYS}$	BIAS UVLO hysteresis		50		mV
BIAS Voltage	V_{BIAS}			1.8		V
BUCK CONVERTER						
Output Voltage Accuracy	$V_{OUT_SKIP_5V}$	V_{OUT} = 5V, skip mode, no load	4.93	5.0	5.05	V
	$V_{OUT_PWM_5V}$	V_{OUT} = 5V, PWM mode, no load	4.95	5.0	5.05	
	$V_{OUT_SKIP_3.3V}$	V_{OUT} = 3.3V, skip mode, no load	3.245	3.3	3.335	
	$V_{OUT_PWM_3.3V}$	V_{OUT} = 3.3V, PWM mode, no load	3.265	3.3	3.335	
Output Voltage Adjustable Range	V_{OUT}		0.8		10	V
Feedback Voltage Accuracy	V_{FB_PWM}	PWM mode, no load	0.787	0.800	0.813	V
Feedback Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = 25°C			100	nA
High-Side DMOS On-Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 2A		45	90	mΩ
Low-Side DMOS On-Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 2A		22	44	mΩ
High-Side DMOS Current-Limit Threshold	I_{LIM}	MAX20404	5.50	6.25	7.00	A
		MAX20405	6.5	7.5	8.5	
		MAX20406	7.5	8.75	10	
Low-Side DMOS Negative Current-Limit Threshold	I_{NEG}	MAX20404		-2.3		A
		MAX20405		-3		
		MAX20406		-3.5		
LX Leakage	I_{LX_LKG}	V_{SUP} = 36V, V_{LX} = 0V, or V_{LX} = 36V, T_A = +25°C			1	µA
Soft-Start Ramp Time	t_{SS}			2.5		ms
Minimum On Time	t_{ON}	(Note 3)		33	55	ns
Maximum Duty Cycle	D_{MAX}	Dropout Mode	98	99		%

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150 °C, unless otherwise noted. Typical values are at T_A = 25 °C under normal conditions unless otherwise noted. Note 1 and Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING FREQUENCY						
PWM Switching Frequency	f_{SW}	400kHz	360	400	440	kHz
		2.1MHz	1.925	2.1	2.275	MHz
SYNC External Clock Frequency	f_{SYNC}	f_{SW} = 400KHz	360		600	kHz
		f_{SW} = 2.1MHz	1.7		2.6	MHz
Spread Spectrum	SPS	Percentage of f_{SW}		±3		%
PGOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_THR}	V_{OUT} rising	92	94	96	%
	V_{PGOOD_THF}	V_{OUT} falling	91	93	95	
PGOOD Debounce Time	t_{DEB}	Rising		100		µs
		Falling		50		
PGOOD Leakage Current	I_{PGOOD_LKG}	T_A = 25ºC			1	µA
PGOOD Low Voltage Level	V_{PGOOD_LOW}	Sinking 1mA			0.4	V
LOGIC LEVELS						
EN High Voltage Level	V_{EN_HIGH}		1.2			V
EN Low Voltage Level	V_{EN_LOW}				0.5	V
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 36V, T_A = 25ºC			1	µA
SYNC High Voltage Level	V_{SYNC_HIGH}		1.4			V
SYNC Low Voltage Level	V_{SYNC_LOW}				0.4	V
SYNCOUT Output Voltage Level	$V_{SYNCOUT}$	No Load	2.6	3.3	3.9	
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			20		°C

Note 1: Limits are 100% tested at TA = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at TA = +25°C.

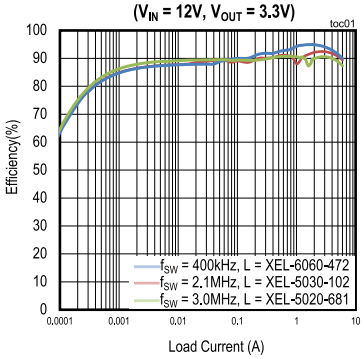
Note 2: The device is designed for continuous operation up to TJ = +125°C for 95,000 hours and TJ = +150°C for 5,000 hours.

Note 3: Guaranteed by design; not production tested.

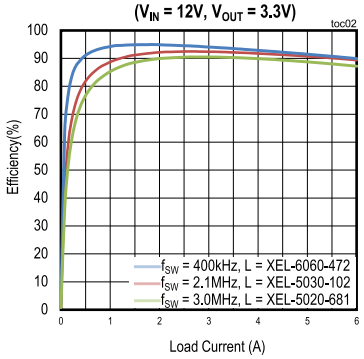
Typical Operating Characteristics

(VSUP = VEN = +14V, TA = +25°C, unless otherwise noted.)

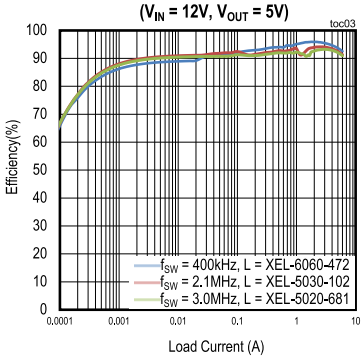
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 12V, V_{OUT} = 3.3V)



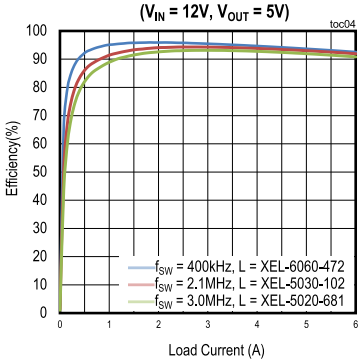
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 12V, V_{OUT} = 3.3V)



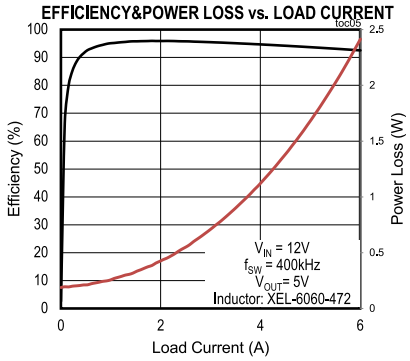
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 12V, V_{OUT} = 5V)



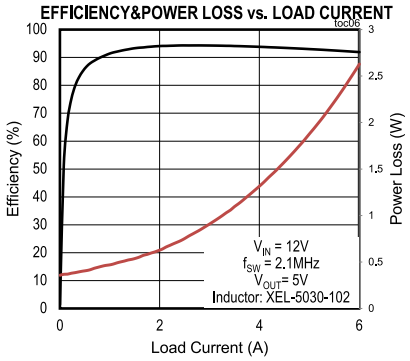
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 12V, V_{OUT} = 5V)



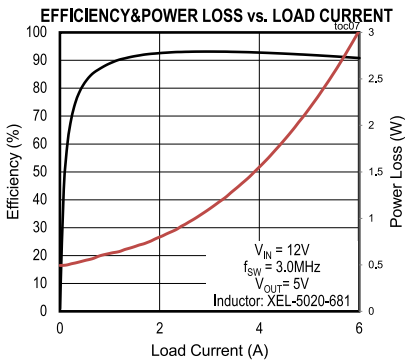
EFFICIENCY&POWER LOSS vs. LOAD CURRENT



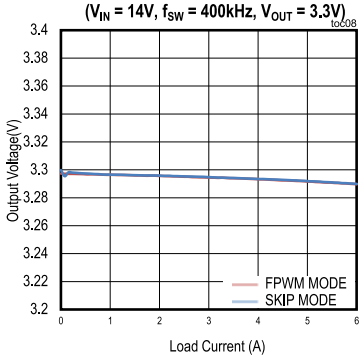
EFFICIENCY&POWER LOSS vs. LOAD CURRENT



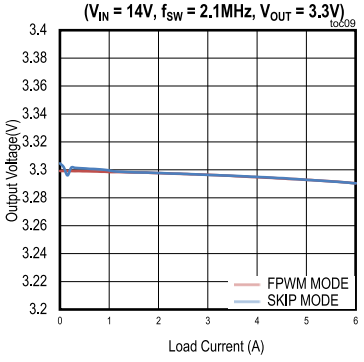
EFFICIENCY&POWER LOSS vs. LOAD CURRENT



LOAD REGULATION
(V_{IN} = 14V, f_{SW} = 400kHz, V_{OUT} = 3.3V)



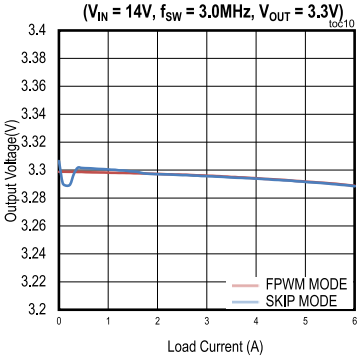
LOAD REGULATION
(V_{IN} = 14V, f_{SW} = 2.1MHz, V_{OUT} = 3.3V)



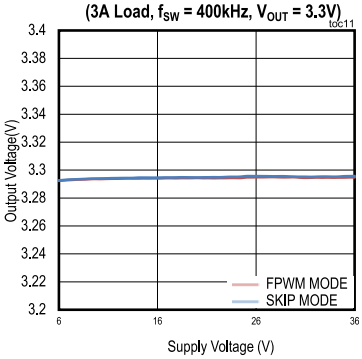
Typical Operating Characteristics (continued)

(VSUP = VEN = +14V, TA = +25°C, unless otherwise noted.)

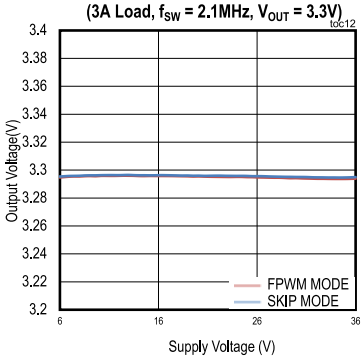
LOAD REGULATION
(V_{IN} = 14V, f_{SW} = 3.0MHz, V_{OUT} = 3.3V)



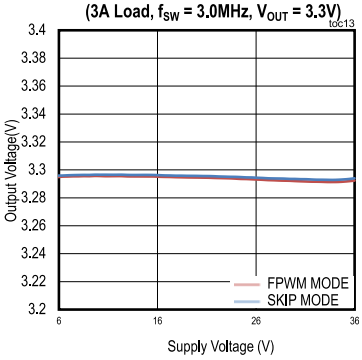
LINE REGULATION
(3A Load, f_{SW} = 400kHz, V_{OUT} = 3.3V)



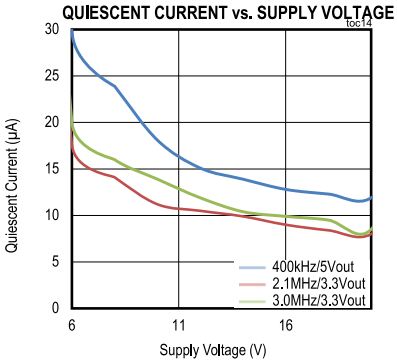
LINE REGULATION
(3A Load, f_{SW} = 2.1MHz, V_{OUT} = 3.3V)



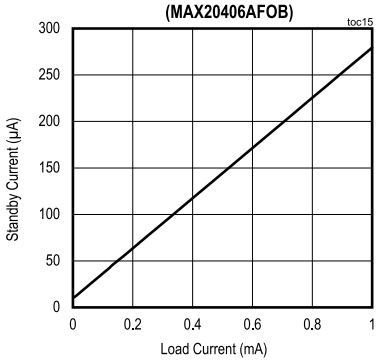
LINE REGULATION
(3A Load, f_{SW} = 3.0MHz, V_{OUT} = 3.3V)



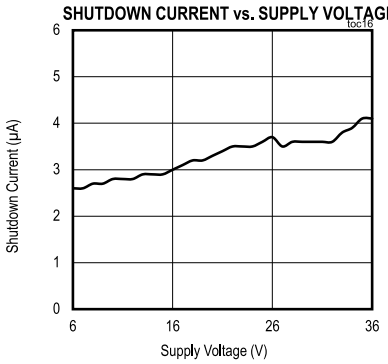
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



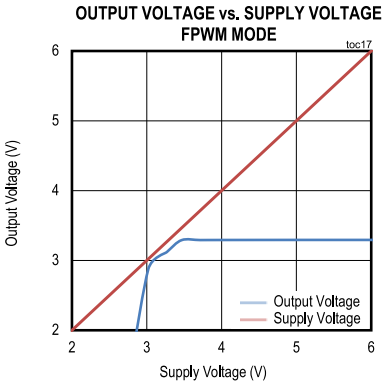
STANDBY CURRENT vs. LOAD CURRENT
(MAX20406AFOB)



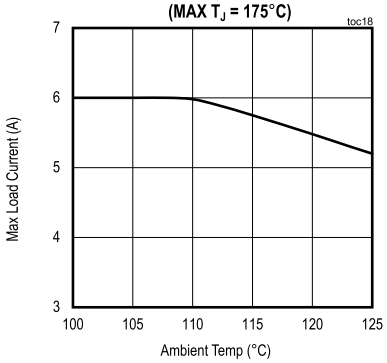
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE vs. SUPPLY VOLTAGE
FPWM MODE



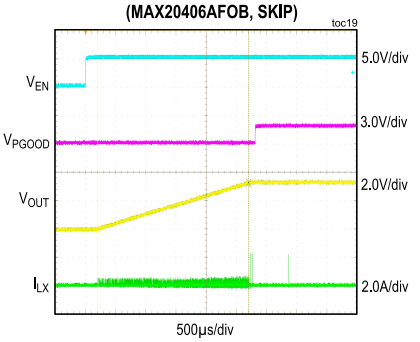
MAX LOAD CURRENT vs. AMBIENT TEMPERATURE
(MAX20406AFOB)
(MAX T_J = 175°C)



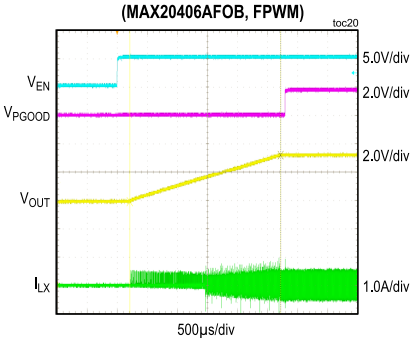
Typical Operating Characteristics (continued)

(VSUP = VEN = +14V, TA = +25°C, unless otherwise noted.)

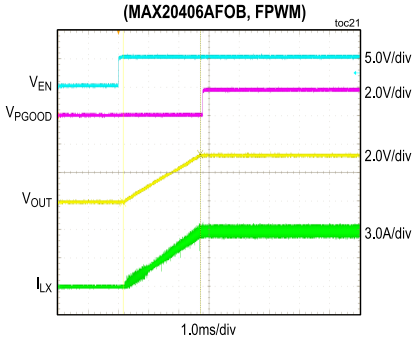
STARTUP INTO NO LOAD
(MAX20406AFOB, SKIP)



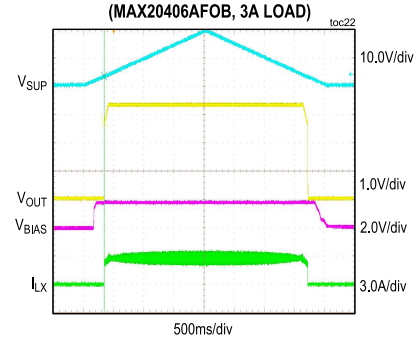
STARTUP INTO NO LOAD
(MAX20406AFOB, FPWM)



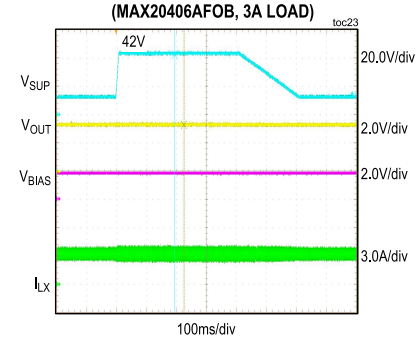
STARTUP INTO FULL LOAD
(MAX20406AFOB, FPWM)



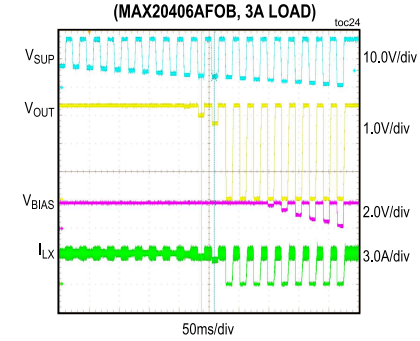
SLOW INPUT VOLTAGE RISING
(MAX20406AFOB, 3A LOAD)



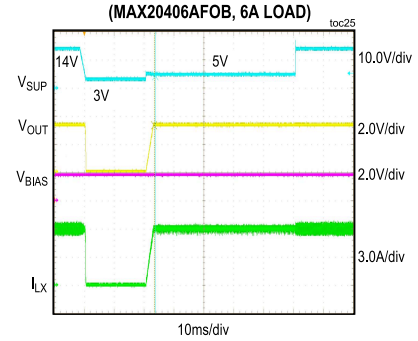
LOAD DUMP
(MAX20406AFOB, 3A LOAD)



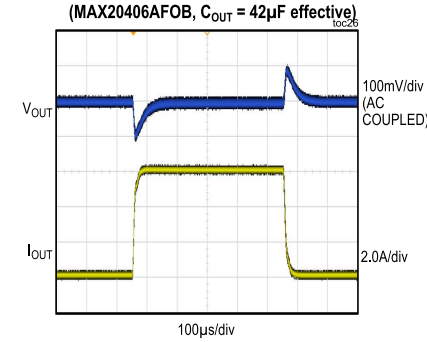
DIPS AND DROPS
(MAX20406AFOB, 3A LOAD)



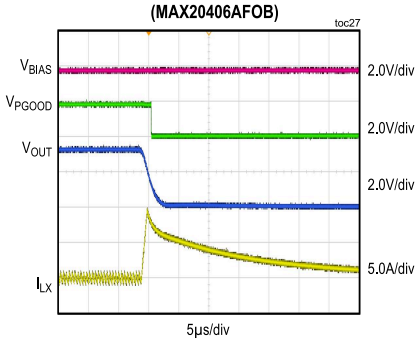
COLD CRANK
(MAX20406AFOB, 6A LOAD)



LOAD TRANSIENT
(MAX20406AFOB, C_{OUT} = 42µF effective)



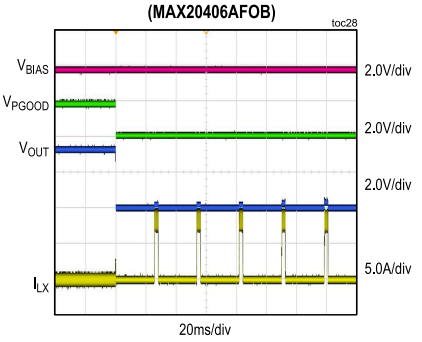
SHORT CIRCUIT RESPONSE
(MAX20406AFOB)



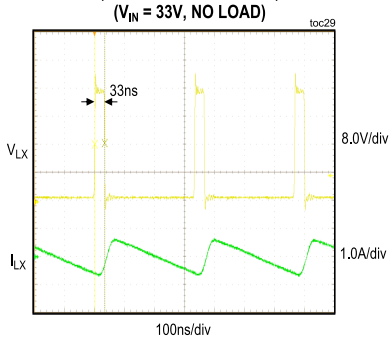
Typical Operating Characteristics (continued)

(VSUP = VEN = +14V, TA = +25°C, unless otherwise noted.)

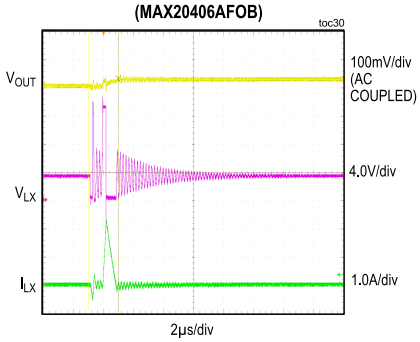
HIPCUP MODE
(MAX20406AFOB)



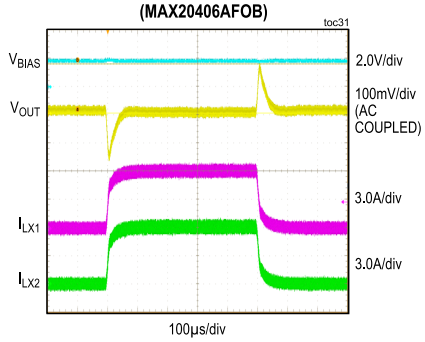
MINIMUM ON TIME
(MAX20406AFOF, FPWM)
(V_{IN} = 33V, NO LOAD)



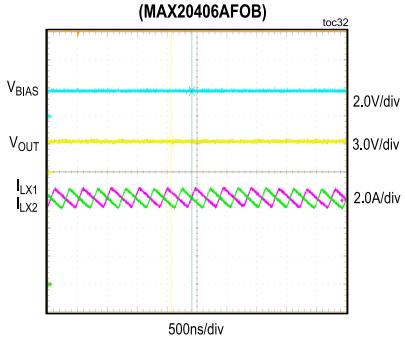
SKIP MODE NO LOAD OPERATION
(MAX20406AFOB)



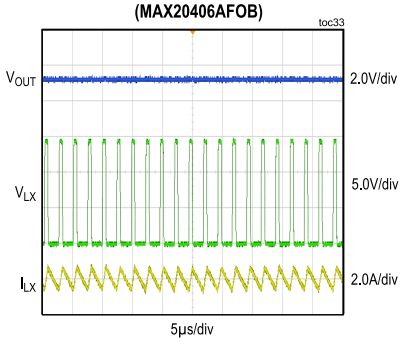
DUAL PHASE LOAD TRANSIENT
(MAX20406AFOB)



DUAL PHASE CURRENT SHARING
(MAX20406AFOB)

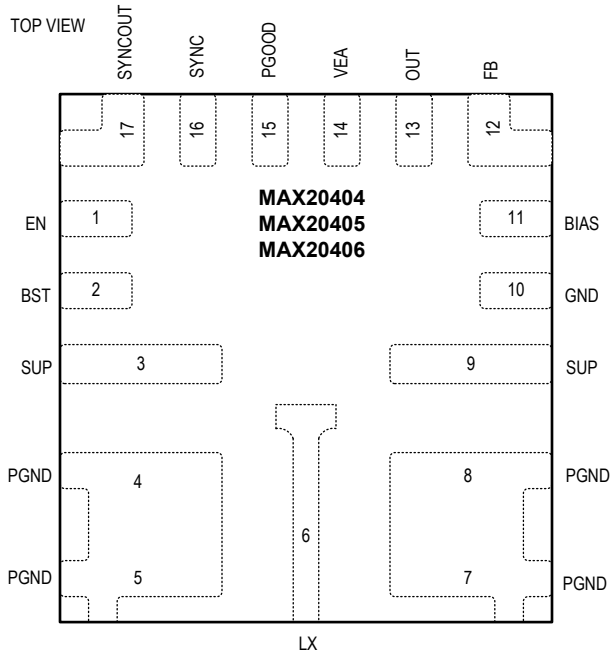


STEADY STATE SWITCHING WAVEFORM
(MAX20406AFOB)



Pin Configuration

MAX20404/MAX20405/MAX20406



17 FC2QFN
3.5mm x 3.75mm

Pin Description

PIN	NAME	FUNCTION
1	EN	High-voltage-compatible input for circuit activation. If this pin is low, the part is off.
2	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
3,9	SUP	IC Supply Input. Connect a 1µF or larger ceramic capacitor in parallel with a 4.7µF cap from SUP to PGND.
4,5,7,8	PGND	Power Ground. Connect all PGND pins together.
6	LX	BUCK Switching Node. High impedance when part is off. Connect LX to the switched side of the appropriate inductor.
10	GND	Analog Ground
11	BIAS	1.8V Internal BIAS Supply. Connect a minimum of 2µF ceramic capacitor to PGND.
12	FB	Feedback Pin. Connect a resistor-divider from OUT to FB to GND for external adjustment of output voltage. Connect to BIAS for internal fixed voltages.
13	OUT	Buck Regulator Output Voltage-Sense Input. Bypass OUT to PGND with a minimum capacitor as for appropriate paragraph.
14	VEA	Internal Voltage Loop Error-Amplifier Output. Connect to VEA of the slave for dual-phase operation. Leave unconnected for single-phase operation.
15	PGOOD	Open-Drain Reset Output. External Pullup Required.

Pin Description (continued)

PIN	NAME	FUNCTION
16	SYNC	SYNC. If connected to GND, Skip-mode operation is enabled under light loads. If connected to BIAS, forced-PWM mode is enabled.
17	SYNCOUT/ NC	180-Degree Out-of-Phase Clock Output for Multiphase Operation. NC for single-phase operation.

Detailed Description

The MAX20404/MAX20405/MAX20406 is a small, synchronous buck converter with integrated high-side and low-side switches. The device is designed to deliver up to 6A with input voltages from +3V to +36V while using only 10µA quiescent current at no load (V_{SUP} = 12V, V_{OUT} = 3.3V). Voltage quality can be monitored by observing the PGOOD signal. The IC can operate in drop-out by running at 99% duty cycle, making it ideal for automotive and industrial applications.

MAX20404/MAX20405/MAX20406 offers two fixed output voltages of 5V and 3.3V or a FB pin for an external resistor-divider. Frequency is internally fixed at 2.1MHz, 3MHz, or 400KHz, which allows for small external components, reduced output ripple, and guarantees no AM interference. The device automatically enters skip mode (SYNC pin pulled low) at light loads with ultra-low-quiescent current of 10µA at no load. It can be ordered with spread-spectrum frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency. The architecture is an average current-mode control that allows much better noise rejection of the current loop. The IC comes with a small minimum ON time of 33ns to allow for large step-down ratios in single stage without skipping cycles.

The device can also be used in a dual-phase configuration with the help of SYNCOUT and VEA pin. An innovative Average Current Mode Control architecture provides noise immunity and accurate dynamic current sharing during transients. High-power designs with up to 12A of output current can be enabled with integrated switches using the IC's dual-phase capability. FC2QFN provides improved thermal and EMI performance. Symmetrical pin-out across V_{IN} and PGND further improves the EMI performance, enabling low-noise designs.

Multiphase Operation

MAX20404/MAX20405/MAX20406 is capable of dual-phase operation for high-current applications, and each IC can be configured as a master or a slave. The multi-phase operation is intended for forced-PWM mode only. SYNCOUT will be 180 degrees out of phase with the master clock. If the device is in Skip mode, then no clock will be present on SYNCOUT. To enable low-Iq operation in dual-phase configuration, disable the EN of the slave to turn OFF the IC and save quiescent current.

For a slave, connect SYNCOUT to BIAS. When EN is high, there will be a procedure to detect if the IC is a master (SYNCOUT not connected to BIAS) or a slave. The pin VEA will be the voltage-error amplifier output for the master or the current-error amplifier input for the slave. Connect the VEA pin of the master to VEA of the slave to ensure balanced current sharing between two phases. FB of the master and slave should be connected to their respective BIAS pins for internal fixed V_{OUT} setting. Since the slave IC uses the outer voltage loop of the master (through the VEA pin), the internal resistor-divider of the slave IC is not used and any mismatch in the output voltage is avoided. Refer to Figure 1 for dual-phase configuration setup using MAX20404/MAX20405/MAX20406.

For external resistor-divider configurations, use two separate resistor-dividers for each IC to avoid the FB pins of master and slave being connected together at the same point.

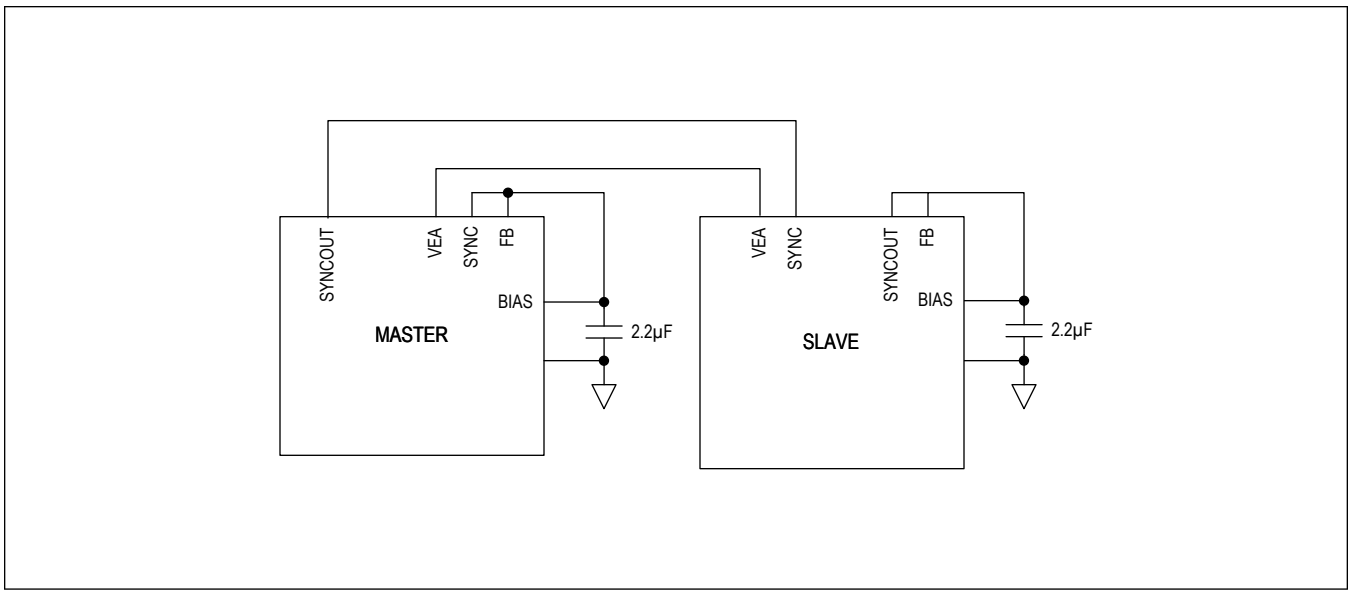


Figure 1. Typical Dual-Phase Configuration Setup Using Fixed Internal V_{OUT} Setting

Linear Regulator Output (BIAS)

The device includes a 1.8V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to GND. During start-up, the bias regulator draws power from the input and switches over to the output after the start-up is complete (if V_{OUT} > 2.5V). For output voltages less than 1.8V, the bias regulator is always tied to the input

System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3V. EN turns on the internal linear (BIAS) regulator. Once V_{BIAS} is above the internal lockout threshold (V_{UVBIAS} = 1.63V (typ)), the converter activates and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During shutdown, the BIAS regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 4µA (typ). Drive EN high to bring the device out of shutdown.

Synchronization Input (SYNC)

MAX20404/MAX20405/MAX20406 comes with a SYNC pin, which is a logic-level input used for operating-mode selection and frequency control. Connecting SYNC to BIAS or to an external clock enables forced fixed-frequency (FPWM) operation. Connecting SYNC to GND enables automatic skip-mode operation for better light-load efficiency. The IC synchronizes to an external clock at the rising edge applied at the SYNC pin. The devices synchronize to the external clock in two cycles. When the external clock signal at SYNC is absent for more than two clock cycles, the devices use the internal clock.

Soft Start

The devices include a fixed, internal 2.5ms soft start. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Short-Circuit Protection

The devices feature a current limit that protects them against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the

specified LX current-limit threshold. The converter then turns the high-side MOSFET off and the low-side MOSFET on to allow the inductor current to ramp down. Once the inductor current crosses below the current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

A hard short is detected when the output voltage falls below 50% of the target (for fixed internal output) or 25% of the target (for external output) while in current limit. If this occurs, hiccup mode activates, and the output turns off for 25ms. The output then enters soft start and powers back up. This repeats indefinitely while the short circuit is present. Hiccup mode is disabled during soft start.

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed 5V or 3.3V output voltage. To set the output to other voltages between 0.8V and 10V, connect a resistor-divider from the output (OUT) to GND Figure 2. Select R_{FB2} (FB to GND resistor) less than or equal to 100kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

Equation 1:

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} is the feedback regulation voltage. See *Electrical Characteristics*.

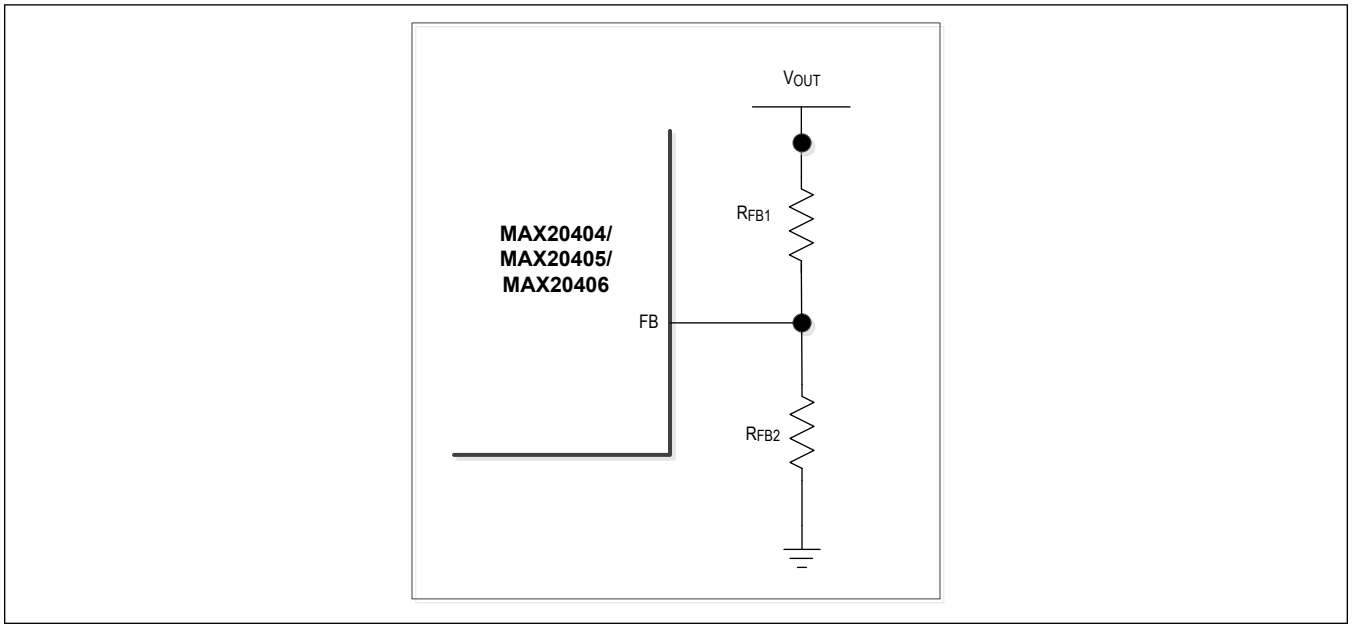


Figure 2. Output Voltage Setting Using External Resistor-Divider

Dual-Phase Operation

Low-Iq Operation in Dual Phase

MAX20404/MAX20405/MAX20406 comes with dual-phase capability where each IC can be either configured as master or slave. The SYNCOUT pin of the master outputs 180-degree out-of-phase clock when SYNC is tied high (FPWM mode). For low-Iq mode, the SYNC pin of the master should be pulled low (Skip mode). In this mode, there is no clock present on SYNCOUT pin of the master and the master IC enters Skip mode. The internal circuit of the slave IC remains ON during this time and actively looks for the SYNCOUT signal from the master. Since the slave IC is ON, the quiescent current is slightly higher, even though both the ICs skip pulses.

To improve the light-load efficiency and further reduce the Iq, slave EN should be pulled low. This disables the slave and its internal circuits, further reducing the Iq. Table 1 summarizes the truth table for low-Iq operation.

Table 1. Configurations for Low-Iq Operation

MASTER	SLAVE	MODE
EN = High, SYNC=BIAS	EN = High	FPWM (high Iq)

Table 1. Configurations for Low-Iq Operation (continued)

EN = High, SYNC=Low	EN = High	Skip mode (low Iq)
EN = High, SYNC=Low	EN = Low	Standby mode (ultra-low Iq)
EN = Low	EN = High	Not allowed

Setting Output Voltage

For setting the output voltage to internal fixed voltage, order the same fixed V_{OUT} setting for both master and slave ICs and connect the FB pin to its respective BIAS. It is recommended NOT to connect the FB pins of the master and slave together.

For setting the output voltage to a value other than the available fixed V_{OUT} options, connect a resistor-divider between OUT, FB, and GND as shown inFigure 3. An identical but separate resistor-divider for master and slave is recommended.

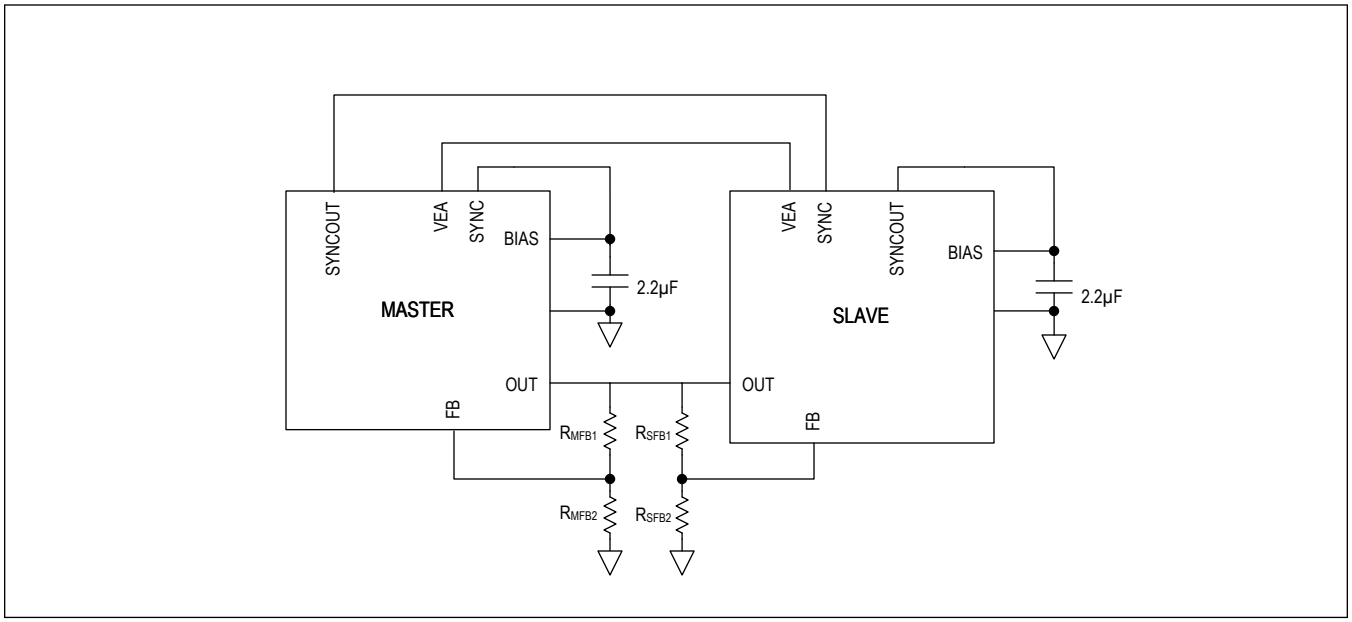


Figure 3. Typical Application Circuit for Dual-Phase Configuration with External Resistor-Divider

Inductor Selection

Inductor design is a compromise between the size, efficiency, control-loop bandwidth, and stability of the converter. Insufficient inductance value would increase the inductor current ripple, causing higher conduction losses and higher output voltage ripple. Since the slope compensation is fixed internally for MAX20404/MAX20405/MAX20406, it might also cause current-mode-control instability to appear. A large inductor reduces the ripple, but increases the size and cost of the solution and slows the response. Table 2 provides optimized inductance values for each switching frequency. The nominal standard value selected should be within ±30% of the specified inductance.

Table 2. Inductor Selection

SWITCHING FREQUENCY	OUTPUT VOLTAGE (V)	VARIANT	INDUCTOR_TYP(µH)
400kHz	0.8-3	MAX20404/5/6	2.2
	3-10	MAX20404/5	6.8
		MAX20406	4.7
2.1MHz	0.8-3	MAX20404/5/6	0.56
	3-6	MAX20404/5/6	1

Table 2. Inductor Selection (continued)

	6-10	MAX20404/5/6	1.2
3.0MHz	0.8-3	MAX20404/5/6	0.47
	3-6	MAX20404/5	0.9
		MAX20406	0.68
	6-10	MAX20404/5	0.9
		MAX20406	0.82

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. MAX20404/MAX20405/MAX20406 incorporates a symmetrical pin-out that can be leveraged for better EMI performance. Connect two high-frequency 0603 or smaller capacitors on two SUP pins on either side of the package for good EMI performance. Connect a high-quality, 4.7µF (or larger) low-ESR ceramic capacitor on the SUP pin for low-input voltage ripple.

A bulk capacitor with higher ESR (such as an electrolytic capacitor) is normally required as well to lower the Q of the front-end circuit and provide the remaining capacitance needed to minimize input-voltage ripple. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

Equation 6:

$$I_{RMS} = I_{LOAD(MAX)} \cdot \left(\frac{\sqrt{V_{OUT} \cdot (V_{SUP} - V_{OUT})}}{V_{SUP}} \right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$V_{SUP} = 2 \times V_{OUT}$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple consists of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

Equation 7:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \cdot V_{OUT}}{V_{SUP} \cdot f_{SW} \cdot L}$$

and:

$$C_{IN} = \frac{I_{OUT} \cdot D(1 - D)}{\Delta V_Q \cdot f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

where: I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

Output capacitance is selected to satisfy the output load-transient, output voltage ripple and closed-loop stability requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. For a buck converter that is controlled by inductor current, as employed in MAX20404/MAX20405/MAX20406, output capacitance also affects the control-loop stability.

The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 4 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output-ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 8:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{p-p}}$$

$$COUT = \frac{\Delta Ip-p}{8 \cdot \Delta V_Q \cdot f_{SW}}$$

where:

$$\Delta I_{p-p} = \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot L}$$

$$V_{OUT_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔIP-P is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency.

The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient-load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 9:

$$C_{OUT} = \frac{\Delta I}{\Delta V \cdot 2\pi \cdot f_C}$$

where ΔI is the load change, ΔV is the allowed voltage droop, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. Any calculations involving C_{OUT} should consider capacitance tolerance, temperature, and voltage derating. The values give in the table below are actual capacitances after considering these factors.

For optimal phase margin, the recommended output capacitances are shown in Table 3. If a lower or higher output capacitance is required for the application, contact the factory for an optimized solution.

Table 3. Output Capacitance Selection

FREQUENCY(kHz)	OUTPUT VOLTAGE (V)	OUTPUT CAPACITOR_TYP (µF)	OUTPUT CAPACITOR_MIN (µF)
400	0.8-3	800	640
	3-6	100	90
	6-10	66	40
2100	0.8-3	235	120

Table 3. Output Capacitance Selection (continued)

	3-6	50	35
	6-10	44	20
3000	0.8-3	141	60
	3-6	30	20
	6-10	30	15

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Refer to Figure 2 and the following guidelines for good PCB layout:

1) Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.

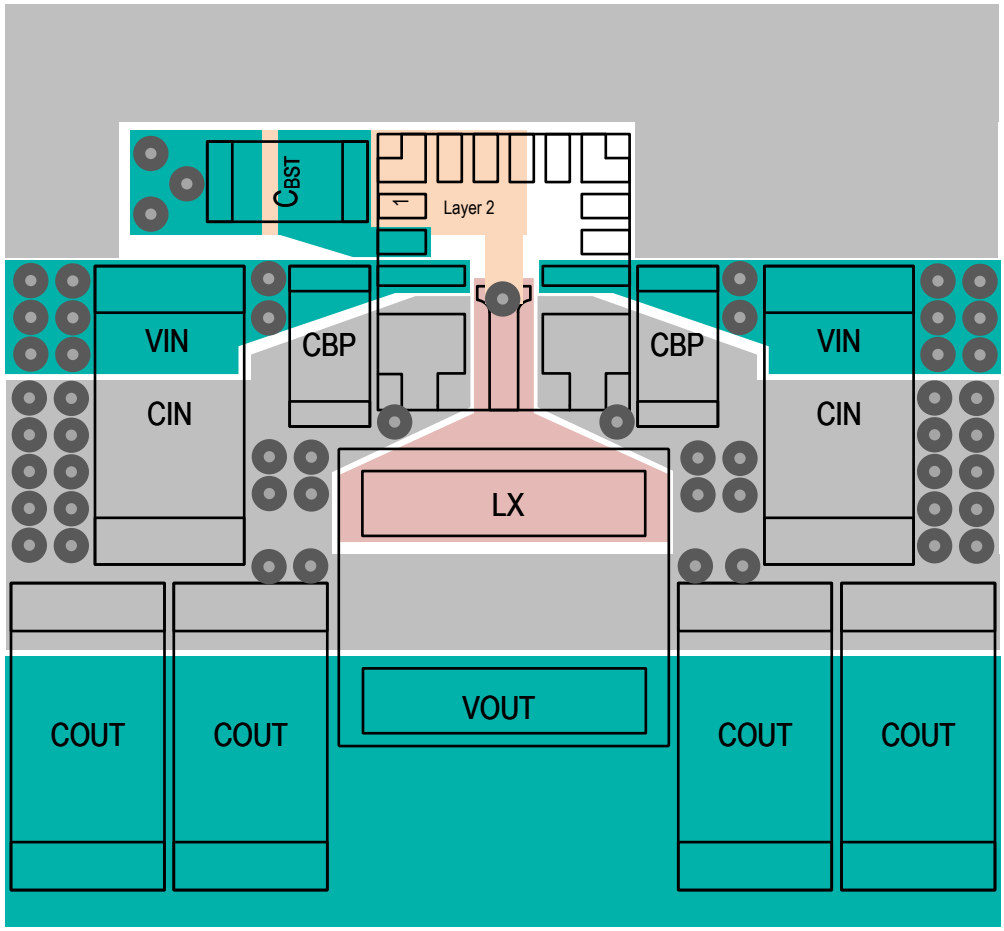
2) Place the ceramic input-bypass capacitors, C_{BP} and C_{IN}, as close as possible to the SUP and PGND pins on both sides of the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. C_{BP} should be located closest to the IC and should have very good high-frequency performance (small package size and high capacitance). This will provide the best EMI rejection and minimize internal noise on the device, which can degrade performance.

3) Place the inductor (L), output capacitors (C_{OUT}), bootstrap capacitor (C_{BST}) and BIAS capacitor (C_{BIAS}) in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors (C_{OUT}) near the inductor so that the ground side of C_{OUT} is near the CIN ground connection to minimize the current-loop area. Place the BIAS capacitor (C_{BIAS}) next to the BIAS pin.

4) Place the bootstrap capacitor C_{BST} close to the IC and use short wide traces to minimize the loop area in order to minimize the parasitic inductance. Use the nearest layer for return trace (C_{BST} to LX) to minimize the inductance further. Refer to the layout in the EVKIT for optimum design. High parasitic inductance can impact switching speed (increase switching losses) and cause high dv/dt noise.

5) Use a continuous copper GND plane on the layer next to the IC to shield the entire circuit. GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias at the GND terminals of the IC and input/output/ bypass capacitors. Do not separate or isolate PGND and GND connections with separate planes or areas.

6) Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor and LX node and other noisy signals.


CBST
1
Layer 2
VIN
CBP
CBP
VIN
CIN
CIN
LX
VOUT
COUT
COUT
COUT
COUT

Typical Application Circuits

Figure 1. Single Phase 400kHz 6A Operation

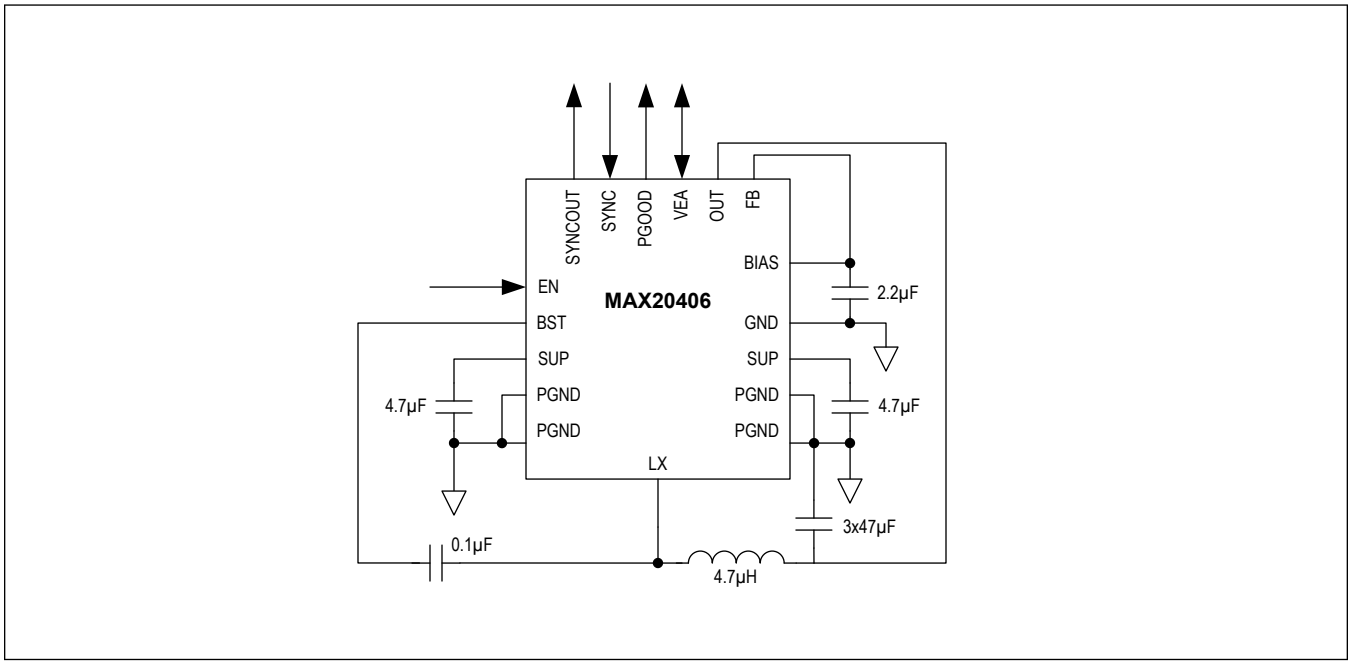
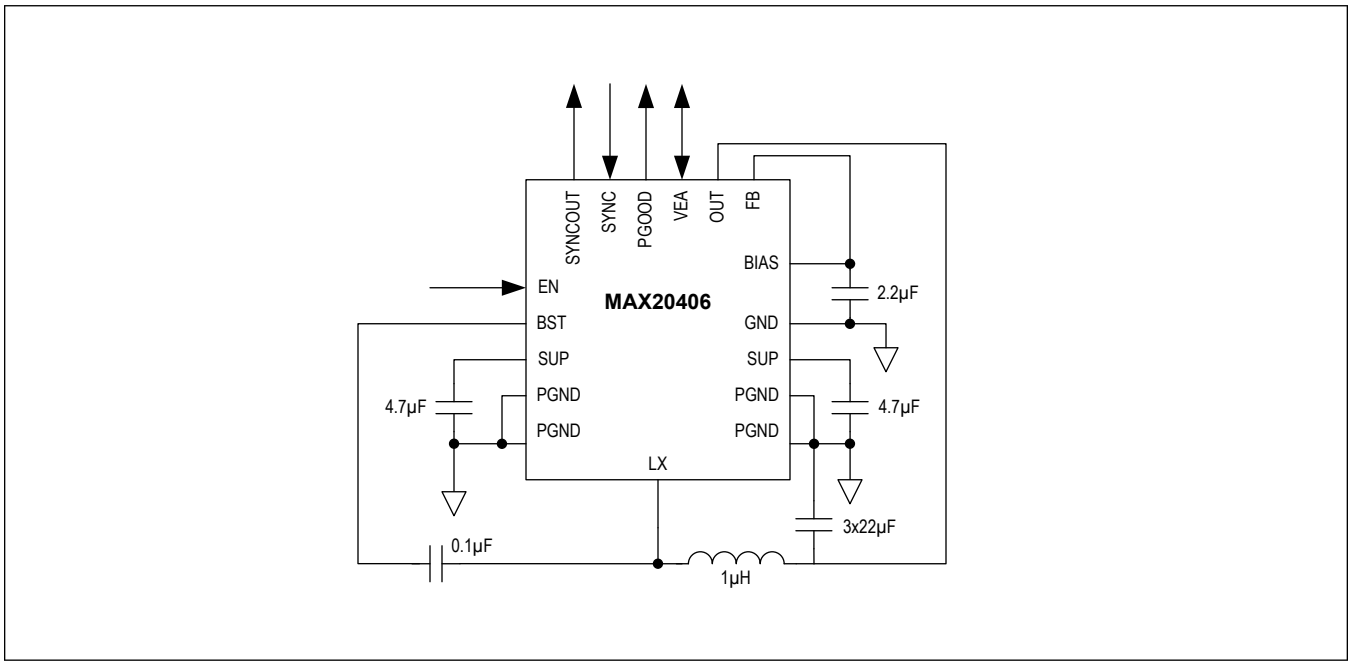
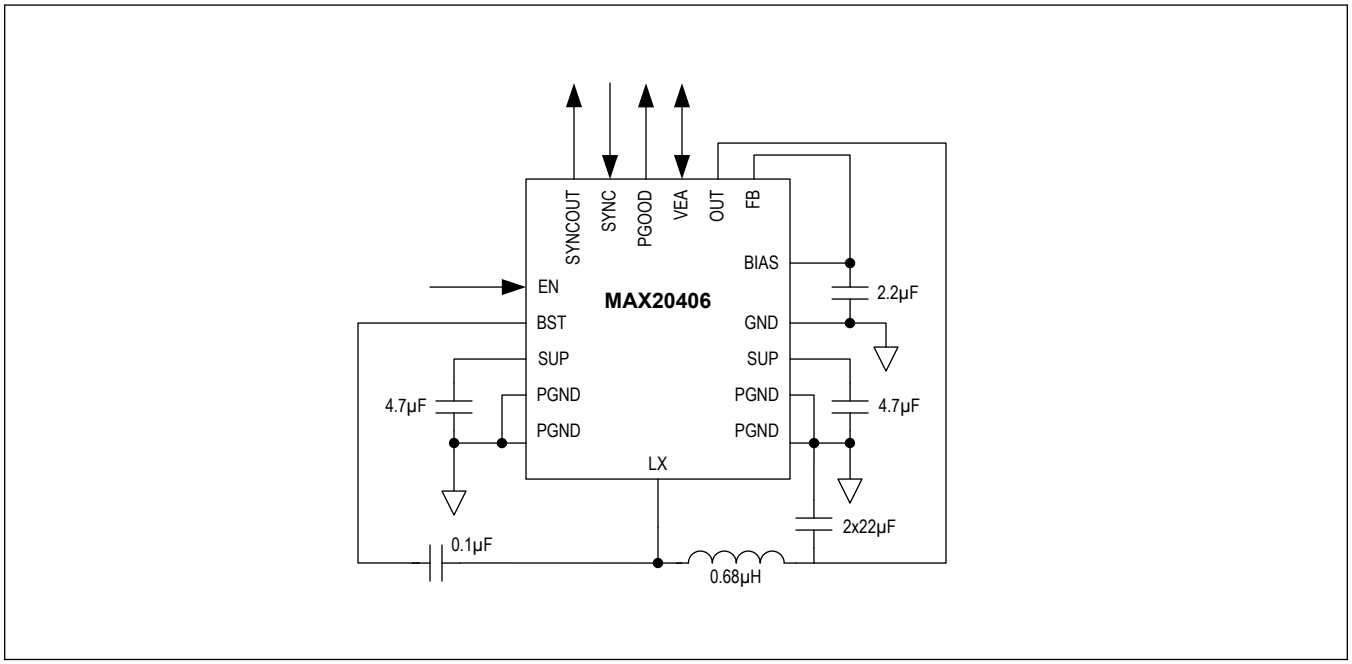


Figure 2. Single Phase 2.1MHz 6A Operation



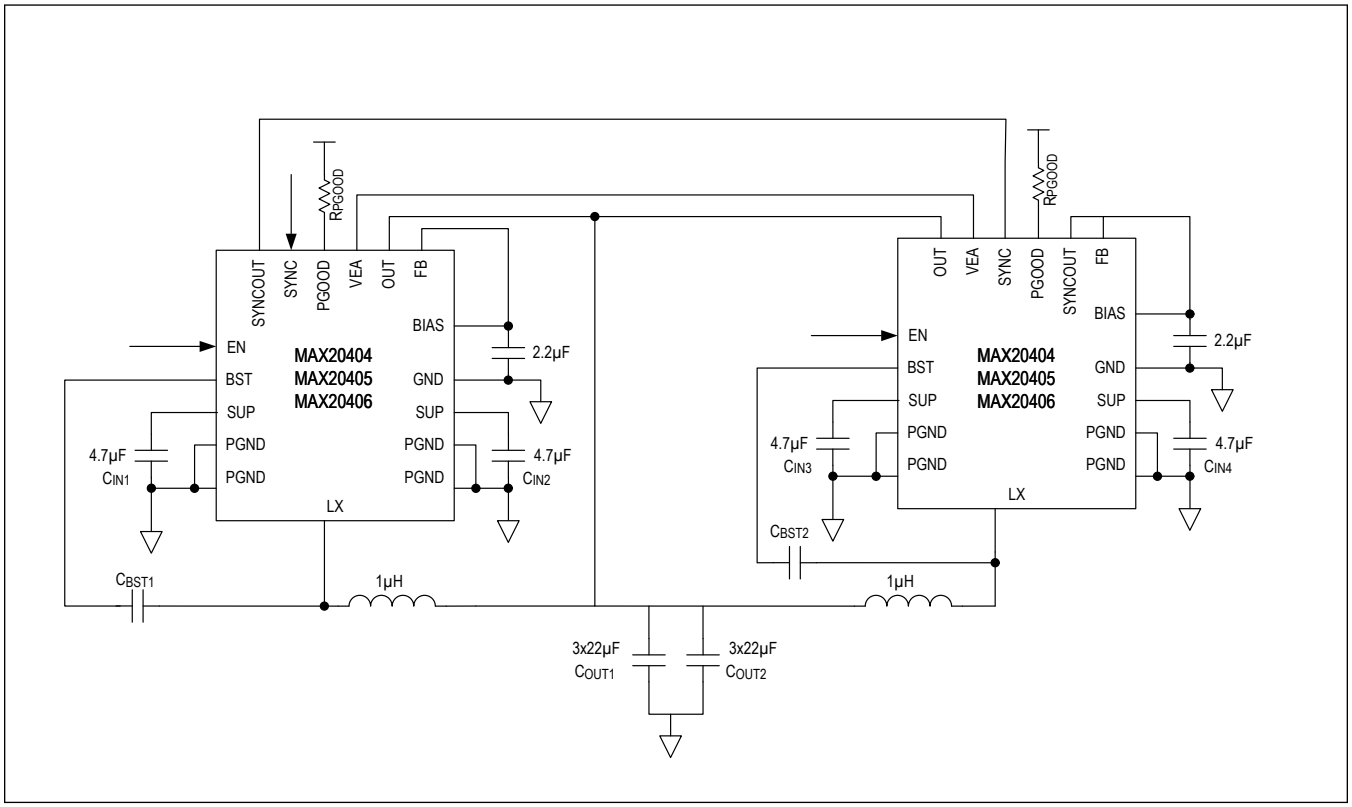
Typical Application Circuits (continued)

Figure 3. Single Phase 3MHz 6A operation



Typical Application Circuits (continued)

Figure 4. Dual Phase Master-Slave 2.1MHz Operation



Ordering Information

PART NUMBER	V_{OUT} (FB TIED TO BIAS)[1]	MAXIMUM LOAD CURRENT (A)	FREQUENCY (kHz)	SPREAD SPECTRUM[2]
MAX20404AFOA/VY+	5	4	2100	ON
MAX20404AFOB/VY+	3.3	4	2100	ON
MAX20404AFOC/VY+*	5	4	400	ON
MAX20404AFOD/VY+*	3.3	4	400	ON
MAX20404AFOE/VY+*	5	4	3000	ON
MAX20404AFOF/VY+*	3.3	4	3000	ON
MAX20405AFOA/VY+*	5	5	2100	ON
MAX20405AFOB/VY+*	3.3	5	2100	ON
MAX20405AFOC/VY+*	5	5	400	ON
MAX20405AFOD/VY+	3.3	5	400	ON
MAX20405AFOE/VY+*	5	5	3000	ON
MAX20405AFOF/VY+*	3.3	5	3000	ON
MAX20406AFOA/VY+	5	6	2100	ON
MAX20406AFOB/VY+	3.3	6	2100	ON
MAX20406AFOC/VY+*	5	6	400	ON
MAX20406AFOD/VY+*	3.3	6	400	ON
MAX20406AFOE/VY+*	5	6	3000	ON
MAX20406AFOF/VY+*	3.3	6	3000	ON
MAX20406AFOG/VY+*	5	6	2100	OFF
MAX20406AFOH/VY+*	3.3	6	2100	OFF

** Future Part - Contact factory for availability.*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

/VY+ Denotes a side wettable automotive qualified package.

1 Other fixed output voltage between 2.9V to 6V with 100mV step are available, contact the factory for custom requests.

2 All ICs come default with Spread Spectrum turned ON. For SS OFF parts, contact the factory.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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