Click here for production status of specific part numbers.

MAX38903A/MAX38903B/ MAX38903C/MAX38903D

1.7V–5.5V_{IN}, 1A Low Noise LDO Linear Regulators in TDFN and WLP

General Description

The MAX38903A/B/C/D are a family of low-noise linear regulators that deliver up to 1A of output current with only 7μV_{RMS} of output noise from 10Hz to 100kHz.

These regulators maintain ±1% output accuracy over a wide input voltage range, requiring only 100mV of input-to-output headroom at full load. The 1200µA no-load supply current is independent of dropout voltage.

The MAX38903A has nine pin-selectable output voltages 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.1V, 3.3V, 4.0V, and 5V. The MAX38903B/C output voltage can be adjusted to a value in the range of 0.6V to 5.0V using two external resistors. The MAX38903B also includes an active-high POK signal for trouble-free load startup.

The MAX38903D has factory-preset output voltages over the range of 0.7V to 5V in 50mV steps. All versions include a programmable output soft-start rate, output over-current and thermal overload protection.

The MAX38903A/B are offered in a 10-pin, 3mm x 3mm TDFN package, while the MAX38903C/D are offered in a 9-bump, 0.4mm pitch, 1.4mm x 1.4mm wafer-level package (WLP).

Applications

- Communication Systems, Test Equipment, Medical Equipment
- High-End Audio Systems
- High-Resolution Data Acquisition Systems

Benefits and Features

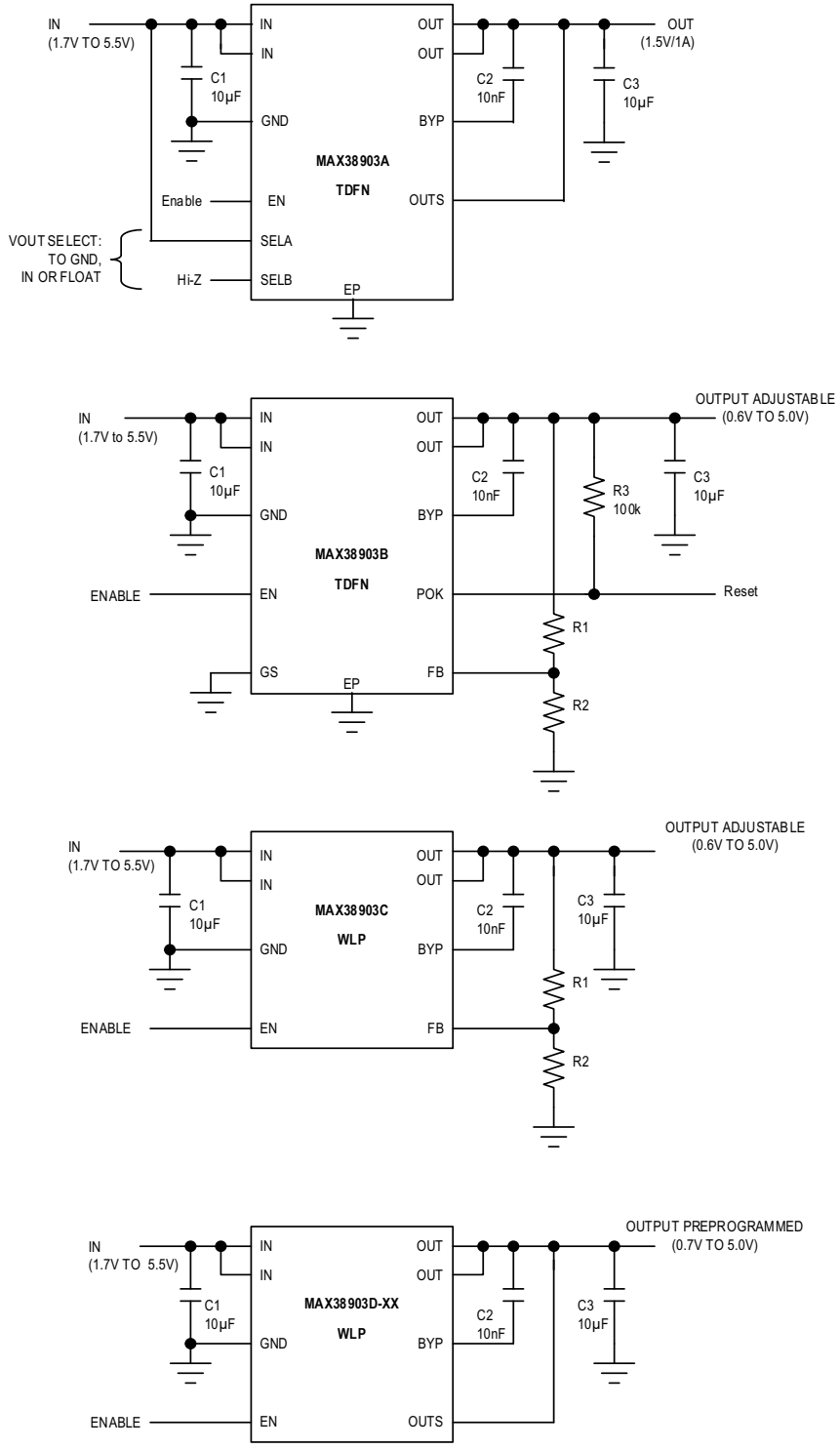
- Delivers Flexible Operating Range
  - 1.7V to 5.5V Input Voltage Range
  - 0.6V to 5.0V Programmable Output Voltage
  - 1A Maximum Output Current
  - 100mV Maximum Dropout at 1A Load
  - < 1µA Shutdown Supply Current
- Reduces Noise and Improves Accuracy
  - ±1% DC Accuracy Over Load, Line, and Temperature
  - 7μV_{RMS} Output Noise, 10Hz to 100kHz
  - 1200µA Operating Supply Current
  - 70dB PSRR at 10kHz
- Enables Ease-of-Use and Robust Protection
  - Stable with 4µF(min) Output Capacitance
  - Programmable Soft-Start Rate
  - Overcurrent and Overtemperature Protection
  - Output-to-Input Reverse Current Protection
  - Power-OK Output
- Reduces Size, Improves Reliability
  - 3mm x 3mm, 10-pin TDFN Package and 1.4mm x 1.4mm, 3 x 3 Bump, 0.4mm Pitch WLP
  - -40°C to 125°C Operating Temperature

Ordering Information appears at end of data sheet.

19-100370; Rev 2; 1/19

maxim integrated™

Typical Operating Circuits



Absolute Maximum Ratings

IN, EN, POK, RSEL, BYP to GND .....-0.3V to +6V
FB, OUT, OUTS, SELA, SELB to GND.....-0.3V to +6V
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4mW/°C above 70°C).....1951mW
WLP (derate 11.9mW/°C above 70°C).....952mW

Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T1033+1C
Outline Number	**21-0137**
Land Pattern Number	**90-0003**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	9°C/W

WLP

Package Code	N91D1+1
Outline Number	**21-100257**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	83.98°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 0.047µF, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 100mA, circuit of Figure 2, unless otherwise specified. Note 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by output accuracy		1.7		5.5	V
Input Undervoltage Lockout	V_{IN_UVLO}	V_{IN} rising, 100mV hysteresis		1.5	1.6	1.7	V
Output Voltage Range	V_{OUT}	V_{IN} > V_{OUT} + 0.1V		0.6		5.0	V
Output Capacitance	C_{OUT}	For stability and proper operation		4	10		µF
Supply Current	I_Q	I_{OUT} = 0mA			1200	2000	µA
	$I_{SHUTDOWN}$	V_{EN} = 0V	T_J = +25°C		0.01	0.1	
			T_J = +125°C		0.1		µA
Output Accuracy (MAX38903A/D Only)	ACC38903A/D	I_{OUT} from 0.1mA to 1A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V, V_{OUT} from 0.7V to 5.0V		-1.0		+1.0	%
Output Accuracy (MAX38903B/C Only)	$ACC_{38903B/C}$	I_{OUT} from 0.1mA to 1A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V, V_{OUT} from 0.6V to 5.0V		0.594	0.6	0.606	V
Load Regulation		I_{OUT} from 0.1mA to 1A			0.02		%
Load Transient		I_{OUT} = 50mA to 1A to 50mA, t_{RISE} = t_{FALL} = 1µs			50		mV
Line Regulation		V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V			0.05		%
Line Transient		V_{IN} = 4V to 5V to 4V, I_{OUT} = 1A, t_{RISE} = t_{FALL} = 5µs			3		mV
Dropout Voltage (Note 2)		I_{OUT} = 1A	V_{IN} = 3.6V TDFN		48	100	mV
			V_{IN} = 3.6V WLP		32	100	
			V_{IN} = 2.5V TDFN		57	160	
			V_{IN} = 2.5V WLP		42	160	
			V_{IN} = 1.7V TDFN		85	300	
			V_{IN} = 1.7V WLP		68	300	
Current Limit		V_{OUT} = 95% of regulation		1.15	1.4	1.6	A
Output Noise		I_{OUT} = 100mA, f = 10Hz to 100kHz	C_{BYP} = 47nF		7		$µV_{RMS}$
Power Supply Rejection Ratio	PSRR	I_{OUT} = 100mA	f = 1kHz		70		dB
			f = 10kHz		70		
			f = 100kHz		60		
			f = 1MHz		40		
BYP Capacitor Range	C_{BYP}	Regulator remains stable		0.001		0.1	µF
BYP Soft-Start Current		From BYP to GND during startup			50		µA
EN Input Threshold		V_{IN} from 1.7V to 5.5V	EN rising		0.8	1.2	V
			EN falling	0.4	0.7		
EN Input Leakage Current		V_{EN} from 1.7V to 5.5V	T_J = +25°C	-1	0.001	+1	µA
			T_J = +125°C		0.01		
POK Threshold (MAX38903B Only)		V_{OUT} when $\overline{POK}$ switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		

Electrical Characteristics (continued)

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 0.047µF, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 100mA, circuit of Figure 2, unless otherwise specified. Note 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POK Voltage, Low (MAX38903B Only)		I_{POK} = 1mA			10	100	mV
POK Leakage Current (MAX38903B Only)		V_{POK} = 5.5V	T_J = +25°C	-0.1	+0.001	+0.1	µA
			T_J = +125°C		0.01		
SELA/B Input Resistance (MAX38903A Only)	$R_{INSELA/B}$	When shorted to GND or IN				500	Ω
		When Hi-Z		1			MΩ
SELA/B Input Capacitance (MAX38903A Only)	$C_{INSELA/B}$	When Hi-Z				10	pF
Input Reverse Current Threshold		V_{OUT} = 3.6V, when V_{IN} falls to 0V			400		mA
Thermal Shutdown Threshold		T_J when output turns on/off	T_J rising		165		°C
			T_J falling		150		

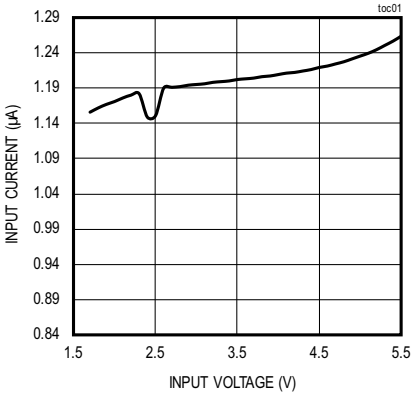
Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

Note 2: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 95% of its nominal value.

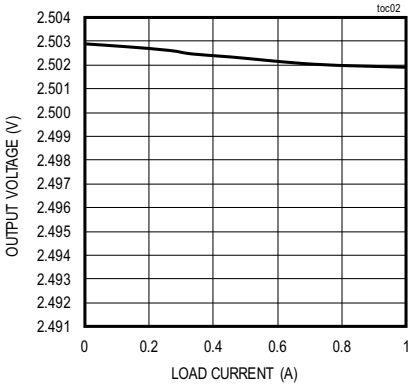
Typical Operating Characteristics

(MAX38903A, V_{IN} = 3.6V, V_{OUT} = 2.5V, T_A = 25°C, C_{IN} = 10µF , C_{OUT} = 10µF, unless otherwise noted.)

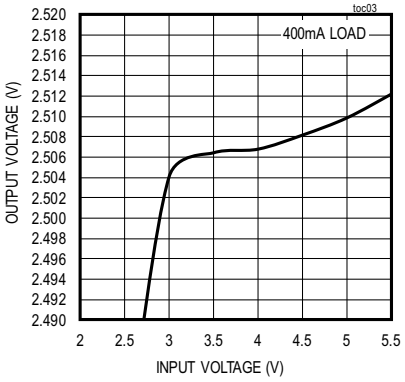
QUIESCENT CURRENT
EN = HIGH, NO LOAD



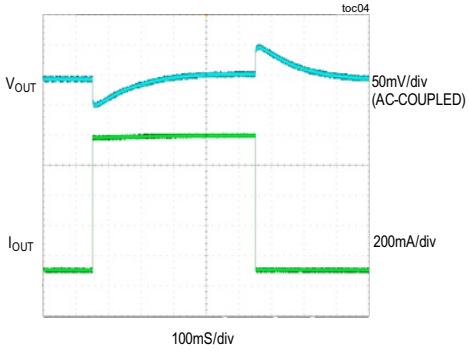
LOAD REGULATION



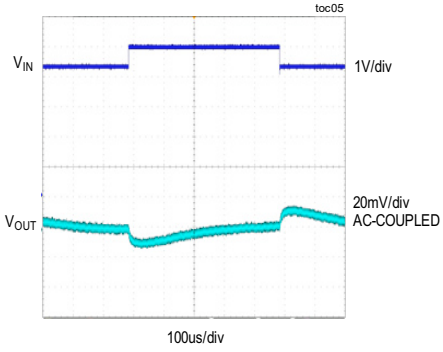
LINE REGULATION



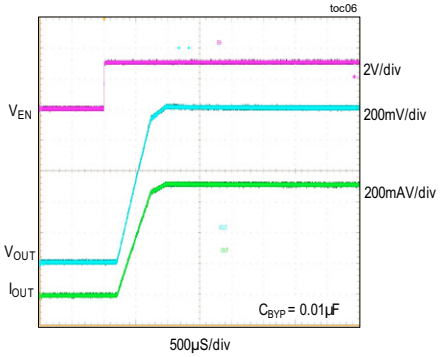
LOAD TRANSIENT RESPONSE
100mA TO 1A TO 100mA



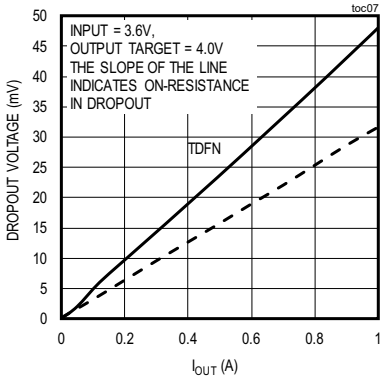
LINE TRANSIENT RESPONSE



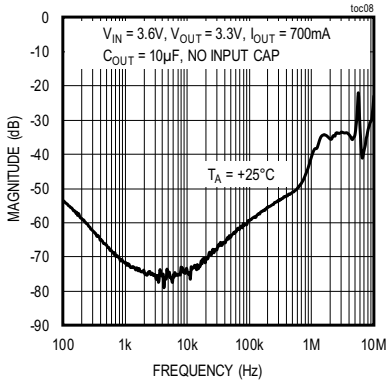
STARTUP WAVEFORM



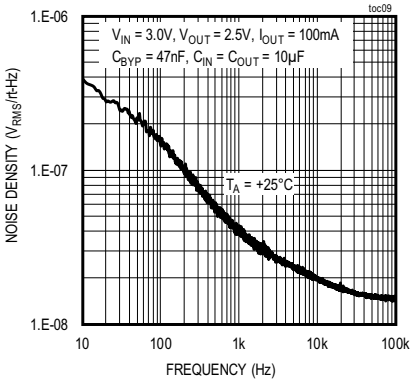
DROPOUT VOLTAGE vs. LOAD CURRENT



PSRR vs. FREQUENCY



OUTPUT NOISE SPECTRAL DENSITY
vs. FREQUENCY



Pin Configurations

MAX38903A

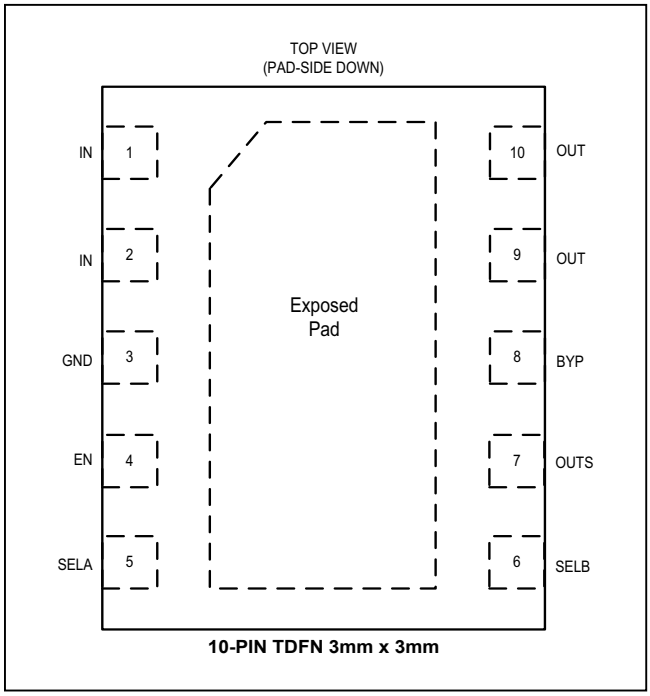


Figure 1. MAX38903A Pin Configuration

MAX38903B

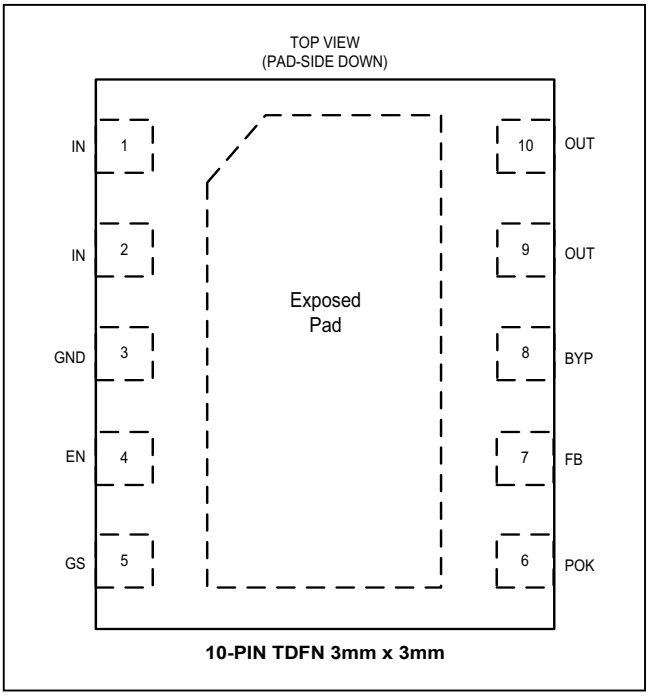


Figure 2. MAX38903B Pin Configuration

MAX38903C

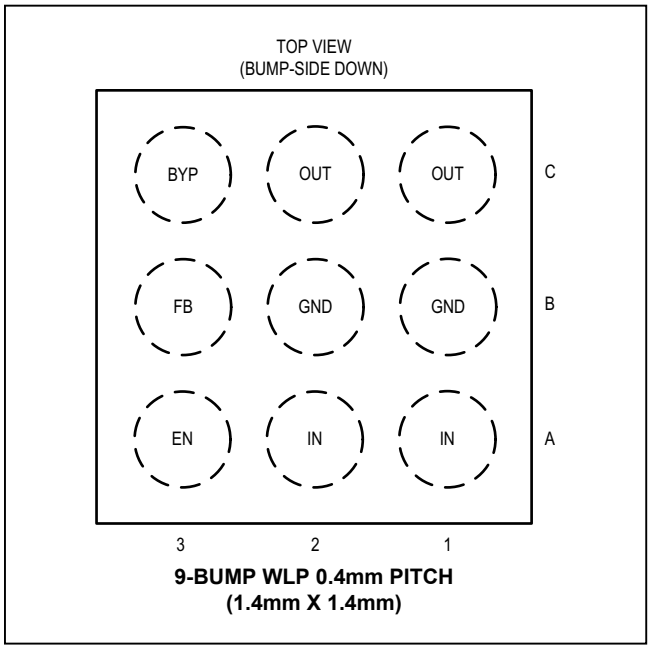


Figure 3. MAX38903C Pin Configuration

MAX38903D

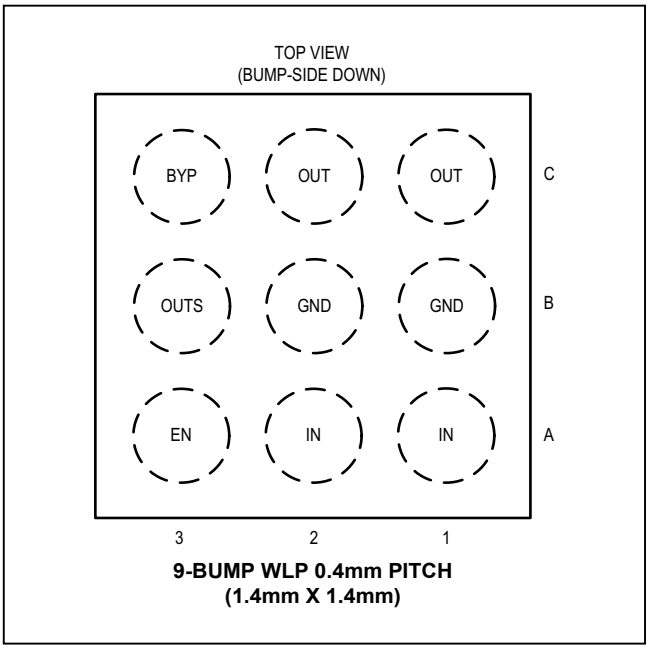
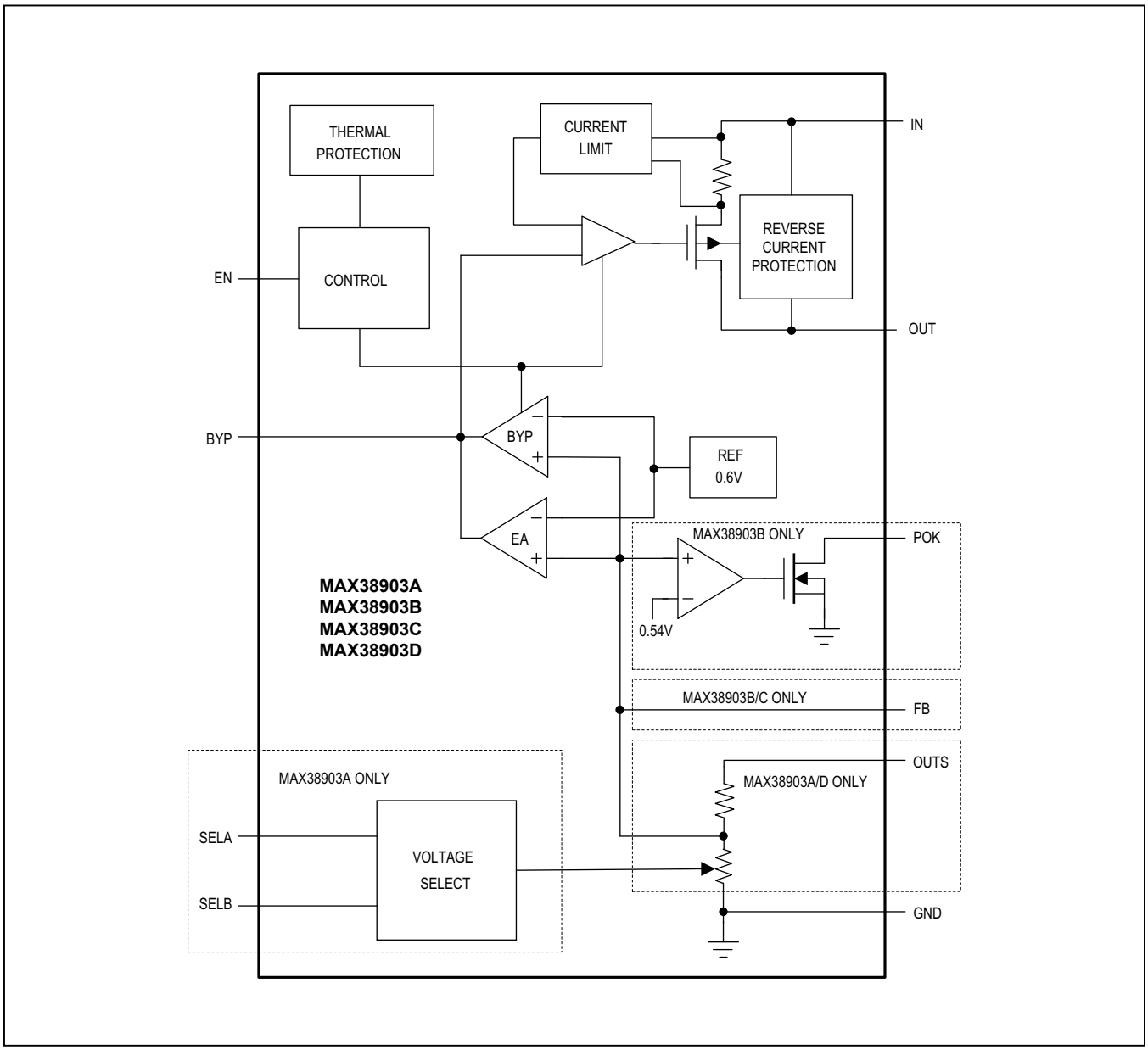


Figure 4. MAX38903D Pin Configuration

Pin Description

PIN				NAME	FUNCTION
MAX38903A	MAX38903B	MAX38903C	MAX38903D		
1, 2	1, 2	A1, A2	A1, A2	IN	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V and bypass with a 10µF capacitor from IN to GND.
3	3	B1, B2	B1, B2	GND	Regulator Ground. Bring IN and OUT bypass capacitor GND connections to this pin for best performance.
4	4	A3	A3	EN	Enable Input. Connect this pin to a logic signal to enable (V_{EN} high) or disable (V_{EN} low) the regulator output. Connect to IN to keep the output enabled whenever a valid supply voltage is present.
5	—	—	—	SELA	Select Input A. Connect to GND, IN, or leave unconnected to select the output voltage. This pin is read only at startup
—	5	—	—	GS	Ground Sense. Connect GS to GND.
6	—	—	—	SELB	Select Input B. Connect to GND, IN, or leave unconnected to select the output voltage. This pin is read only at startup
—	6	—	—	POK	Active-High Power-OK Output. Connect a pullup resistor from this pin to a supply to create a reset signal that goes high after the regulator output has reached its regulation voltage.
7	—	—	B3	OUTS	Output Voltage Sense Input. Connect to the load at a point where accurate regulation is required to eliminate resistive metal drops.
—	7	B3	—	FB	Feedback Divider Input. Connect a resistor divider string from OUT to GND with the midpoint tied to this pin to set the output voltage. In the *Typical Operating Circuits*, V_{OUT} = 0.6V x (1 + R1/R2).
8	8	C3	C3	BYP	Bypass Capacitor Input. Connect a 0.001µF to 0.1µF capacitor between OUT and BYP to reduce output noise and set the regulator soft-start rate.
9, 10	9, 10	C1, C2	C1, C2	OUT	Regulator Output. Sources up to 1A at the output regulation voltage. Bypass with a 10µF (4µF minimum, including voltage derating) low ESR (< 0.03Ω) capacitor to GND.
EP	EP	—	—	EP	Exposed Pad (TDFN Only). Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heatsinking.

Simplified Functional Diagram



Detailed Description

The MAX38903A/B/C/D low noise linear regulators deliver up to 1A of output current with only 7μV_{RMS} of output noise in a 10Hz to100kHz bandwidth. These regulators maintain their output voltage over a wide input range, requiring only 100mV of input-to-output headroom at full load.

The MAX38903A/B/C/D maintains a low 1200µA (typ) supply current, independent of the load current and dropout voltage. The regulator control circuitry includes a programmable soft-start circuit, short-circuit, reverse input current, and thermal overload protection. Other features include an enable input and power-ok (POK) output (MAX38903B only). See *Simplified Functional Diagram*.

Enable (EN)

The MAX38903A/B/C/D include an enable input (EN). Pull EN low to shut down the output, or drive EN high to enable the output. If a separate shutdown signal is not available, connect EN to IN.

Bypass (BYP)

The capacitor connected from BYP to OUT filters the noise of the reference, feedback resistors and regulator input stage, and provides a high-speed feedback path for improved transient response. A 0.01µF capacitor rolls-off input noise at around 32Hz.

The slew rate of the output voltage during startup is also determined by the BYP capacitor. A 0.01µF capacitor sets the slew rate to 5V/ms. This startup rate results in a 50mA slew current drawn from the input at start-up to charge the 10µF output capacitance.

The BYP capacitor value can be adjusted from 0.001µF to 0.1µF to change the startup slew rate according to the following formula:

$$\text{Startup Slew Rate} = (5V/ms) \times (0.01\mu F/C_{BYP})$$

where C_{BYP} is in µF.

Note that this slew rate applies only at startup. Recovery from a short-circuit will occur at a slew rate approximately 500 times slower.

Also note that, being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Protection Features

The MAX38903A/B/C/D are fully protected from an output short-circuit by a current-limiting and thermal overload circuit. If the output is shorted to GND, the output current is limited to 1.4A (typ). Under these conditions, the part quickly heats up. When the junction temperature reaches 165°C, a thermal limit circuit shuts off the output device. When the junction cools to 150°C, the output turns back on in an attempt to reestablish regulation. While the fault persists, the output current cycles on and off as the junction temperature slews between 150°C and 165°C.

The MAX38903A/B/C/D are also protected against reverse current when the output voltage is higher than the input. In the event that extra output capacitance is used at the output, a power-down transient at the input would normally cause a large reverse current through a conventional regulator. The MAX38903A/B/C/D include a reverse voltage detector that trips when IN drops 10mV below OUT, shutting off the regulator and opening the pMOS body diode connection, preventing any reverse current.

Output Voltage Configuration (MAX38903A)

The MAX38903A output can be set to one of nine voltages by shorting or opening the SELA and SELB inputs, as shown in Table 1. SELA and SELB should be connected to GND, IN, or left unconnected. Alternatively, they may be driven high, low, or open with external logic. However, the states of SELA and SELB are sampled only at startup. The regulation voltage can be set to a different level by cycling EN or IN momentarily to GND.

Table 1. MAX38903A Output Configuration

V_{OUT} (V)	SELA STATE	SELB STATE
1.2	Unconnected	IN
1.5	IN	Unconnected
1.8	Unconnected	GND
2.5	Unconnected	Unconnected
3.0	GND	GND
3.1	GND	IN
3.3	GND	Unconnected
4.0	IN	GND
5.0	IN	IN

Output Voltage Configuration (MAX38903B/C)

The MAX38903B and MAX38903C use external feedback resistors to set the output regulation voltage, as shown in the *Typical Operating Circuits*. The output can be set from 0.6V to 5.0V. Set the lower feedback resistor R2 to 300kΩ or less to minimize FB input bias current error. Then calculate the value of the upper feedback resistor R1, as follows:

$$R1 = R2 * \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} is the feedback regulation voltage of 0.6V. To set the output voltage to 2.5V, for example, R1 should be:

$$R1 = 300k\Omega * \left(\frac{2.5V}{0.6V} - 1\right) = 950k\Omega$$

Output Voltage Configuration (MAX38903D)

The MAX38903D output voltage comes pre-programmed to values listed below. Additionally, any voltage between 0.7V and 5.0V in 50mV steps can be factory trimmed and special ordered.

Power-OK (MAX38903B)

The MAX38903B includes an additional open-drain output (POK) that goes high to indicate the output voltage is in regulation. Connect a pullup resistor from this pin to an external supply. During startup, POK stays low until the output voltage rises to 91%(typ) of its regulation level. If an overload occurs at the output, or the output is shut-down, POK goes low.

Input Capacitor

A 10µF ceramic capacitor is recommended for the input. Select a capacitor that does not degrade significantly over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

Output Capacitor

A minimum of 4µF capacitance is required at OUT to ensure stability. Select a ceramic capacitor that maintains its capacitance (4µF minimum) over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

Thermal Considerations

The MAX38903A/B is packaged in an 10-pin 3mm x 3mm TDFN package with an exposed paddle. The exposed paddle is the main path for heat to leave the IC, and therefore must be connected to a ground plane with thermal vias to allow heat to dissipate from the device. Thermal properties of the IC package are given in the *Package Information* section.

Table 2. MAX38903D Output Voltage

PART NUMBER	V_{OUT} (V)
MAX38903D-07	0.7
MAX38903D-08	0.8
MAX38903D-10	1.0
MAX38903D-12	1.2
MAX38903D-15	1.5
MAX38903D-18	1.8
MAX38903D-20	2.0
MAX38903D-25	2.5
MAX38903D-27	2.7
MAX38903D-30	3.0
MAX38903D-33	3.3
MAX38903D-46	4.6
MAX38903D-50	5.0
MAX38903D__	*

**For other preprogrammed voltage selections, contact a Maxim Integrated representative.*

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX38903AATB+	-40°C to +125°C	10-pin TDFN 3mm x 3mm	9 Selectable Output Voltage, Enable, Reset Output
MAX38903BATB+	-40°C to +125°C	10-pin TDFN 3mm x 3mm	Resistor Configurable Output Voltage, Enable, Reset Output
MAX38903CANL+	-40°C to +125°C	9-bumps WLP 0.4mm pitch	Resistor Configurable Output Voltage, Enable
MAX38903DANL_ _+	-40°C to +125°C	9-bumps WLP 0.4mm pitch	Factory-Trimmed Option from 0.7V to 5.0V in 50mV Steps
MAX38903DANL27+	-40°C to +125°C	9-bumps WLP 0.4mm pitch	Factory Programmed to 2.7V

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	10/18	Updated *Front Page*, *Typical Operating Circuits*, Electrical Characteristics, and *Ordering Information* table	1–6, 11, 12
2	1/19	Updated *Package Information*, Table 2, and *Ordering Information*	3, 11, 12

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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