nanoPower Pushbutton On/Off Controller and Battery Freshness Seal

MAX16169

General Description

The MAX16169 is an extremely low-power, pushbutton, on/off controller with a switch debouncer and built-in latch. This device accepts a noisy input from a mechanical switch and produces a clean, latched output, and a one-shot interrupt output, in response to a switch closure exceeding the debounce period at PB_IN/$\overline{\text{PB\_IN}}$. A switch closure longer than the shutdown period at PB_IN/$\overline{\text{PB\_IN}}$ results in a longer one-shot interrupt output. The MAX16169 family has two sets of devices, one in which a more extended switch closure greater than the shutdown period deasserts the latched output, and another in which the latched output stays asserted. See *Table 1* for more information.

The MAX16169 operates from a supply range of +1.3V to +5.5V and consumes less than 40nA of supply current to ensure minimal battery drain in low-power applications, and to allow use as a battery "freshness seal". The robust switch input (PB_IN/$\overline{\text{PB\_IN}}$) accepts up to ±60V levels and is ±40kV ESD-protected for harsh environments. The latched output can serve as a logic signal to control a regulator or as a switch to connect the load directly to the power supply when the load current is low, providing 200mA of output current with less than 30mV voltage drop. A separate $\overline{\text{INT}}$ output provides a system interrupt whenever a valid pushbutton signal is detected. An asynchronous $\overline{\text{CLR}}$ input allows an external signal to force the latched output to the off state.

The MAX16169 operates over the -40°C to +125°C temperature range and is available in a 2mm x 2mm 6-pin micro dual-flat no-leads (µDFN) package.

Applications

- Portable Medical Devices
- Portable Instruments
- Handheld Consumer Electronics
- Industrial Equipment
- Internet of Things (IoT) Devices
- Disposable Low-Power Electronics
- Asset Tracking Devices

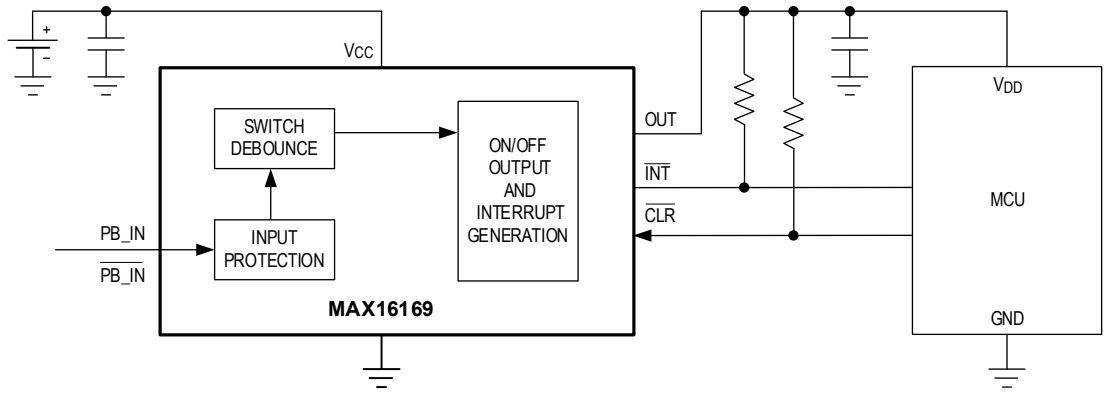
Benefits and Features

- Ultra Low Current Saves Power
  - 40nA (max) Standby Current (I_{SB})
  - V_{CC} Range: 1.3V to 5.5V
- Debounces Noisy Switches
  - 50ms and 2s Debounce Timing Options
  - 8s and 16s Shutdown Timing Periods
- Flexible Configurations Provide Design Options
  - Latched Output Supplies 200mA Load Current with Less Than 30mV Drop
  - One-shot $\overline{\text{INT}}$ Output on Each Switch Closure
  - 8ms, 32ms, 64ms, and 128ms $\overline{\text{INT}}$ Timing Options
  - Active-Low or Active-High Pushbutton Input
  - 2mm x 2mm 6-pin µDFN
- Robust Features Increases End Equipment Reliability
  - Pushbutton Input Handles up to ±60V
  - ±40kV Human-Body Model (HBM) Electrostatic Discharge (ESD) Protection

Ordering Information ***appears at end of data sheet.***

19-101732; Rev 0; 11/23

Typical Application Circuit



SWITCH DEBOUNCER/FRESHNESS SEAL PROVIDING POWER DIRECTLY TO LOAD

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Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6V

PB_IN/$\overline{PB\_IN}$ to GND ..... -60V to +60V

$\overline{CLR}$, $\overline{INT}$, OUT to GND..... -0.3V to +6V

Operating Temperature Range .....-40°C to +125°C

Junction Temperature .....+150°C

Storage Temperature Range.....-40°C to +150°C

Soldering Temperature (reflow).....+260°C

Continuous Power Dissipation (Multilayer Board)

6-µDFN (T_A = +70°C, derate 4.50mW/°C above +70°C) 357.8mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 µDFN

Package Code	L622+1C
Outline Number	*21-0164*
Land Pattern Number	*90-0004*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	223.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	122°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		1.3		5.5	V
Power Supply Current	I_{SB}	V_{CC} = 3.3V, OUT not asserted, PB_IN/$\overline{PB\_IN}$ not connected. -40°C ≤ T_A ≤ +70°C		2	40	nA
		V_{CC} = 3.3V, OUT not asserted, PB_IN/$\overline{PB\_IN}$ not connected. -40°C ≤ T_A ≤ +85°C		2	80	nA
Power Supply Current	I_{CC}	During PB_IN/$\overline{PB\_IN}$ detection or $\overline{INT}$ assertion		10	30	µA
	I_{SB_UVLO}	V_{CC} < 1.3V, I_{OUT} = 0, PB_IN/$\overline{PB\_IN}$ not connected, $\overline{CLR}$ not asserted		1	5	µA
Timing Accuracy		Deviation from the nominal value of debounce time (t_{DB}), shutoff time (t_{SO}), and interrupt time (t_{INT})	-20	±5	+20	%
Input High Voltage	V_{IH}	$\overline{CLR}$ and PB_IN/$\overline{PB\_IN}$, V_{CC} = 2.7V to 5.5V	70			%V_{CC}
		$\overline{CLR}$ and PB_IN/$\overline{PB\_IN}$, V_{CC} = 1.3V to 2.7V	80			%V_{CC}
Input Low Voltage	V_{IL}	$\overline{CLR}$ and PB_IN/$\overline{PB\_IN}$			30	%V_{CC}
Minimum Input High Time Detected		PB_IN		50		ms
Minimum Input Low Time Detected		$\overline{PB\_IN}$		50		ms
PB_IN/$\overline{PB\_IN}$ Hysteresis				100		mV
PB_IN Pulldown Resistance		0 < V_{PB_IN} < V_{CC}	1000	1400	2000	kΩ
$\overline{PB\_IN}$ Pullup Resistance		0 < $V_{\overline{PB\_IN}}$ < V_{CC}	1000	1400	2000	kΩ
PB_IN/$\overline{PB\_IN}$ Input Current	I_{IN}	V_{PB_IN} = ±60V $V_{\overline{PB\_IN}}$ = ±60V	-170		+170	µA
PB_IN/$\overline{PB\_IN}$ Voltage Range		Continuous; 0V ≤ V_{CC} ≤ 5V	-60		+60	V
		Transient; 0V ≤ V_{CC} ≤ 5.5V	-60		+60	V
$\overline{CLR}$ Input Current	I_{CLR}		-10	±1	+10	nA
$\overline{CLR}$ Falling Edge to OUT Low Propagation Delay	t_{CO}	R_L = 10kΩ, C_L = 100pF		200		ns
$\overline{CLR}$ Lockout Time		The period following the rising edge of OUT during which transitions on $\overline{CLR}$ are ignored	1.6 x t_{INT}	2 x t_{INT}	2.4 x t_{INT}	ms
OUT Output Voltage	V_{OL}	V_{CC} = 3.3V, I_{SINK} = 1.6mA			0.4	V
		V_{CC} = 1.3V, I_{SINK} = 200µA			0.2	V

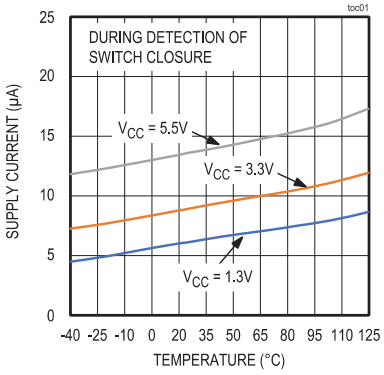
(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT Output Voltage	V_{OH}	V_{CC} = 3.3V, I_{SOURCE} = 200mA	V_{CC} – 0.03			V
		V_{CC} = 2.0V, I_{SOURCE} = 2mA	V_{CC} – 0.01			
		V_{CC} = 1.3V, I_{SOURCE} = 500uA	V_{CC} – 0.01			
$\overline{INT}$ Output Voltage	V_{OL_INT}	V_{CC} = 3.3V, I_{SINK} = 1mA			0.2	V
		V_{CC} = 1.3V, I_{SINK} = 200µA			0.2	
$\overline{INT}$ Leakage Current			–10	±1	+10	nA
Interrupt Pulse Duration	t_{INT}	Beginning at t_{DB}	25.6	32	38.4	ms
		Beginning at the end of t_{SO}	102.4	128	153.6	
PB_IN/$\overline{PB\_IN}$ ESD Protection		Human Body Model		±40		kV

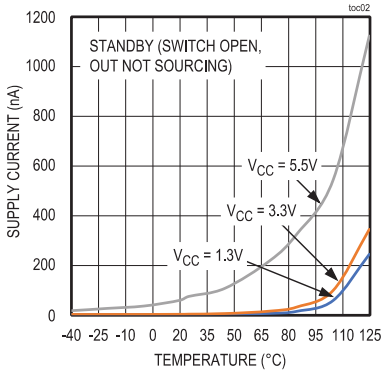
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

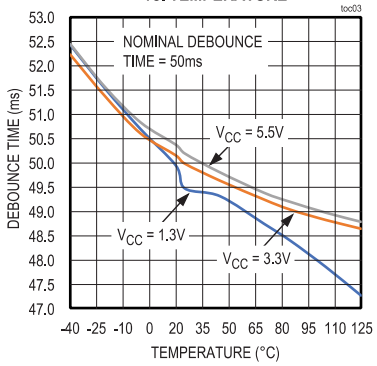
SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE



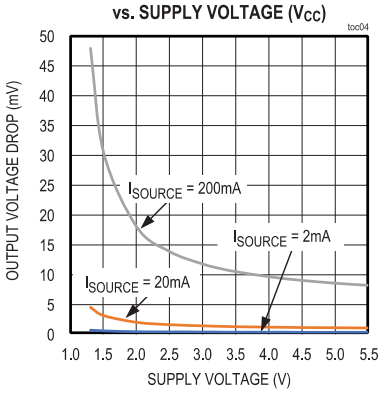
SUPPLY CURRENT (I_{SB}) vs. TEMPERATURE



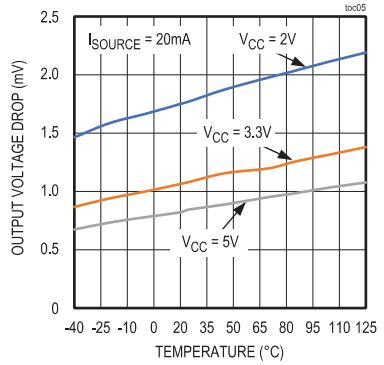
DEBOUNCE TIME (t_{DB}) vs. TEMPERATURE



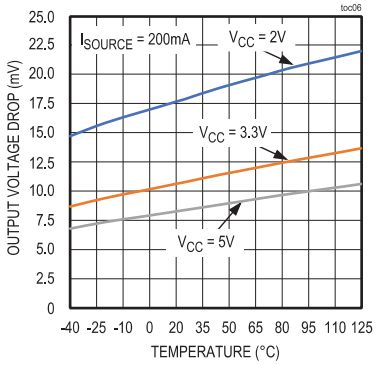
OUT VOLTAGE DROP vs. SUPPLY VOLTAGE (V_{CC})



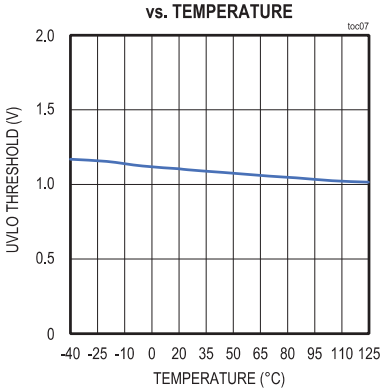
OUT VOLTAGE DROP vs. TEMPERATURE



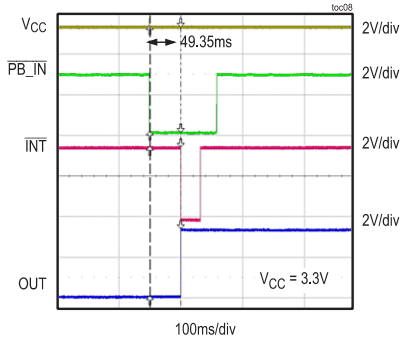
OUT VOLTAGE DROP vs. TEMPERATURE



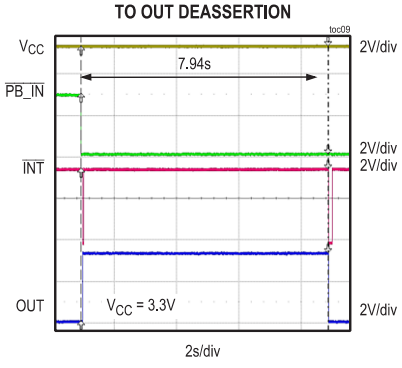
UVLO THRESHOLD vs. TEMPERATURE



MAX16169 SWITCH DEBOUNCE TO OUT ASSERTION

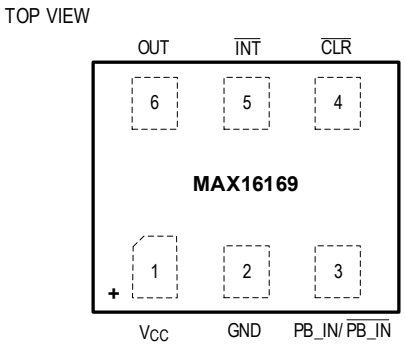


MAX16169 SWITCH DEBOUNCE TO OUT DEASSERTION



Pin Configurations

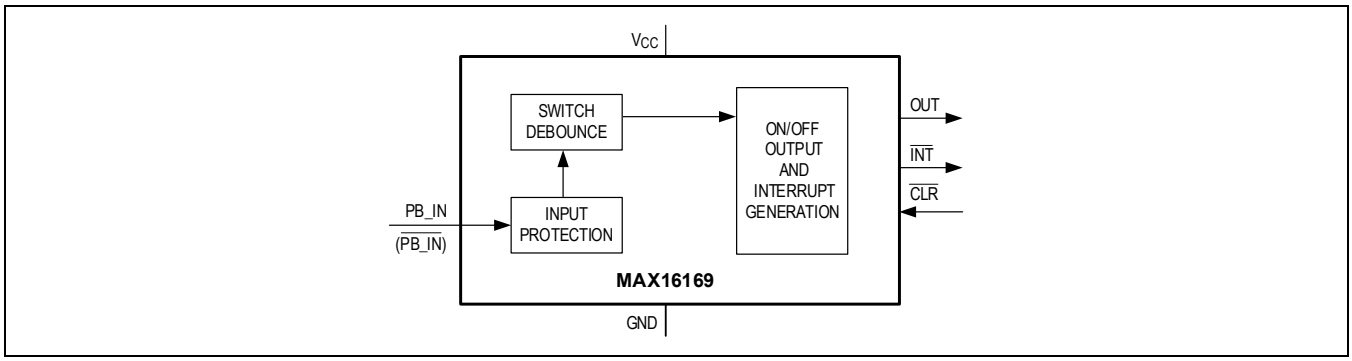
6 µDFN



Pin Descriptions

PIN	NAME	FUNCTION
1	V_{CC}	Power Supply Input. Bypass with a 0.1µF capacitor to ground.
2	GND	Ground
3	PB_IN/ $\overline{PB\_IN}$	Pushbutton Input. $\overline{PB\_IN}$ is internally pulled up to V_{CC}. Holding $\overline{PB\_IN}$ low for a period greater than the debounce time (t_{DB}) forces OUT to latch high and generates a one-shot pulse at $\overline{INT}$. For the MAX16169, a $\overline{PB\_IN}$ switch closure longer than the shutdown period results in a longer one-shot pulse at $\overline{INT}$. With timing option A, MAX16169 deasserts the latched output when the switch closure period exceeds the shutdown period. With the timing option B/C, MAX16169 does not deassert the latched output.
4	$\overline{CLR}$	Clear Input. Pulling $\overline{CLR}$ low deasserts the latched OUT signal. If OUT is already deasserted when $\overline{CLR}$ is pulled low, the state of OUT is unchanged.
5	$\overline{INT}$	Active-Low, Open-Drain Interrupt/Reset Output. $\overline{INT}$ is a one-shot output pulse. $\overline{INT}$ asserts for the interrupt timeout period when PB_IN is held high ($\overline{PB\_IN}$ is held low) for a period greater than the debounce time (t_{DB}). $\overline{INT}$ is high-impedance when deasserted, even when pulled above V_{CC}.
6	OUT	Active-High, Push-Pull Latched Output. OUT is connected to V_{CC} when high.

Block Diagram



Detailed Description

The MAX16169 is a pushbutton on/off controller with a switch debouncer and latched output for controlling system power. A switch closure that pulls PB_IN high ($\overline{PB\_IN}$ low) and is stable for a period greater than or equal to the debounce time (t_{DB}) causes OUT to assert high. Driving $\overline{CLR}$ low causes OUT to deassert. The MAX16169 family has two sets of devices, one in which a more extended switch closure greater than the shutdown period deasserts the latched output, and another in which the latched output stays asserted. Each debounced switch closure also initiates a one-shot $\overline{INT}$ output. See *Table 1* for more details on the values of t_{DB}, t_{SO}, and other timing intervals.

Table 1. MAX16169 Input Timing Characteristics

TIMING OPTION*	DEBOUNCE TIME (t_{DB})	SHUTDOWN PERIOD (t_{SO})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{DB})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{SO})	SWITCH CLOSURE > t_{SO}
A	50ms	8s	32ms	128ms	OUT deasserts
B	2s	16s	32ms	128ms	OUT stays asserted
C	50ms	16s	32ms	128ms	OUT stays asserted

**Contact the factory for availability.*

Operation

The MAX16169 operates from supply voltages between +1.3V and +5.5V, consuming less than 40nA of supply current when OUT is in the deasserted state, and PB_IN/$\overline{PB\_IN}$ is unconnected. Whenever OUT is deasserted, the state of $\overline{CLR}$ is ignored. After asserting OUT, $\overline{CLR}$ continues to be ignored for a period of 2x the $\overline{INT}$ period. For low-power applications (up to about 200mA output current), OUT can drive the load directly with minimal voltage drop. Each debounced switch closure causes $\overline{INT}$ to assert. A switch closure that is longer than t_{SO} results in $\overline{INT}$ asserting for a period that is 4x longer than the nominal $\overline{INT}$ period. This longer $\overline{INT}$ can be used to signal the system to perform a specific function or initiate a shutdown process. Closing the switch for a time longer than this extended $\overline{INT}$ period will not cause $\overline{INT}$ to be reasserted or the $\overline{INT}$ period to be extended.

Note that when V_{CC} is first applied (for example, when the battery is initially installed), OUT is deasserted.

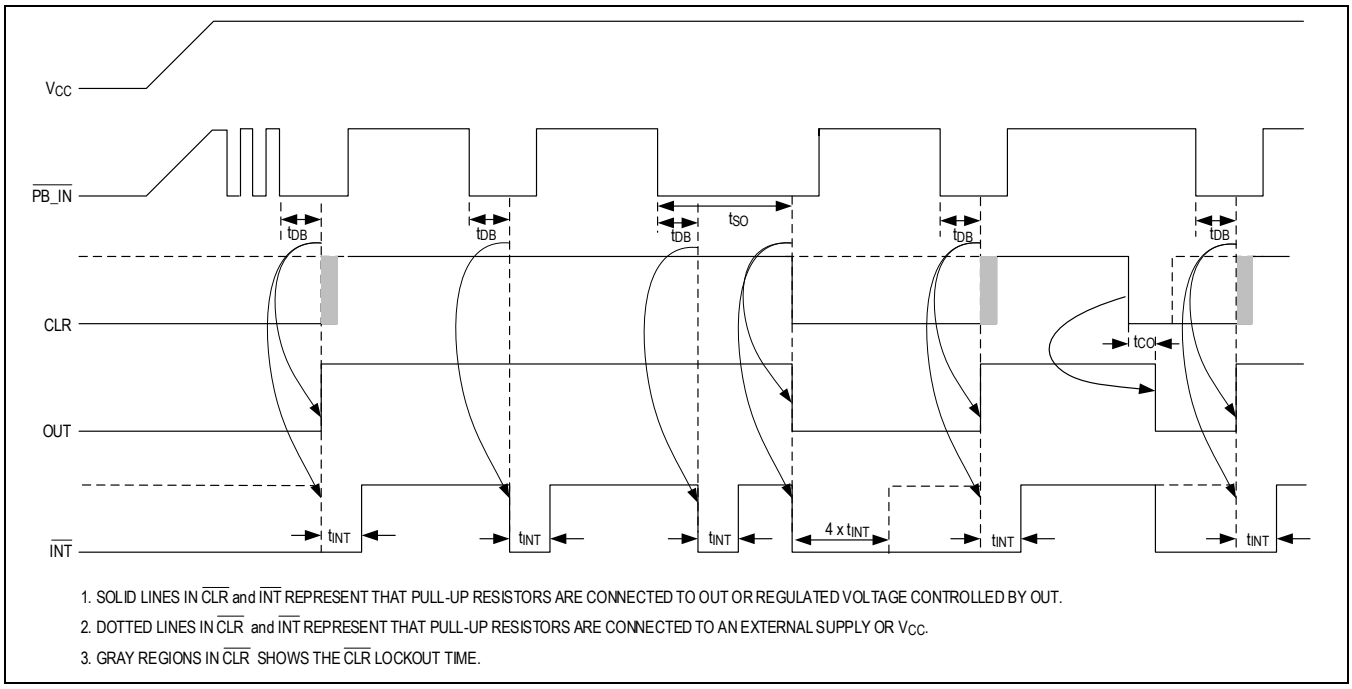


Figure 1. MAX16169 Timing Diagram with Long Pushbutton (t_{SO}) Causes Out to Deassert ($\overline{PB\_IN}$ input example)

Very brief high periods (less than approximately 50ms) at PB_IN/$\overline{PB\_IN}$ are ignored so that fast switch bounces do not interrupt the debounce logic, while valid short presses and releases cause the debouncer to reset. *Figure 1* shows the timing diagram of the MAX16169 with timing option A. A switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} causes OUT to deassert and an extended interrupt at $\overline{INT}$. Typically, $\overline{INT}$ and $\overline{CLR}$ are pulled up either to OUT or to a regulated voltage controlled by OUT, as shown in *Figure 1*. As such, $\overline{INT}$ and $\overline{CLR}$ are pulled low while OUT is deasserted. If pulled up to a constant supply voltage, $\overline{INT}$ and $\overline{CLR}$ will behave as shown by the horizontal dashed lines while OUT is deasserted.

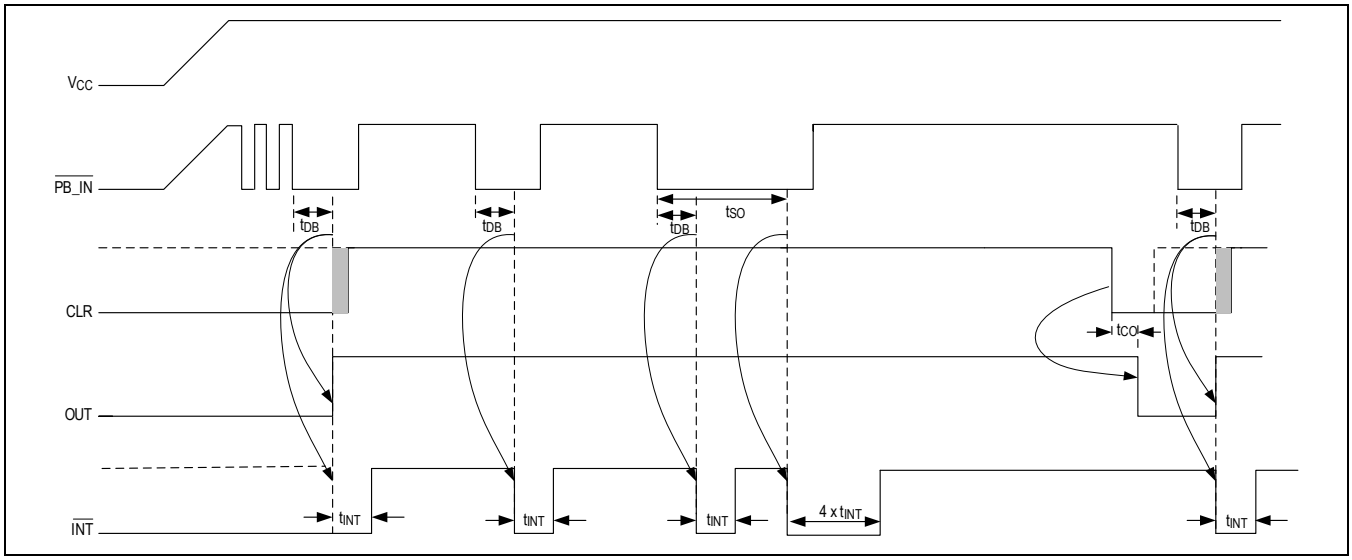


Figure 2. MAX16169 Timing Diagram with Long Pushbutton (t_{SO}) Keeps OUT Asserted ($\overline{PB\_IN}$ input example)

Figure 2 shows the timing diagram for the MAX16169 with timing option B/C. A switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} does not cause OUT to deassert, but it causes an extended interrupt. Typically, $\overline{INT}$ and $\overline{CLR}$ are pulled up either to OUT or to a regulated voltage controlled by OUT, as shown in *Figure 2*. As such, $\overline{INT}$ and $\overline{CLR}$ are pulled low while OUT is deasserted. If pulled up to a constant supply voltage, $\overline{INT}$ and $\overline{CLR}$ will behave as shown by the horizontal dashed lines while OUT is deasserted.

Robust Switch Input

The switch input (PB_IN/$\overline{PB\_IN}$) has overvoltage clamping diodes to protect against damaging fault conditions. Switch input voltages can safely swing ±60V relative to ground.

±40kV ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX16169 has extra protection against static electricity to protect against ESD of ±40kV at the switch input without damage. ESD protection can be tested in various ways; this product is characterized for protection to ±40kV using the Human Body Model.

Human Body Model

Figure 3 shows the Human Body Model, while *Figure 4* shows the current waveform it generates when discharged into a low-impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

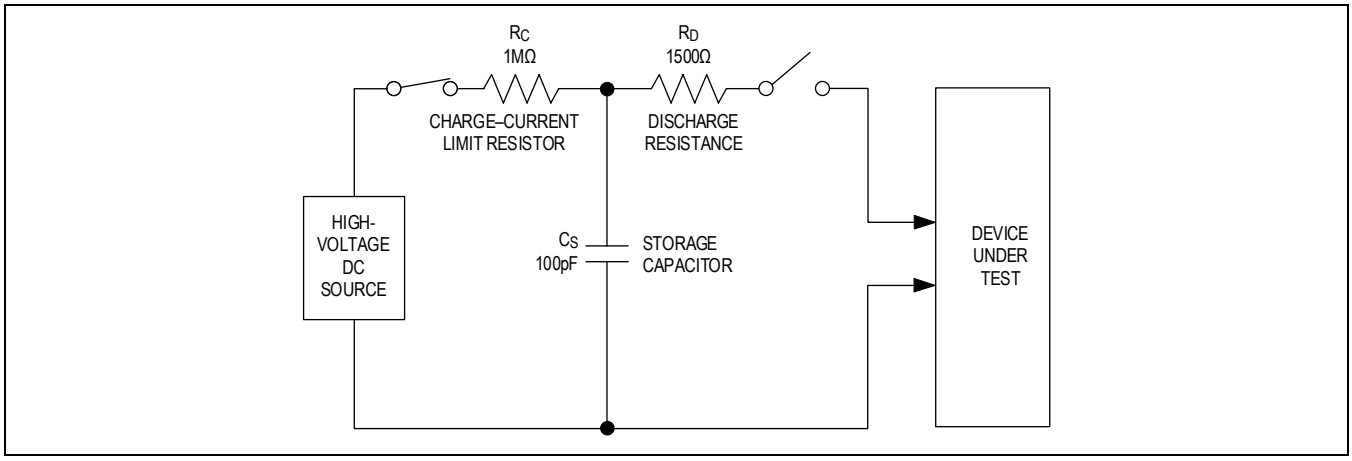


Figure 3. Human Body ESD Test Model

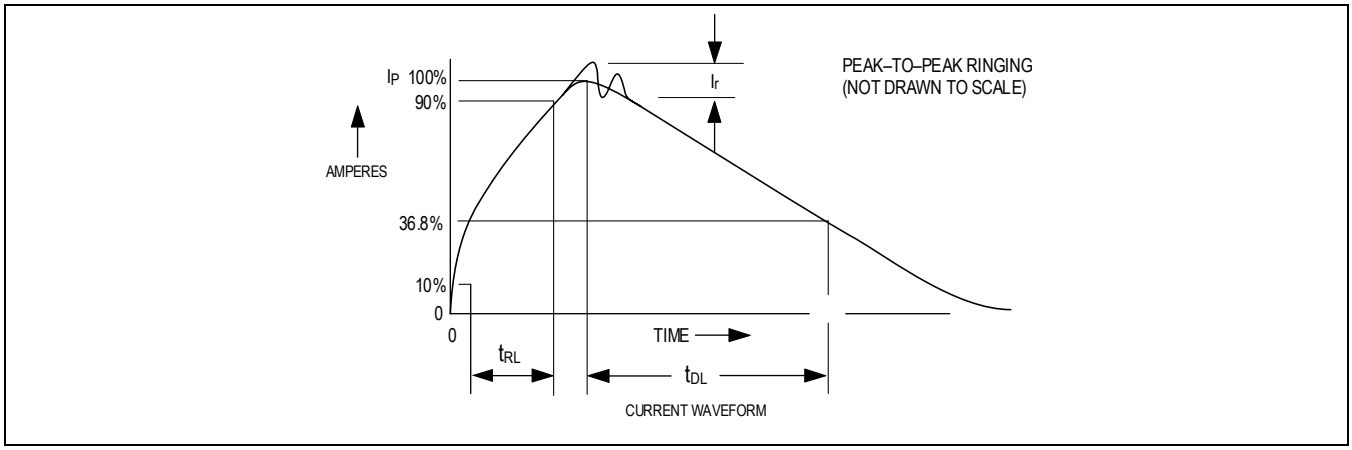


Figure 4. Human Body Current Waveform

Applications Information

Powering the Load

OUT is capable of driving most of the portable system loads. When the supply current of circuitry is 200mA, the voltage drop from V_{CC} to OUT is less than 30mV. The *Typical Application Circuit*, shows OUT providing power directly to the load.

Ordering Information

PART NUMBER	DEBOUNCE TIME (t_{DB})	SHUTDOWN PERIOD (t_{SO})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{DB})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{SO})	SWITCH CLOSURE > t_{SO}	PB POLARITY	PACKAGE
MAX16169AALTA+/ MAX16169AALTA+T	50ms	8s	32ms	128ms	OUT deasserts	$\overline{PB\_IN}$	µDFN

All devices are specified over the -40°C to +125°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and real

Contact the factory for the availability of future variants.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/23	Initial release	—