A²B Transceiver

AD2437

A²B BUS FEATURES

- Line topology
  - Single main node, up to 16 subordinate nodes
  - Up to 30 m between nodes and up to 300 m overall cable length
- Communication over distance
  - Synchronous data
    - Multichannel I²S/TDM to I²S/TDM
    - Clock synchronous, phase aligned in all nodes
    - Low latency node to node communication
  - Control and status information I²C to I²C
  - GPIO over distance
- Bus power or local power subordinate nodes
- Configurable with SigmaStudio+ graphical software tool

BASELINE A²B TRANSCEIVER FEATURES

- Configurable as A²B bus main node or subordinate node
- Programmable via I²C and SPI interfaces
- 8-bit to 32-bit multichannel I²S/TDM interface
  - I²S/TDM/PDM programmable data rate
  - Up to 51 channels of 16-bit data or 32 channels of 24-bit data between nodes
- PDM inputs for up to 4 high dynamic range microphones on main or subordinate nodes
- Support for receiving I²S/TDM and PDM data on the same node
- Unique ID register for each transceiver
- Support for crossover or straight-through cabling

AD2437 TRANSCEIVER ENHANCEMENTS

- Mixed Signal
  - ADC monitoring of supply voltages
  - Supports 3.3 V input at VIN in Low Voltage Input (LVI) mode
- Digital
  - High speed SPI (up to 10 Mbps) over distance
  - Dedicated hardware reset pin
  - I²S/TDM crossbar switch
    - Flexible mapping of Tx/Rx TDM channel data to A²B slot
  - Support for I²C fast mode plus (1 MHz)
  - Support for LED lighting control using 4 PWM outputs
  - 8 GPIO pins with configurable pin mapping

APPLICATIONS

- Conference room transducer nodes
- Musical instrument connectivity
- Distributed audio systems
- Personal audio zones

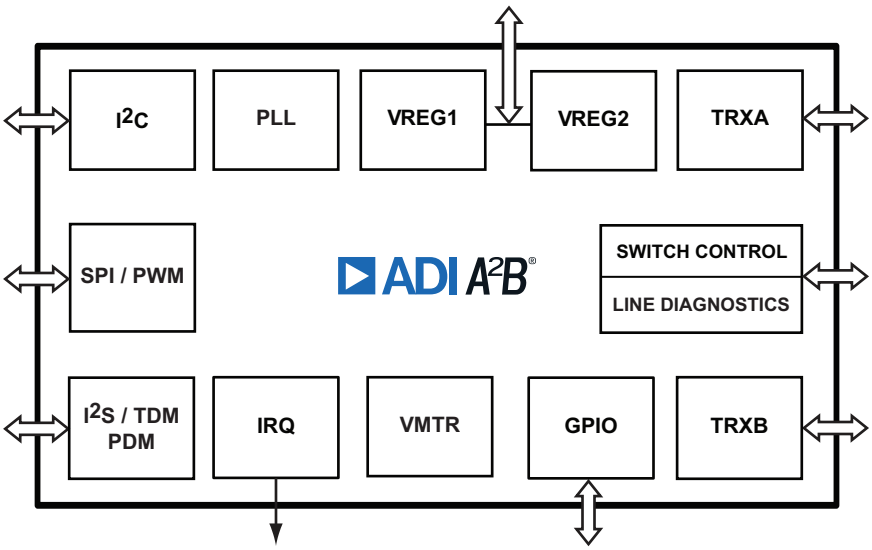

Figure 1. Functional Block Diagram

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REVISION HISTORY

7/2023—Revision 0: Initial Version

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

GENERAL DESCRIPTION

The AD2437 A²B® transceiver provides a multichannel, I²S/TDM link over distances of up to 30 m between nodes. It embeds bidirectional synchronous pulse-code modulation (PCM) data (for example, digital audio), clock, and synchronization signals onto a single-pair differential cable. A²B supports a direct point to point connection and allows multiple, daisy-chained nodes at different locations to contribute and/or consume time division multiplexed channel content.

A²B is a single main node, multiple subordinate node system where the transceiver at the host controller is the main node. The main node generates clock, synchronization, and framing for all subordinate nodes. The main A²B transceiver is programmable over a control port (I²C/SPI) for configuration and read back. An extension of the control port protocol is embedded in the A²B data stream. This allows direct access to registers and status information on subordinate transceivers, as well as I²C to I²C, SPI to I²C, or SPI to SPI communication from the host to a peripheral in a subordinate node. SPI to SPI communication between subordinate nodes can be performed directly and does not need to involve the main node.

The transceiver can connect directly to general-purpose digital signal processors (DSPs), field-programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), digital microphones, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and codecs through a multichannel I²S/TDM interface. It also provides a pulse density modulation (PDM) interface for direct connection of up to four PDM digital microphones.

The transceiver supports a bus power feature, where the main node supplies voltage and current to the subordinate nodes over the same daisy-chained, single-pair wire or XLR/DMX cable as used for the communication link.

The transceiver also supports a broad spectrum of Ethernet cables in which the A²B occupies only one pair of a category (CAT) cable. This frees up the remaining CAT cable pairs for power delivery.

Table 1. Product Features

Feature	AD2437
Main node capable	Yes
Functional TRX blocks	A + B
I²S/TDM support	Yes
PDM microphone inputs	4 mics
A²B bus power	Up to 50 W
Nominal bus bias voltage (VBUS)	24 V
SPI over distance	Yes
Power configuration	CFG-4

A²B BUS DETAILS

Figure 2 shows a single main node, multiple subordinate node A²B communications system with the main transceiver controlled by the host. The host generates a periodic synchronization signal on the I²S/TDM interface at a fixed frequency (typically 48 kHz) to which all A²B nodes synchronize.

Communications along the A²B bus occur in periodic superframes. The superframe frequency is the same as the synchronization signal frequency, and data is transferred at a bit rate that is 1024 times faster (typically 49.152 MHz). Each superframe is divided into periods of downstream transmission, upstream transmission, and no transmission (where the bus is not driven). Data is exchanged over the A²B bus in equal width slots for both upstream and downstream transmissions. Up to 32 bidirectional slots can be configured at 24 bits, while up to 51 slots can be configured at 16 bits.

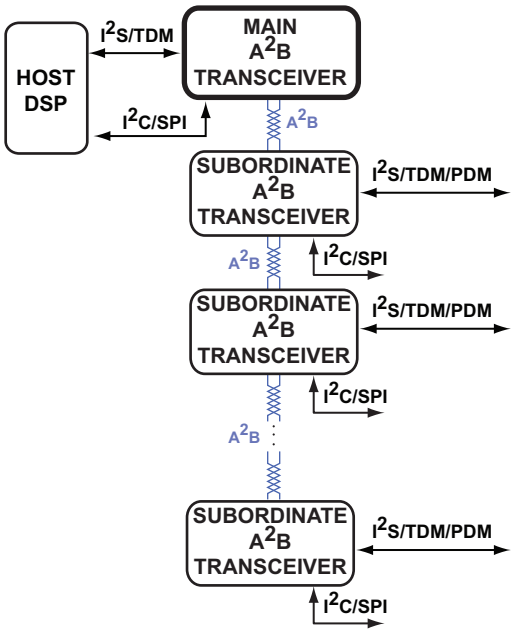


Figure 2. Communication System Block Diagram

The A²B bus also communicates the following control and status information between nodes:

- I²C to I²C or SPI to I²C/SPI communication
- General-purpose input/output (GPIO)
- Interrupts

In Figure 3, a superframe is shown with an initial period of downstream transmission and a later period of upstream transmission.

All signals on the A²B bus are line coded, and the main node forwards the synchronization signal downstream from the main transceiver to the last subordinate node transceiver in the form

of a synchronization preamble. This preamble is followed by control data to build a synchronization control frame (SCF). Downstream, TDM synchronous data and SPI tunnel data are added directly after the control frame. Every subordinate node can use or consume some of the downstream data and add data for downstream nodes. The last subordinate node transceiver responds after the response time with a synchronization response frame (SRF). Upstream TDM synchronous data and SPI tunnel data are added by each node directly after the response frame. Each node can also use or consume upstream data.

The embedded control and response frames allow the host to individually address each subordinate transceiver in the system. The host also enables access to remote peripheral devices that are connected to the subordinate transceivers via the I^2C or SPI ports for I^2C to I^2C, SPI to SPI, and SPI to I^2C communication over distance between multiple nodes.

All nodes in an A^2B system are sampled synchronously in the same A^2B superframe. Synchronous I^2S/TDM downstream data from the nodes arrives at all downstream subordinate nodes in the same A^2B superframe, and every node's upstream audio data arrives synchronously in the same I^2S/TDM frame at any upstream node. I^2S/TDM to I^2S/TDM communication over distance does not require involvement of the main node and can be performed directly between subordinate nodes. The remaining audio phase differences between subordinate nodes can be compensated for by register-programmable fine adjustment of the SYNC pin signal delay.

There is a sample delay incurred for data moving between the A^2B bus and the I^2S/TDM interfaces because data is received and transmitted over the I^2S/TDM every sample period (typically 48 kHz). This timing relationship between samples over the A^2B bus is shown in Figure 4. It shows the data transfer between the main node and a subordinate node, but would be similar for data transfer between any two subordinate nodes as well.

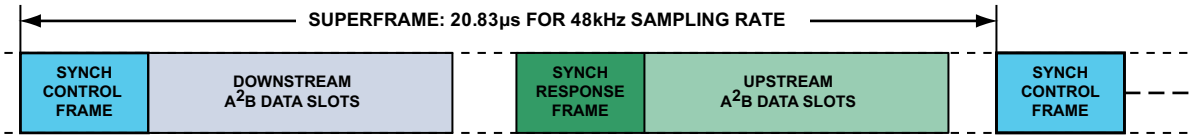


Figure 3. A^2B Superframe

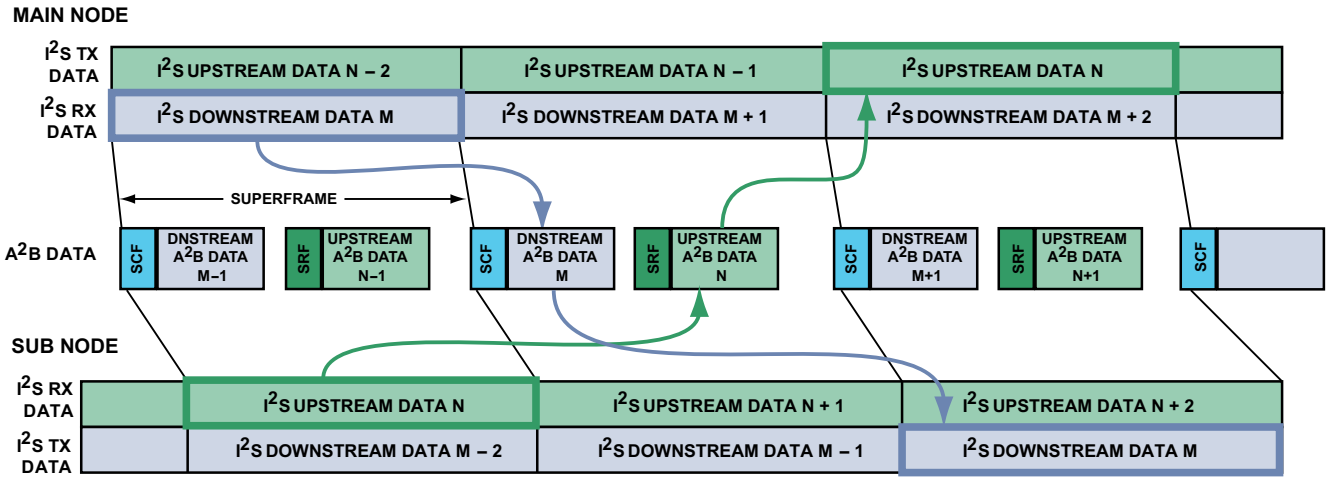


Figure 4. A^2B Bus Synchronous Data Exchange

Note in Figure 4, both downstream and upstream samples are named for the frame where they enter the A²B system as follows:

- I²S/TDM data received by the main node transceiver in superframe M creates downstream data M and is transmitted over the A²B bus in the next superframe.
- I²S/TDM data received by the subordinate node transceivers in superframe N creates upstream data N and is transmitted over the A²B bus in the next superframe.
- Data received via the A²B bus is transmitted on the I²S/TDM interface of an A²B transceiver in the following superframe.
- Data transmitted across the A²B bus (from any node to any node) has two frames of latency plus any internal delay that has accumulated in the transceivers, as well as delays due to wire length. Therefore, overall latency is slightly over two samples (<50 µs at 48 kHz sample periods) from the I²S/TDM interface in one A²B transceiver to the I²S/TDM interface of another A²B transceiver.

To support and extend the A²B bus functions and performance, the transceivers have additional features, as described in the following sections.

I²C INTERFACE

The I²C interface in the transceiver provides access to the internal registers. It has the following features:

- Target functionality in the A²B main node
- Controller or target functionality in the A²B subordinate node
- Multi-controller support in the A²B subordinate node
- 100 kbps, 400 kbps, or 1Mbps rate operation
- 7-bit addressing
- Single-word and burst mode read and write operations
- Clock stretching

All transceivers can be accessed by a locally connected processor using the 7-bit I²C device address (BASE_ADDR) established by the logic levels applied to the ADR2 and ADR1 pins at power-on reset, thus providing for up to four I²C controller devices connecting to the same I²C bus. A subordinate configured transceiver recognizes only this I²C device address. A main configured transceiver, however, also recognizes a second I²C device address for remote access to subordinate nodes and remote peripherals over the A²B bus (BUS_ADDR). The least significant bit (LSB) of the 7-bit device address determines whether an I²C data exchange uses the BASE_ADDR (bit 1 = 0) to access the local transceiver or BUS_ADDR (bit 1 = 1) to access a bus node subordinate transceiver and remote peripherals through a main configured transceiver. See the *AD2437 A²B Transceiver Technical Reference* for details.

I²S/TDM INTERFACE

The I²S/TDM serial port operates in full-duplex mode, where both the transmitter and receiver operate simultaneously using the same critical timing bit clock (BCLK) and synchronization (SYNC) pins. A²B main transceivers receive the timing signals from BCLK and SYNC pins driven by the host device. A²B subordinate transceivers generate the timing signals on the BCLK and SYNC output pins. The I²S/TDM port features:

- Programmable clock and frame sync timing and polarity
- Numerous TDM operating modes
- 16- or 32-bit data width
- I²S TX/RX crossbar to associate specific TDM data channels with specific A²B slots
- Simultaneous operation with PDM port

The I²S/TDM/PDM port includes five programmable data pins (SIO0-SIO4) which can be configured to exchange any combination of up to two PDM streams (SIO0/1 only) and up to five I²S/TDM streams, with a maximum of four I²S/TDM streams in the same direction (see Table 2).

Table 2. SIO Pin Mapping[1]

	A2B_PDMCTL.PDM1EN /PDM0EN			
Pin	**00**	**01**	**10**	**11**
SIO0	DRX0	PDM0	DRX0	PDM0
SIO1	DRX1, DTX3	DRX0, DTX3	PDM1	PDM1
SIO2	DRX2, DTX2	DRX1, DTX2	DRX1, DTX2	DRX0, DTX2
SIO3	DRX3, DTX1	DRX2, DTX1	DRX2, DTX1	DRX1, DTX1
SIO4	DTX0	DTX0	DTX0	DTX0

[1] Pin mapping of I²S/TDM DTXn and DRXn depends on A2B_PDMCTL and A2B_I2SCFG registers. See the *AD2437 A²B Transceiver Technical Reference* for details on pin mappings.

I²S Reduced or Increased Rate

Subordinate transceivers can run the I²S/TDM/PDM interface at a reduced or increased rate frequency, with respect to the superframe rate. The reduced rate frequency is derived by dividing the superframe rate from a programmable set of values. The subordinate transceiver also supports increased sampling rates of 2× and 4× superframe rates (f_{SYNCM}). Each subordinate node transceiver can be configured to run at a different I²S/TDM rate.

In reduced rate mode, the transceiver provides an option for a processor to track the full rate audio frame, which contains new reduced rate samples. The GPIO7 pin can be used as a strobe, and the direction can be configured as an input or output.

PULSE DENSITY MODULATION (PDM) INTERFACE

PDM microphones can directly interface to the SIO0/1 pins of the A²B transceiver. The PDM block on the transceiver converts a PDM input stream into pulse code modulated (PCM) data for transmission over the A²B bus, to the local device through the I²S/TDM port, or both. The PDM interface is available on both main and subordinate transceivers. It supports high dynamic range microphones with high signal-to-noise ratio (SNR) and extended maximum sound pressure level (SPL). The output rate of the PDM demodulators is controllable at the superframe (SFF), SFF/2, or SFF/4 rates. In addition, reduced rate modes support frame rates of SFF/2, SFF/4, SFF/8, SFF/12, SFF/16, SFF/20, SFF/24, SFF/28, SFF/32, and SFF/128 (for example, down to 375 Hz for a superframe rate of 48 kHz).

The PDM block supports high pass filtering of the input with a selectable cut-off frequency including 1, 60, 120, and 240 Hz. A register setting selects whether rising edge data or falling edge data is sampled first.

On a subordinate node, either BCLK or GPIO7 can clock PDM microphones. If GPIO7 is the clock, the BCLK frequency can be set to a different frequency using the I²S/TDM registers. In this case, GPIO7 is the PDM clock (PDMCLK) capturing PDM input on SIO0/SIO1. The clock rate from PDMCLK is 64× the SYNC frequency. BCLK and GPIO7 can also work concurrently to clock PDM microphones at the same frequency and phase alignment, but with opposite polarity.

On a main node, BCLK is always an input, so the clock to PDM microphones attached to a main node typically come from GPIO7. It is possible to use BCLK to drive the PDM clock inputs on a main node, but this restricts the possible TDM settings because BCLK is required to fall within the specification in Table 8.

DATA SLOT EXCHANGE BETWEEN SUBORDINATE NODES

On the DTX pins of the I²S/TDM interface, subordinate transceivers can selectively output upstream data and downstream data that originates from other nodes without the need for data slots routed through the main node. Similarly, RX data channels from an I²S/TDM frame can become upstream and/or downstream slots on the A²B bus and can be received by any node.

I²S TX/RX CROSSBAR

The I²S crossbar provides flexible mapping between channels in the I²S/TDM interface and slots on the A²B bus.

When a node receives data over the A²B bus and sends it to the I²S/TDM interface, by default, there is a one-to-one mapping. For example, the first received slot is mapped to the first channel on the I²S/TDM interface, and so on. Using the I²S TX crossbar, the channels on the I²S/TDM interface can be reordered to map to an A²B bus slot for each TDM channel.

Similarly, when a node receives data from the I²S/TDM interface and sends it over the A²B bus, by default, all the received I²S/TDM channels (defined in the A2B_SLOT registers) are mapped one-to-one on the A²B bus. Using the I²S RX crossbar, the TDM channels can be individually selected to send data over A²B bus slots. For example, only TDM channels marked as valid are put onto the A²B bus and channels not in use are masked. See the *AD2437A²B Transceiver Technical Reference* for details.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI interface in the transceiver has the following features:

- Master or slave configurable
- Supports up to 3 slave-select outputs
- Up to 12.288 MHz operation
- Programmable clock phase (CPHA) and polarity (CPOL)
- Subordinate transceiver register access
- Local register access

SPI transactions take place between SPI ports of connected transceivers or between the SPI port and the I²C port of connected transceivers over the A²B bus. The transceiver provides the ability for SPI communication to occur over the A²B bus between multiple nodes in a system. The SPI interface is enabled by default and the transceiver is configured as an SPI slave. To use the alternative pin functionality, the SPI interface must be disabled by writing the value 0x02 to the A2B_SPICFG register.

SPI Over Distance

An SPI tunnel is an extension to the A²B protocol where SPI control and data are exchanged between A²B nodes using dedicated slots on the A²B bus. SPI tunnels are configured and allocated by the host. SPI over distance supports the following features:

- Full-duplex read/writes between master and slave
  - Up to 256 bytes of pipelined reads
  - Extended full-duplex mode with pipelined reads for more than 256 bytes of data
- Atomic SPI transfer
- Bulk SPI to SPI writes
- Extended bulk SPI writes

PULSE WIDTH MODULATION (PWM) INTERFACE

The PWM interface has the following features:

- Support for LED lighting control.The PWM output sends the clock at a fixed frequency and modulates the duty cycle (high/low time) for brighter or dimmer lights.
- Support for 3 PWM outputs and 1 output enable (OE) master dimmer. Each output rises on a different phase to limit instantaneous current draw.
- Two PWM frequency generators that can be programmed to frequencies 192 kHz, 96 kHz, 48 kHz, 24 kHz, 12 kHz, 3 kHz, 1.5 kHz, 750 Hz, 375 Hz, or 187.5 Hz.
- Supports independent blink rates of 0, 0.25, 0.5, 0.75, and 1.0 seconds (blink period) for PWM and OE channels with a blink duty cycle fixed at 50%.

The PWM block also supports a frequency hopping scheme. The PWM frequency hopper randomly selects frequencies from 187.5 Hz to 3 kHz to spread the PWM emissions over a range of frequencies.

The PWM outputs are shared with the SPI pins. Disable SPI functionality when PWM channels are enabled.

GPIO OVER DISTANCE

The transceiver supports general-purpose input/output (GPIO) communication over the A^{2}B bus between multiple nodes without host intervention after initial programming. The host is required only for initial setup of the GPIO bus ports. I/O pins of different nodes can be logically OR or AND gate combined.

MAILBOXES

The transceiver supports interrupt driven, bidirectional message exchange between I^{2}C/SPI controller devices (microcontrollers) at different subordinate nodes and the host connected to the main node transceiver using two dedicated mailboxes per subordinate node. The mailboxes can be used to customize handshaking among numerous nodes in a system to coordinate system events, such as synchronizing audio.

LINE DIAGNOSTICS

The line diagnostic block of the transceiver with XLR/DMX and CAT cables can detect mainly two types of fault conditions occurring on the A^{2}B bus. These include:

- Open wire fault (A^{2}B cable between nodes is disconnected or a node drops from the A^{2}B bus)
- Overcurrent condition

And, the line diagnostic block of the transceiver with a single-pair wire can detect, isolate, and indicate the following type of cable line faults occurring on the A^{2}B bus:

- Positive terminal of cable shorted to VBAT
- Positive terminal of cable shorted to ground
- Negative terminal of cable shorted to VBAT
- Negative terminal of cable shorted to ground
- Positive terminal of cable shorted to the negative terminal of the cable
- Open wire fault (A^{2}B cable between the node is disconnected or the node drops from the A^{2}B bus)
- Wrong port (adjacent A^{2}B nodes are not connected to the correct A^{2}B ports)
- Reverse wires (positive terminal of the cable at one node is connected to the negative terminal of the next node and conversely)
- Defective node (node is not responding)

These line faults are detected during and after discovery in the system run time. When a fault is detected during discovery, the switches that enable the bias current to the next-in-line node are disconnected automatically. The main node indicates the fault condition to the host controller via the interrupt (IRQ) pin. See the *AD2437 A^{2}B Transceiver Technical Reference* for details.

CLOCK SUSTAIN STATE

In the clock sustain state, audio signals of locally powered subordinate nodes are attenuated in the event of lost bus communication. When the bus loses communication and a reliable clock cannot be recovered by the subordinate node, the subordinate node transceiver enters the sustain state and, if enabled, signals this event on a GPIO pin.

In the clock sustain state, the phase-locked loop (PLL) of the subordinate transceiver continues to run for 1024 SYNC periods, while gradually attenuating the negative values to zero and the positive values to –109 dB on the enabled I^{2}S SIOn data pins. After the 1024 SYNC periods, the subordinate node transceiver resets and reenters the power-up state.

DEDICATED INTERRUPT

The transceiver features a dedicated interrupt pin (IRQ) to signal:

- Bit errors on the bus
- A line fault on the bus
- An interrupt from GP input pins
- Mailbox interrupts
- SPI and VMTR interrupts

Once the IRQ pin is asserted, the host controller checks the type and source of the interrupt. This pin can be configured active high or active low.

SUPPORT FOR PARALLEL A^{2}B BUSES

This feature allows for parallel A^{2}B buses to exist between nodes in a system, thereby doubling the possible A^{2}B bandwidth between two nodes. The parallel A^{2}B main nodes are I^{2}S targets and share BCLK and SYNC. On the A^{2}B subordinate node, one of the A^{2}B transceivers is configured as an I^{2}S target and the other remains the I^{2}S controller (default behavior). BCLK and SYNC are shared between the two A^{2}B bus subordinate nodes and any attached peripherals.

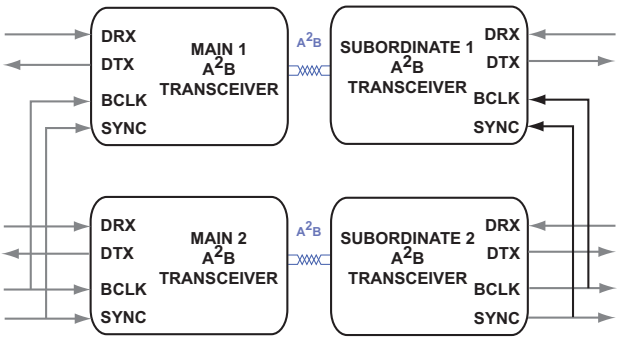


Figure 5. Parallel A²B Bus Diagram

VOLTAGE MONITOR (VMTR) ADC

The voltage monitor ADC is a multichannel successive approximation ADC. It allows software to monitor the health of key voltages on A²B bus nodes. The VMTR:

- Selectively monitors VIN, VBUS, DVDD, TRXVDD, and IOVDD supply voltages and high/low side downstream currents
- Features an on-chip analog front end that conditions input to the ADC
- Uses an internal reference voltage
- Features an option to enable interrupts based on a maximum and minimum threshold
- Provides measured voltages and interrupts that are available in the next superframe

POWER ON RESET

The transceiver remains in reset state until all the supplies (VIN, IOVDD, DVDD, and TRXVDD) are stable. Refer to Operating Conditions for chip reset assertion and deassertion voltage specifications.

HARDWARE RESET

The transceiver features a dedicated active low hardware reset pin to reset the device. The reset pin can be deasserted after all the power domains are stable, thereby eliminating the need for power-up sequencing.

LOW VOLTAGE INPUT (LVI) MODE

The transceiver supports a low voltage input mode in which VIN can be 3.3V. In this mode, only VOUT1 is available. VOUT2 must be connected to the VIN pin. In LVI mode, there is no restriction on VBUS—any voltage within the respective specified range can be used.

POWER CONFIGURATIONS

The transceiver supports one power configuration:

- CFG-4 — Supports up to 50 W depending on cable and connector configuration.

The operating power configuration of the transceiver can be identified by reading the A2B_SWSTAT2.HPSW_CFG_ DET bit field. With the single-pair cable configuration, an external NMOS is used on both the high side and low side to deliver power along each of the data wire to the sub node. When using the XLR/DMX cables, only one NMOS is used at the high side to send power over both the data wires. When using the RJ45 connector, only one NMOS is used at the high side to deliver power to the sub node, but over the non-data wire pairs of the 8P8C modular connector.

Refer to Table 1, Product Features, for the bus power capabilities.

STANDBY MODE

Standby is a low power mode in which only a minimal (19-bit) SCF exists to keep all of the subordinate node transceivers synchronized. There is no downstream or upstream data traffic on the A²B bus and there is no SRF field. Standby mode can be exited and system traffic can be resumed without the need for rediscovery of the A²B node transceiver again. The GPIO settings retain their values while the transceiver is in standby mode.

UNIQUE ID

Each transceiver contains a 5-byte unique ID, which can be read from registers using software.

SUPPORT FOR CABLING

By default, the A²B transceiver is configured for use with crossover cables with single-pair cables. Straight-through, single-pair cables can also be used by swapping the connections of the dc bias inductors at the connector side. With RJ45 connectors, it is recommended to use straight-through CAT cables (T568 wiring standard) with the A²B transceivers. Straight-through CAT cabling is enabled using a register programming feature that allows polarity reversal on the B-side transceiver. With XLR/DMX cables, standard 3-pin XLR/DMX cables are used.

Contact Analog Devices for the latest reference schematic detailing implementation.

ADDITIONAL INFORMATION

Contact Analog Devices to request the *AD2437 A²B Transceiver Technical Reference*, which provides detailed information about the AD2437 transceivers.

SPECIFICATIONS

Specifications are subject to change without notice. For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter		Conditions	Min	Nominal	Max	Unit
Power Supplies						
V_{DVDD}	Digital Core Logic Supply Voltage		1.70	1.90	1.98	V
V_{IOVDD}	Digital Input/Output (I/O) Supply Voltage	3.3 V I/O	3.00	3.30	3.63	V
		1.8 V I/O	1.70	1.90	1.98	V
V_{PLLVDD}	Phased-Locked Loops (PLL) Supply Voltage		1.70	1.90	1.98	V
V_{TRXVDD}	Transceiver Supply Voltage		3.00	3.30	3.45	V
V_{VIN}[1]	Input Supply Voltage	Normal Mode, LVI Mode = 0	3.7		9.0	V
		LVI Mode = 1 (VIN and VOUT2 are connected)	3.17		3.45	V
V_{VBUS}[2, 3, 4]	Bus Bias Supply Voltage		12.0		24.0	
VBUS System Operating Conditions						
$I_{VBUS\_SYS\_HP}$	Bus Current	V_{VBUS} = 12 V to 24 V			2.1	A
Digital I/O						
V_{IH}[5]	High Level Input Voltage	V_{IOVDD} = 1.98 V	0.7 × V_{IOVDD}			V
		V_{IOVDD} = 3.63 V	2.2			V
V_{IL}[5]	Low Level Input Voltage	V_{IOVDD} = 1.70 V			0.3 × V_{IOVDD}	V
		V_{IOVDD} = 3.00 V			0.8	V
V_{IH_I2C}[6]		V_{IOVDD} = 3.63 V, 1.98 V	0.7 × V_{IOVDD}			V
V_{IL_I2C}[6]		V_{IOVDD} = 3.00 V, 1.70 V			0.3 × V_{IOVDD}	V
CONSUMER GRADE						
T_J	Junction Temperature		0		105	°C
INDUSTRIAL GRADE						
T_J	Junction Temperature		–40		+105	°C

[1] V_{VIN} must be ≤ (V_{VBUS} + 0.6 V).
[2] Bus bias must be stable after discovery.
[3] Refer to Line Power Switch section of the Electrical Characteristics table for the maximum bus current specification.
[4] Ensure that the last subordinate node meets the minimum V_{VBUS} requirement. If line fault diagnostics are not required on the B-port of a last subordinate node operating in LVI mode, nominal V_{VBUS} = V_{IN} = 3.3 V.
[5] Applies to ADR1, ADR2, SCK, MISO, MOSI, SIOn, BCLK, SYNC, $\overline{RST}$, and GPIO7 pins.
[6] Applies to SDA and SCL pins.

ELECTRICAL CHARACTERISTICS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Current						
Digital Core Logic Supply Currents						
I_{DVDD_OP}	V_{DVDD} Operating Current	V_{DVDD} = 1.98 V	10.0	14.1	16.5	mA
I_{DVDD_RST}	V_{DVDD} Reset Current	$\overline{RST}$ = 0 V	1.2	1.7	2.5	mA
I_{DVDD_STBY}	V_{DVDD} Standby Current	A2B_DATCTL = 0x80	8.5	10.7	12.5	mA
PLL Supply Currents						
I_{PLLVDD_OP}	V_{PLLVDD} Operating Current	V_{PLLVDD} = 1.98 V	0.45	0.68	0.92	mA
I_{PLLVDD_RST}	V_{PLLVDD} Reset Current	$\overline{RST}$ = 0 V	0.02	0.06	0.12	mA
I_{PLLVDD_STBY}	V_{PLLVDD} Standby Current	A2B_DATCTL = 0x80	0.45	0.68	0.92	mA
Transceiver Supply Currents[1]						
I_{TRXVDD_OP}	V_{TRXVDD} Operating Current	TX enabled, RX disabled, 100% duty cycle (I_{TXVDD}), V_{TRXVDD} = 3.45 V	12.5	15.0	16.5	mA
		TX disabled, RX enabled, 100% duty cycle (I_{RXVDD}), V_{TRXVDD} = 3.45 V	1.75	2.75	3.25	mA
I_{TRXVDD_RST}	V_{TRXVDD} Reset Current	$\overline{RST}$ = 0 V	1.7	2.8	4.0	mA
I_{TRXVDD_STBY}	V_{TRXVDD} Standby Current	A2B_DATCTL = 0x80	2.1	3.3	4.5	mA
IOVDD Supply Currents[2]						
I_{IOVDD_RST}	V_{IOVDD} Reset Current	$\overline{RST}$ = 0 V	65.0	92.0	115.0	µA
I_{IOVDD_STBY}	V_{IOVDD} Standby Current	A2B_DATCTL = 0x80	75.0	99.0	125.0	µA
VBUS Supply Currents						
I_{VBUS_OP}	V_{VBUS} Operating Current	V_{VBUS} = 24 V	0.68	0.79	0.90	mA
I_{VBUS_RST}	V_{VBUS} Reset Current	$\overline{RST}$ = 0 V, VBUS = 24 V	0.68	0.79	0.90	mA
I_{VBUS_STBY}	V_{VBUS} Standby Current	A2B_DATCTL = 0x80, VBUS = 24 V	0.68	0.79	0.90	mA
VIN Supply Currents						
I_{VIN_OP}	V_{VIN} Operating Current, LVI Mode = 0	V_{VIN} = 9 V, I_{VOUT1} = 17.4 mA[3], I_{VOUT2} = 31.5 mA[3]	38.96	46.08	50.72	mA
	V_{VIN} Operating Current, LVI Mode = 1	V_{VIN} = 3.45 V, I_{VOUT1} = 17.4 mA, I_{VOUT2} = 0 mA	11.00	15.43	18.32	mA
I_{VIN_RST}	V_{VIN} Reset Current, LVI Mode = 0	$\overline{RST}$ = 0 V, V_{VIN} = 9 V, V_{DVDD} = 1.98 V, V_{PLLVDD} = 1.98 V, V_{TRXVDD} = 3.45 V, V_{IOVDD} = 3.63 V	5.23	7.92	10.53	mA
	V_{VIN} Reset Current, LVI Mode = 1	$\overline{RST}$ = 0 V, V_{VIN} = Maximum V_{TRXVDD} = 3.45 V, V_{DVDD} = 1.98 V, V_{PLLVDD} = 1.98 V, V_{IOVDD} = 3.63 V	1.67	2.37	3.52	mA

Parameter		Conditions	Min	Typ	Max	Unit
Bus Voltage						
Chip Reset Assertion Voltage Threshold[4]						
V_{RST_VIN}		V_{VIN} dropping, LVI Mode = 0, 1	2.49		2.73	V
V_{RST_DVDD}		V_{DVDD} dropping	1.1		1.5	V
V_{RST_IOVDD}		V_{IOVDD} dropping	1.0		1.5	V
V_{RST_TRXVDD}		V_{TRXVDD} dropping, LVI Mode = 0, 1	2.2		2.8	V
Chip Reset Deassertion Voltage Threshold[5]						
V_{RSTN_VIN}		V_{VIN} rising, LVI Mode = 0, 1	2.76		3.10	V
V_{RSTN_DVDD}		V_{DVDD} rising	1.50		1.65	V
V_{RSTN_IOVDD}		V_{IOVDD} rising	1.20		1.62	V
V_{RSTN_TRXVDD}		V_{TRXVDD} rising, LVI Mode = 0, 1	2.53		3.05	V
Voltage Regulator (VREG1, VREG2)						
V_{VOUT1}	V_{REG1} Output Voltage		1.80	1.90	1.98	V
V_{VOUT2}	V_{REG2} Output Voltage		3.15	3.30	3.45	V
I_{VOUT1}[6]	V_{REG1} Output Current				100[7]	mA
I_{VOUT2}[6]	V_{REG2} Output Current				100[7]	mA
$I_{VOUT1} + I_{VOUT2}$					130[7]	mA
ΔV_{OUT1_LNREG}	V_{VOUT1} Line Regulation	V_{VIN} = 3.13 V to 3.47 V, I_{VOUT1} = 100 mA, LVI_MODE = 1			5	mV
ΔV_{OUT1_LNREG}	V_{VOUT1} Line Regulation	V_{VIN} = 3.7 V to 4.9 V, I_{VOUT1} = 100 mA			5	mV
ΔV_{OUT2_LNREG}	V_{VOUT2} Line Regulation	V_{VIN} = 3.7 V to 6.3 V, I_{VOUT2} = 100 mA			15	mV
ΔV_{OUT1_LNREG}	V_{VOUT1} Line Regulation	V_{VIN} = 3.7 V to 9 V, I_{VOUT1} = 40 mA			6	mV
ΔV_{OUT2_LNREG}	V_{VOUT2} Line Regulation	V_{VIN} = 3.7 V to 9 V, I_{VOUT2} = 50 mA			8	mV
ΔV_{OUT1_LDREG}	V_{VOUT1} Load Regulation	V_{VIN} = 3.13 V, I_{VOUT1}=1mA to 100 mA, LVI_MODE = 1			33	mV
ΔV_{OUT1_LDREG}	V_{VOUT1} Load Regulation	V_{VIN} = 3.7 V, I_{VOUT1} = 1 mA to 40 mA			15	mV
ΔV_{OUT2_LDREG}	V_{VOUT2} Load Regulation	V_{VIN} = 3.7 V, I_{VOUT2} = 1mA to 50 mA			25	mV
ΔV_{OUT1_LDREG}	V_{VOUT1} Load Regulation	V_{VIN} = 3.7 V, I_{VOUT1}= 1mA to 100 mA			33	mV
ΔV_{OUT2_LDREG}	V_{VOUT2} Load Regulation	V_{VIN} = 3.7 V, I_{VOUT2} = 1mA to 100 mA			42	mV
C_{Load1}	V_{REG1} Load Capacitance		1.8		26	µF
C_{Load2}	V_{REG2} Load Capacitance		3.9		26	µF

Parameter		Conditions	Min	Typ	Max	Unit
Digital I/O						
I_{IH}[8]	Input Leakage, High	V_{IOVDD} = 3.63 V, V_{IN} = 3.63 V			10.0	µA
I_{IL}[8]	Input Leakage, Low	V_{IOVDD} = 3.63 V, V_{IN} = 0 V			10.0	µA
$V_{OH1.9}$[8]	High Level Output Voltage	V_{IOVDD} = 1.70 V, I_{OH} = 1 mA	1.35			V
$V_{OH3.3}$[8]	High Level Output Voltage	V_{IOVDD} = 3.00 V, I_{OH} = 1 mA	2.40			V
V_{OL}[8]	Low Level Output Voltage	V_{IOVDD} = 3.00 V, I_{OL} = 1 mA			0.40	V
V_{OL}[8]	Low Level Output Voltage	V_{IOVDD} = 1.70 V, I_{OL} = 1 mA			0.40	V
V_{OL_I2C}[9]	I^2C Low Level Output Voltage	V_{IOVDD} = 3.00 V, I_{OL} = 3.0 mA			0.40	V
V_{OL_I2C}[10]	I^2C Low Level Output Voltage	V_{IOVDD} = 1.70 V, I_{OL} = 1.0 mA			0.40	V
C_{PD}	Pin Capacitance				5	pF
Line Power Switch						
Internal VSENSEP Currents						
$I_{VSENSEP}$	$V_{VSENSEP}$	$V_{VSENSEP}$ = V_{VBUS} = 24 V			400	µA
Internal ISENSEP Current						
$I_{ISENSEP}$	$V_{ISENSEP}$	V_{VBUS} − $V_{ISENSEP}$ = 100 mV	13.0	18.0	22.5	µA
SWN Leakage Current						
I_{SWN_LKG}	V_{SWN_LGKG}	V_{SWN} = 3.3 V			3.2	mA
Current Thresholds						
$\Delta V_{HSNS\_LM} = V_{VBUS} - V_{ISENSEP}$	High Side Current Limit Threshold	ON State	100	150	182	mV
$\Delta V_{LSNS\_CF} = V_{ISENSEN} - V_{VSENSEN}$	Low Side Current Fault Threshold	ON State, $V_{VSENSEN}$ = 0.1 V	115	150	160	mV
External High Side NFET Gate Drive						
$V_{SWP} - V_{VSENSEP}$		ON State, $V_{VSENSEP}$ = V_{VBUS}	4.5	4.7	5.1	V
SWP Slew Rate With Soft Start Enabled[11]						
$\Delta V_{SWP}/dt$		CAP_DLY = 0, V_{VBUS} = 7 V	1.9	2.2	2.5	V/ms
		CAP_DLY = 1, V_{VBUS} = 7 V	9.5	11.6	12.8	V/ms
External Low Side NFET Gate Drive						
V_{SWN}		ON State, 220k pull-down to GND on SWN	4.1			V

[1] Main node and last subordinate node only consume half the transceiver current because only one of the two transceivers is used.
[2] I_{IOVDD} operational current depends on switching currents on digital I/O pins such as BCLK, SYNC, ADR1, ADR2, SCK, MISO, MOSI, SIOn, and GPIO7. Customers can calculate the dynamic current using the formula: Output Dynamic Current = (C_{PD} + C_L) × V_{IOVDD} × Switching Frequency.
[3] I_{VOUT1} = Max I_{DVDD} + Max I_{PLLVDD} and I_{VOUT2} = Max I_{TRXVDD} + Typ I_{IOVDD}. The typical IOVDD current for I^2S at 25 MHz is 15 mA, with a standard capacitive load of 6 pF (average) on all pins.
[4] The chip reset signal is asserted when any supply voltage drops below the reset assertion threshold.
[5] The transceiver comes out of reset when all the power supply and the reset pin voltages are above the reset deassertion threshold.
[6] I_{VOUT1} + I_{VOUT2} < 30 mA when V_{IN} is bus powered by a current limiting device like the ADP2360 from the upstream node.
[7] Refer to the VREG Safe Operating Area section.
[8] Applies to ADR1, ADR2, SCK, MISO, MOSI, SIOn, BCLK, SYNC, IRQ, and GPIO7 pins.
[9] Applies to SDA and SCL pins in standard mode, fast mode, and fast mode plus.
[10] Applies to SDA and SCL pins in fast mode and fast mode plus.
[11] Applies when not in current limit with large capacitor bus loading.

Table 3. LVDS Input/Output Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
LVDS						
$\|V_{OD}\|$	Differential Output Voltage Magnitude	See Figure 27.	0.455		0.630	V
Receiver						
V_{TH}	Differential Input Threshold Voltage		–85		+85	mV

VREG Safe Operating Area

Figure 6 through Figure 8 show the safe operating area for VREG VOUT1 and VOUT2. These specifications are supported only when the V_{IN} supply can provide sufficient input current. For instance, V_{IN} on RJ45 bus-powered subordinate nodes is sourced from a current-limited supply. See footnote 6 in Electrical Characteristics.

Note that the safe operating area graphs are supported over the specified junction temperature (T_J) of the device. Perform thermal simulation and/or thermal measurement to meet the T_J specification.

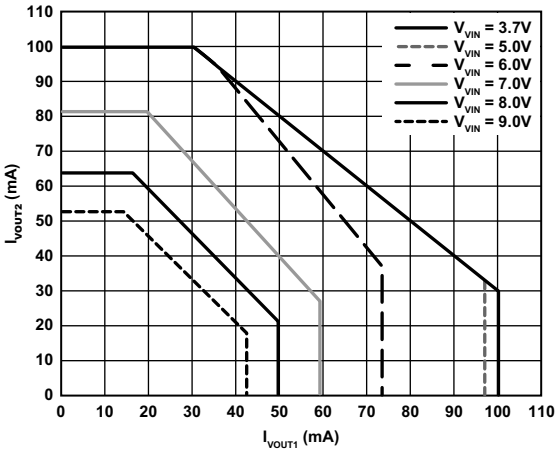


Figure 6. VREG VOUT1 Safe Operating Area, LVI_MODE = 0

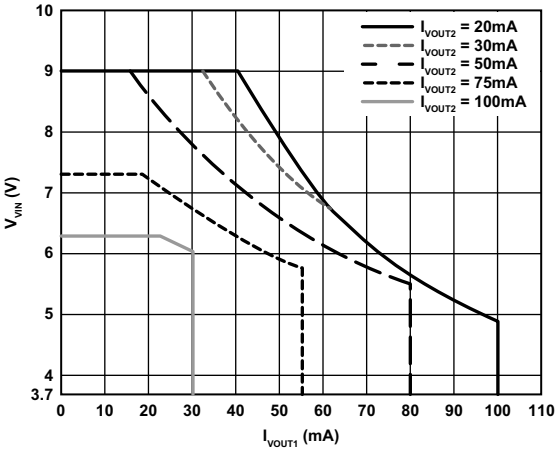


Figure 7. VREG VOUT2 Safe Operating Area, LVI_MODE = 0

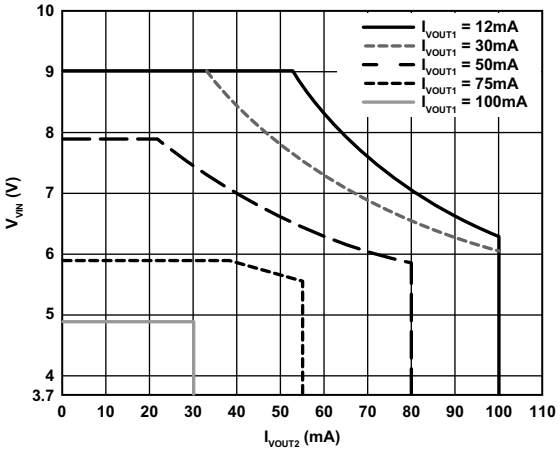


Figure 8. VREG VOUT1 and VOUT2 Safe Operating Area, LVI_MODE = 0

VMTR ADC SPECIFICATIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
VMTR ACTIVE CURRENT					
$I_{DD\_VMTR\_ACTIVE}$		35		58	µA
Resolution			8		Bits
DC ACCURACY					
Applicable for A2B_VMTR_VLTG0 to A2B_VMTR_VLTG4[1]					
Integral Nonlinearity (INL)		–0.82		0.84	LSB
Differential Nonlinearity (DNL)		–0.70		0.83	LSB
Offset Error		–2		2	LSB
Gain Error		–4		4	LSB
Applicable to A2B_VMTR_VLTG5[1]					
Integral Nonlinearity (INL)	A2B_VMTR_VLTG5 range = 0 to 150 mV	–0.90		0.91	LSB
Differential Nonlinearity (DNL)	A2B_VMTR_VLTG5 range = 0 to 150 mV	–0.77		0.77	LSB
Offset Error	A2B_VMTR_VLTG5 range = 0 to 150 mV	–2		2	LSB
Gain Error	A2B_VMTR_VLTG5 range = 0 to 150 mV	–5		5	LSB
Applicable to A2B_VMTR_VLTG6[1]					
Integral Nonlinearity (INL)	A2B_VMTR_VLTG6 range = 0 to 150 mV	–0.89		0.84	LSB
Differential Nonlinearity (DNL)	A2B_VMTR_VLTG6 range = 0 to 150 mV	–0.73		0.78	LSB
Offset Error	A2B_VMTR_VLTG6 range = 0 to 150 mV	–2		2	LSB
Gain Error	A2B_VMTR_VLTG5 range = 0 to 150 mV	–4		4	LSB

[1] See the Voltage Monitor ADC section in the *AD2437 A²B Transceiver Technical Reference* for details.

POWER SUPPLY REJECTION RATIO (PSRR)

Typical PSRR at T_J = 40°C.

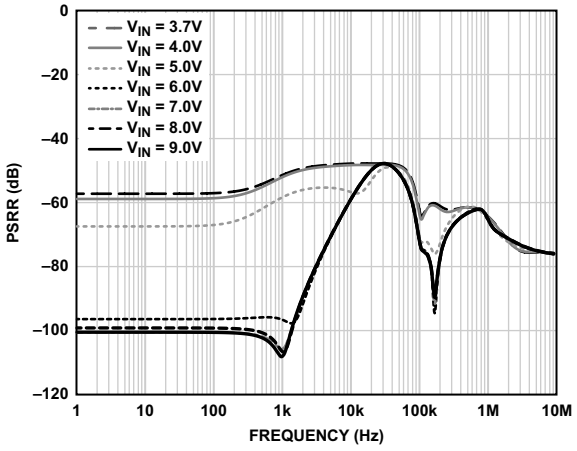


Figure 9. VOUT1 PSRR, I_{VOUT1} = 10 mA, C_{LOAD} = 4.7 µF || 0.1 µF

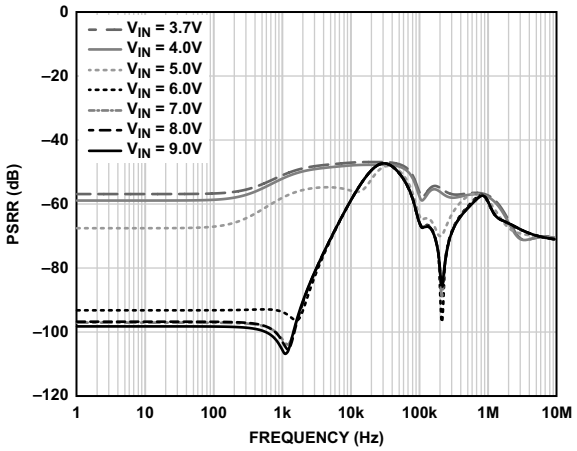


Figure 10. VOUT1 PSRR, I_{VOUT1} = 40 mA, C_{LOAD} = 4.7 µF || 0.1 µF

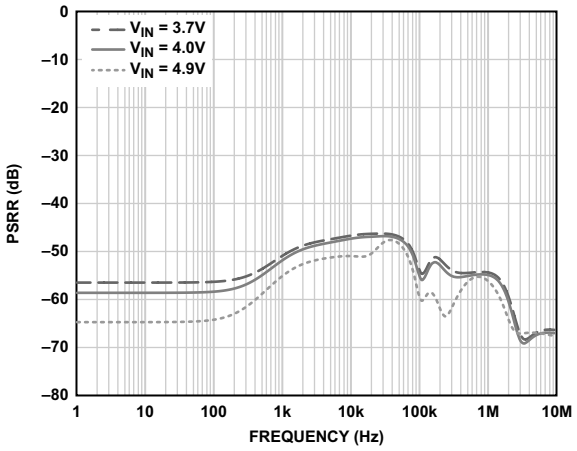


Figure 11. VOUT1 PSRR, I_{VOUT1} = 100 mA, C_{LOAD} = 4.7 µF || 0.1 µF

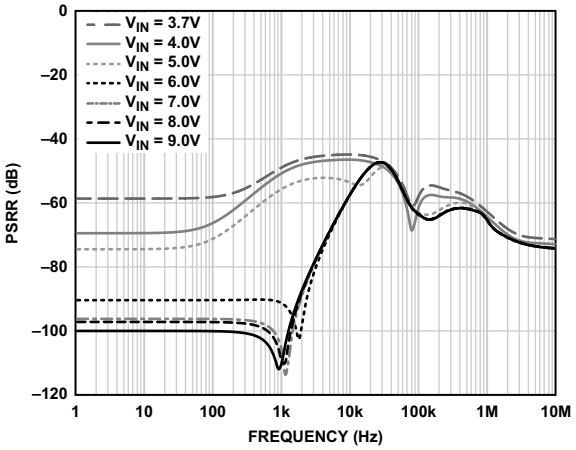


Figure 12. VOUT2 PSRR, I_{VOUT2} = 10 mA, C_{LOAD} = 6.8 µF || 0.1 µF

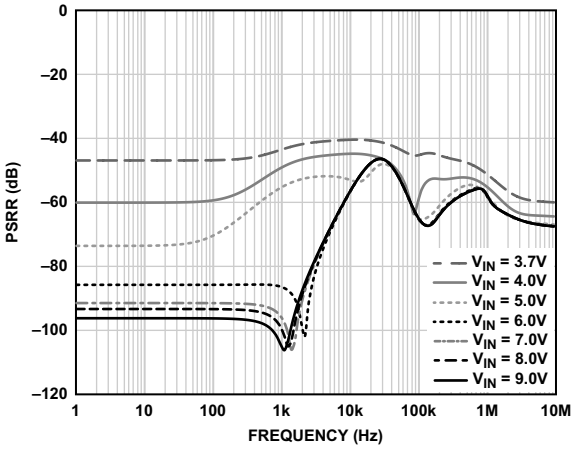


Figure 13. VOUT2 PSRR, I_{VOUT2} = 50 mA, C_{LOAD} = 6.8 µF || 0.1 µF

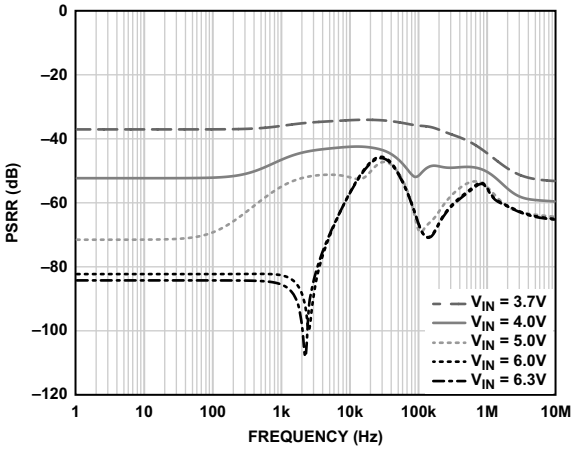


Figure 14. VOUT2 PSRR, I_{VOUT2} = 100 mA, C_{LOAD} = 6.8 µF || 0.1 µF

TIMING SPECIFICATIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Clock and Reset Timing

Table 4 and Figure 15 describe clock and reset operations.

Table 4. Clock and Reset Timing

Parameter		Min	Typ	Max	Unit
Timing Requirements					
f_{SYNCM}	SYNC Pin Input Frequency Continuous Clock				
	44.1 kHz SYNC Input	43.7	44.1	44.5	kHz
	48 kHz SYNC Input	47.5	48.0	48.5	kHz
$t_{SYNCIJ1}$	SYNC Pin Input Jitter RMS TIE[1]			1.0	ns
$t_{MCLKIJ1}$	Main Node Bit Clock Input Jitter RMS TIE[1]			1.0	ns
t_{ACCESS}	Device Access Time After Reset[2]	1.5			ms
t_{RST}	Reset Width[3]	10			µs
$t_{DNSYNCR}$[4]	Delay From First Missed SYNC Input to Reset (A^2B Main Node)	31	32	33	t_{SYNCM}
t_{DNSCFR}[4, 5]	Delay From First Missed SCF to Reset (A^2B Subordinate Node)	31	32	33	t_{SYNCM}
t_{PLK}	PLL Lock Time		7.5		ms
$f_{SYSBCLK}$	A^2B Bus Clock		$1024 \times f_{SYNCM}$		kHz
$t_{SYSBCLK}$	Bit-Period of A^2B Bus Clock		$1/(1024 \times f_{SYNCM})$		ns

[1] Maximum allowed jitter which does not degrade THD + N performance in the last subordinate node.
[2] The time it takes to access local registers via I^2C/SPI once the reset pin is deasserted and the power supplies are stable.
[3] Valid only when all the power supplies are stable. See Figure 15 for t_{RST}.
[4] Only consecutive missed SYNC or SCF transitions for the specified duration result in a reset.
[5] Add 1024 if SUSTAIN = 1.

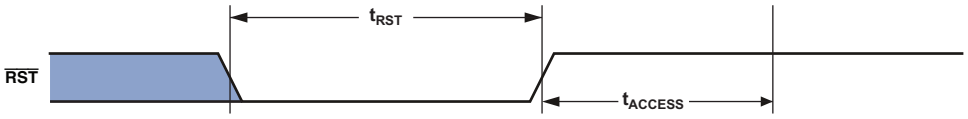


Figure 15. Reset Timing

I^2C Port Timing

The transceiver conforms to the I^2C specification v2.1.

I²S/TDM Port Timing

Table 5, Table 6, Figure 16, and Figure 17 describe I²S/TDM port operations. Note the following:

- The SIO0-SIO4 data pins on the I²S/TDM port can be configured for up to two PDM streams and up to five I²S/TDM streams, with a maximum of four I²S/TDM streams in the same direction. DTXn includes the DTX0, DTX1, DTX2, and DTX3 pins; and DRXn includes DRX0, DRX1, DRX2, and DRX3 in Table 5.
- The I²S/TDM target timing applies to the A²B main transceiver and the A²B subordinate transceiver operating in parallel bus mode.
- The I²S/TDM controller timing applies to the A²B subordinate transceiver.

Table 5. I²S/TDM Port—Controller Timing

Parameter		IOVDD = 1.8 V Min	IOVDD = 1.8 V Max	IOVDD = 3.3 V Min	IOVDD = 3.3 V Max	Unit
Timing Requirements						
t_{RISM}	DRXn Input Setup Before BCLK Sample Edge	1.0		1.5		ns
t_{RIHM}	DRXn Input Hold After BCLK Sample Edge	5.5		2.0		ns
Switching Characteristics						
f_{BCLKM}	BCLK Output Frequency[1]		25.0		50.0	MHz
$t_{BCLKMOJ}$	BCLK Output Jitter (RMS Cycle to Cycle)					
	at f_{BCLKSM} = 12.288 MHz		100		100	ps
	at f_{BCLKSM} = 24.576 MHz		100		100	ps
t_{SOL}/t_{SOH}	Transmit or Receive BCLK Duty Cycle	49%	51%	49%	51%	t_{BCLKM}
t_{SOJ}	SYNC Output Jitter (RMS Cycle to Cycle)					
	Normal Mode 48 kHz		2.25		2.25	ns
	Increased Data Rate 2× SYNC		1.25		1.25	ns
	Increased Data Rate 4× SYNC		1.00		1.00	ns
t_{SOD}	SYNC Output Delay After BCLK Drive Edge		9.75		9.75	ns
t_{SOHD}	SYNC Output Hold After BCLK Drive Edge	3.0		4.5		ns
t_{DODM}	DTXn Output Delay After BCLK Drive Edge		10.25		9.75	ns
t_{DOHM}	DTXn Output Hold After BCLK Drive Edge	5.5		6.0		ns

[1] When V_{IOVDD} = 3.3 V, the setup and hold timing at the 50 MHz maximum bit clock rate can be violated when interfacing with other I²S devices. The timing violations are observed when the subordinate transceiver I²S/TDM port is receiving and the main transceiver I²S/TDM port is transmitting. In this case, the maximum BCLK frequency of 50 MHz cannot be achieved.

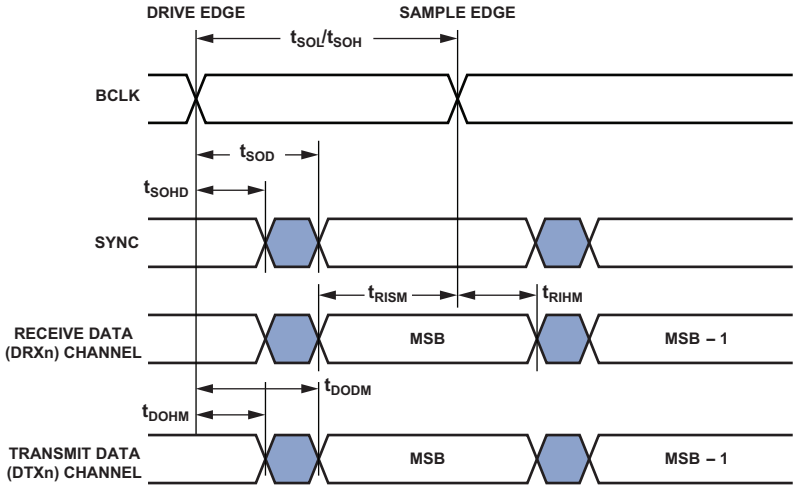


Figure 16. I²S/TDM Port—Controller Timing

Table 6. I²S/TDM Port—Target Timing

Parameter		IOVDD = 1.8 V Min	IOVDD = 1.8 V Max	IOVDD = 3.3 V Min	IOVDD = 3.3 V Max	Unit
Timing Requirements						
t_{BCLKW}	BCLK Width	19.5		9.5		ns
t_{BCLKS}	BCLK Period	39.0		19.0		ns
t_{SIS}	SYNC Input Setup Before BCLK Sample Edge	2.25		2.25		ns
t_{SIH}	SYNC Input Hold After BCLK Sample Edge	2.0		2.5		ns
t_{RISS}	DRXn Input Setup Before BCLK Sample Edge	2.0		1.5		ns
t_{RIHS}	DRXn Input Hold After BCLK Sample Edge	1.5		0.5		ns
Switching Characteristics						
t_{DODS}	DTXn Output Delay After BCLK Drive Edge		16.5		12.0	ns
t_{DOHS}	DTXn Output Hold After BCLK Drive Edge	3.0		3.0		ns

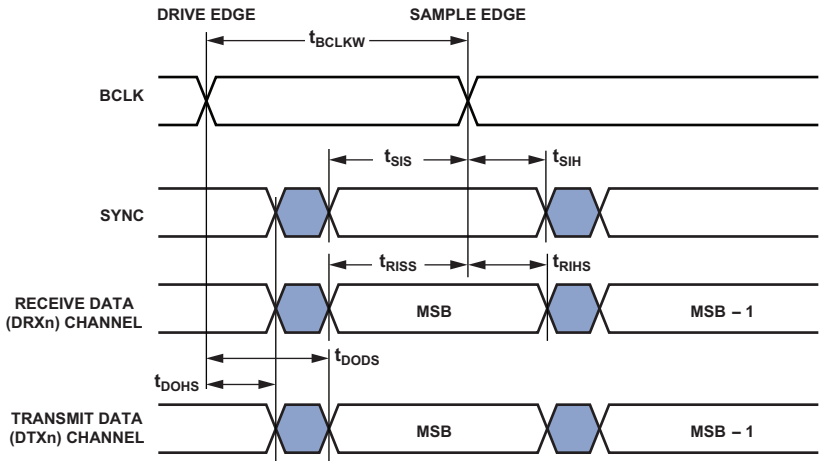


Figure 17. I²S/TDM Port—Target Timing

Table 7. I²S Target (A²B Main Node) DTXn Enable and Three-State Timing

Parameter		IOVDD = 1.8 V Min	IOVDD = 1.8 V Max	IOVDD = 3.3 V Min	IOVDD = 3.3 V Max	Unit
Switching Characteristics[1]						
t_{DOENM}	DTXn Data Enable Delay After BCLK Drive Edge	5.0		4.0		ns
t_{DODIM}	DTXn Data Disable Delay After BCLK Drive Edge		14.5		10.5	ns

[1] Refer to the A2B_TXOFFSET register for three-state programming details.

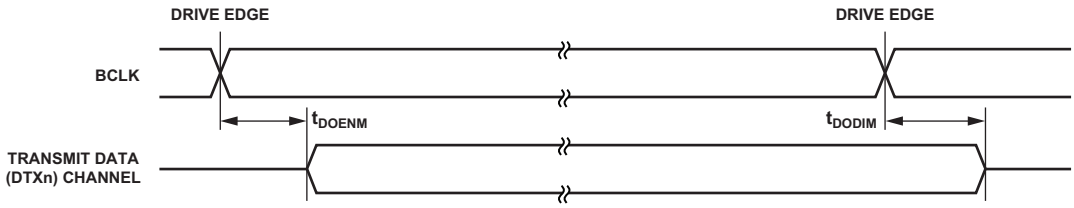


Figure 18. I²S Target (A²B Main Node) DTXn Enable and Three-State Timing

Table 8. Pulse Density Modulation (PDM) Microphone Input Timing

Parameter		IOVDD = 1.8 V Min	IOVDD = 1.8 V Max	IOVDD = 3.3 V Min	IOVDD = 3.3 V Max	Unit
Timing Requirements						
t_{PDMSS}	PDMn Input Setup Before BCLK/PDMCLK	17.5		12.0		ns
t_{PDMHS}	PDMn Input Hold After BCLK/PDMCLK	0		0		ns
Switching Characteristics						
f_{PDMCLK}	BCLK/PDMCLK Output Frequency at f_{SYNC} = 48 kHz	3.040	3.104	3.040	3.104	MHz
$t_{PDMCLKOJ}$	BCLK/PDMCLK Output Jitter RMS Cycle to Cycle		150		150	ps
$t_{PDMCLKW}$	BCLK/PDMCLK Output Pulse Width	161.0		162.5		ns

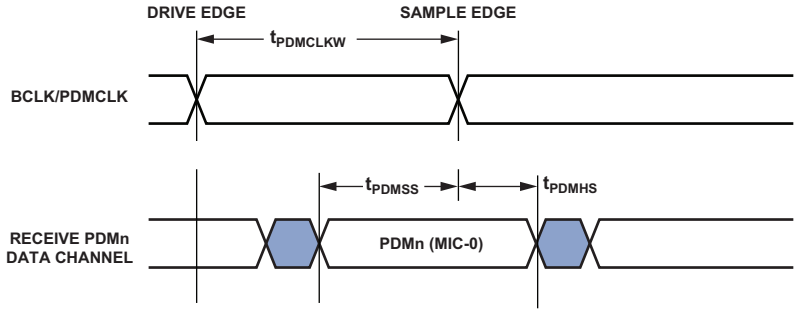


Figure 19. PDM Timing

GPIO and CLKOUT Timing

Table 9 describes GPIO and CLKOUT operations.

Table 9. GPIO and CLKOUT Timing

Parameter		Min	Typ	Max	Unit
Timing Requirement					
t_{GIPW}	GPIO Input Pulse Width	$t_{SYSBCLK}$ + 5			ns
Switching Characteristics					
t_{GOPW}	GPIO Output Pulse Width	$t_{SYSBCLK}$ − 1			ns
$t_{CLKOUTJ}$[1]	CLKOUT Jitter RMS TIE for 48 kHz SYNC				
	at f_{CLKOUT} = 12.288 MHz		1.0	1.90	ns
	at f_{CLKOUT} = 24.576 MHz		1.0	1.95	ns

[1] Jitter measured at Subordinate Node 0.

Serial Peripheral Interface (SPI) Port—Master Timing

Table 10 and Figure 20 describe serial peripheral interface (SPI) port master operations.

Table 10. Serial Peripheral Interface (SPI) Port—Master Timing

		IOVDD = 1.8 V		IOVDD = 3.3 V		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{SMISO}	Data Input Valid to SCK Sample Edge (Data Input Setup)	18.5		17.5		ns
t_{HMISO}	SCK Sample Edge to Data Input Invalid (Data Input Hold)	5.50		6.75		ns
Switching Characteristics						
t_{SCKM}[1]	SCK Period	80.3		80.5		ns
f_{SCKHM}[1]	SCK High Period	32.75		39.5		ns
t_{SCKLM}[1]	SCK Low Period	37.0		39.7		ns
t_{DMOSI}	SCK Drive Edge to Data Out Valid (Data Out Delay)		9.00		3.25	ns
t_{HDMOSI}	SCK Drive Edge to Data Out Invalid (Data Out Hold)	0.5		0.5		ns
t_{SSSM}[1]	$\overline{\text{SPISSELn}}$ Assertion to First SCK Edge	75.75		77.00		ns
t_{HSSM}[1]	Last SCK Edge to $\overline{\text{SPISSELn}}$ Deassertion	35.50		36.75		ns
t_{SSPWM}	$\overline{\text{SPISSELn}}$ Pulse Width High (Inactive State Between Transfers)	11.25		11.25		ns

[1] Measured at $f_{SCKM} = 1/t_{SCKM} = 12.288$ MHz. Specification scales with f_{SCKM}.

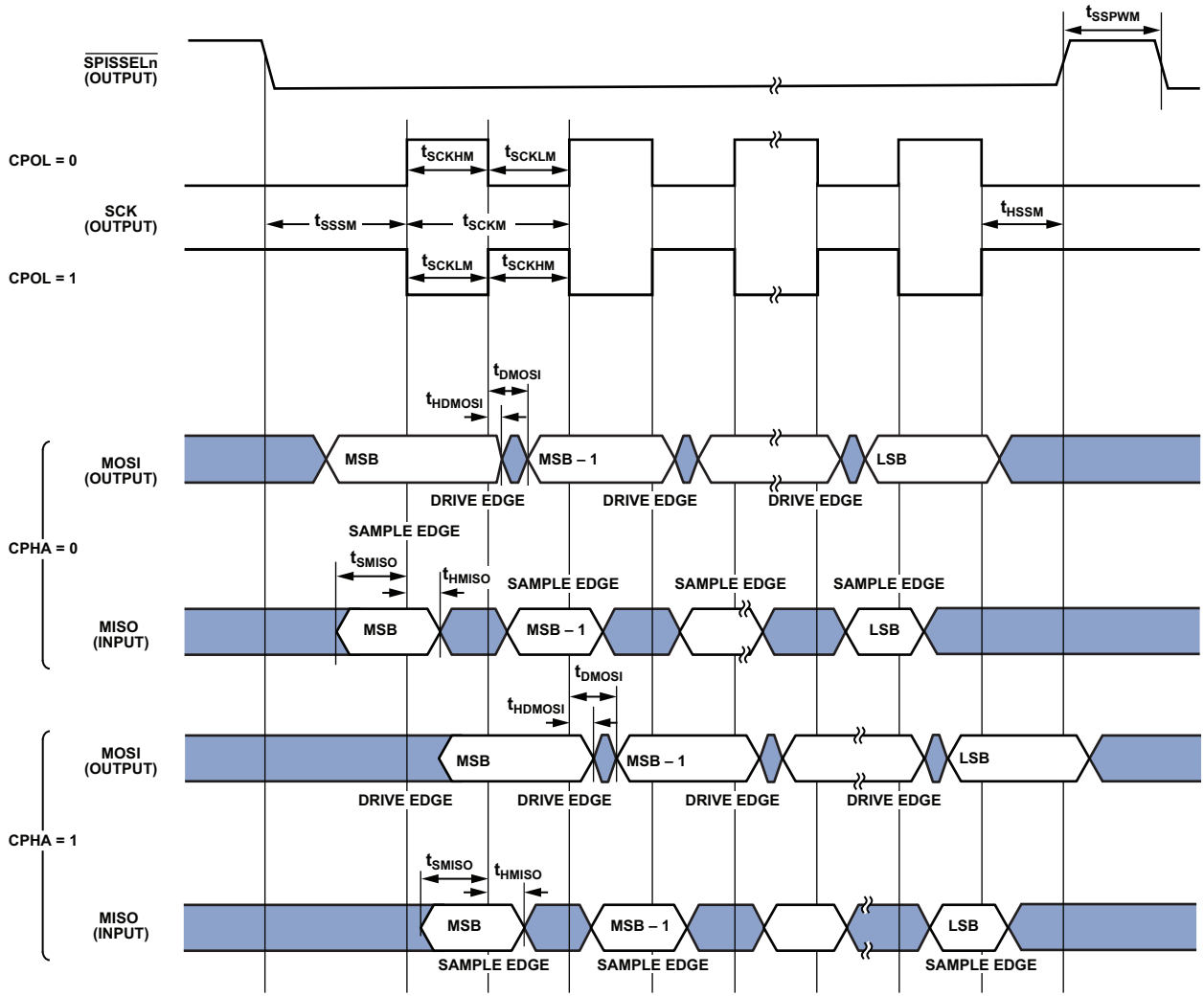


Figure 20. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 11 and Figure 21 describe serial peripheral interface (SPI) port slave operations.

Table 11. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		IOVDD = 1.8 V		IOVDD = 3.3 V		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SCKS}	SCK Period	66.67		66.67		ns
t_{SCKHS}	SCK High Period	30		30		ns
t_{SCKLS}	SCK Low Period	30		30		ns
t_{SMOSI}	Data Input Valid to SCK Sample Edge (Data Input Setup)	2.0		1.0		ns
t_{HMOSI}	SCK Sample Edge to Data Input Invalid (Data Input Hold)	1.8		0.5		ns
t_{SSS}	$\overline{\text{SPISS}}$ Assertion to First SCK Edge	7.0		8.0		ns
t_{HSS}	Last SCK Edge to $\overline{\text{SPISS}}$ Deassertion	10.75		9.75		ns
t_{SSPWS}	$\overline{\text{SPISS}}$ Pulse Width High (Inactive State Between Transfers)	25		25		ns
Switching Characteristics						
t_{DSSOE}	$\overline{\text{SPISS}}$ Assertion to Data Out Active	4.50	28.50	2.50	17.50	ns
t_{DSSHI}	$\overline{\text{SPISS}}$ Deassertion to Data Out High Impedance	1.25	22.00	1.25	12.75	ns
t_{DMISO}	SCK Drive Edge to Data Out Valid (Data Out Delay)		19.50		10.75	ns
t_{HDMISO}	SCK Drive Edge to Data Out Invalid (Data Out Hold)	2.50		3.50		ns

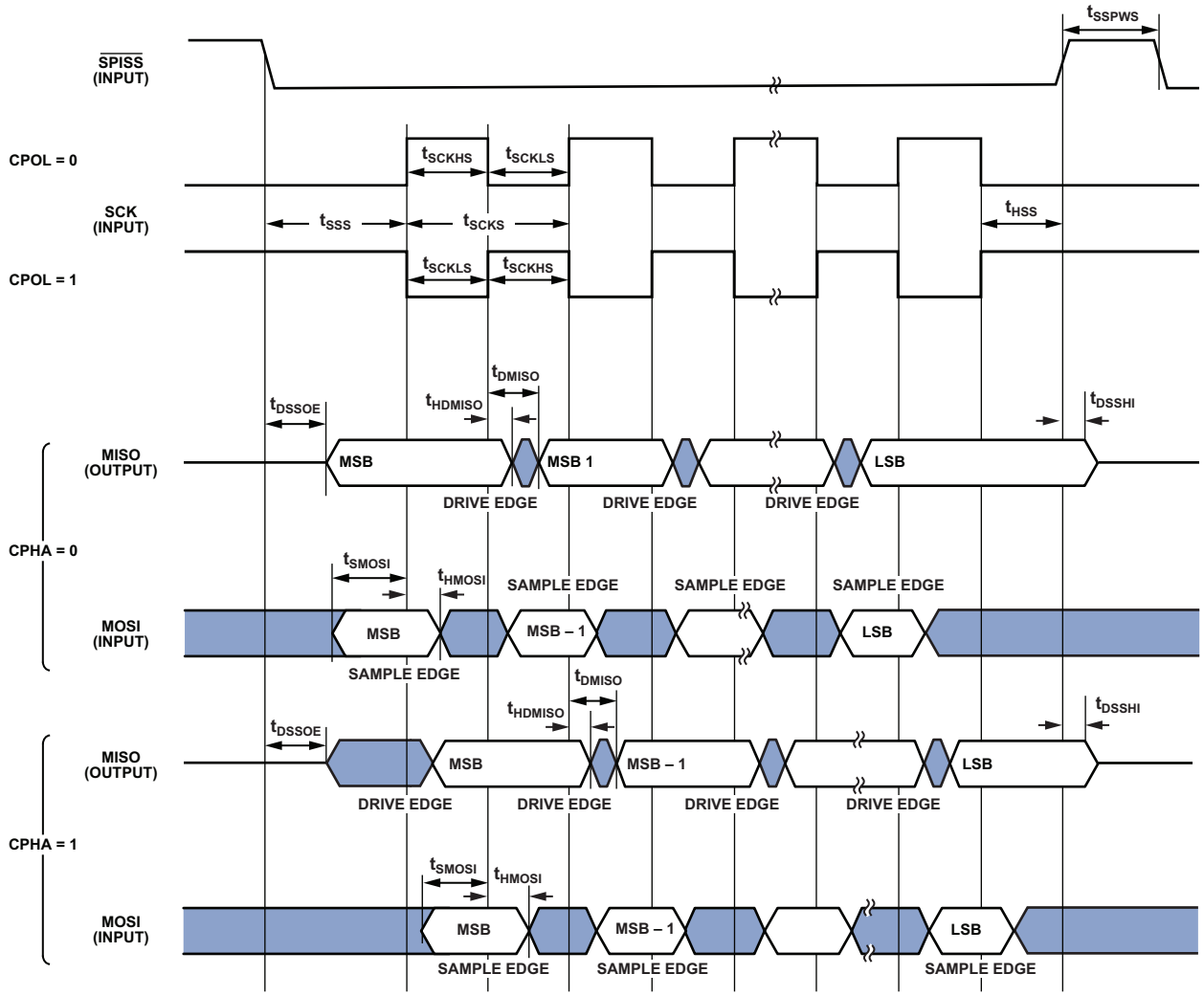


Figure 21. Serial Peripheral Interface (SPI) Port—Slave Timing

Pulse Width Modulation (PWM) Timing

Table 12 describes pulse width modulation (PWM) operations.

Table 12. Pulse Width Modulation (PWM) Timing

Parameter		Min	Typ	Max	Unit
Switching Characteristics					
f_{PWM}	PWM Frequency	$f_{SYNCM}/256$		$f_{SYNCM} \times 4$	Hz
t_{PWM_ON}	PWM Minimum ON Time	0			ns
t_{PWM_OFF}	PWM Minimum OFF Time	18			ns

A²B BUS SYSTEM SPECIFICATION

Table 13. A²B System Specifications

Parameter	System Specification
Cable	CAT5e/CAT6/CAT7; XLR/DMX; or single-pair wire
Maximum Cable Length	300 m total, up to 30 m between nodes
Maximum Number of Nodes	17 nodes (1 main node and 16 subordinate nodes)[1]
Maximum A²B Bus Bandwidth	$1024 \times f_{SYNCM}$
Maximum Number of A²B Data Slots	64 total, up to 32 upstream and 32 downstream data slots. It includes SPI data tunnel slots and audio data slots. The number of SPI data tunnel slots can be configured between 2 and 12; the number of audio slots can be configured between 0 to 32 depending upon system design. See the *AD2437 A²B Transceiver Technical Reference*.
Number of Audio TDM Channels per Node	Individually programmable 0 to 32 upstream channels and 0 to 32 downstream channels
Synchronous A²B Data Slot Size	8, 12, 16, 20, 24, 28, or 32 bits to match I²S/TDM data-word lengths. Same slot size for all nodes. Upstream and downstream can choose different slot sizes. 12-, 16-, or 20-bit slot sizes can carry compressed data over the A²B bus for 16-, 20-, or 24-bit I²S/TDM word lengths.
Audio Sampling Frequency	44.1 kHz or 48 kHz. All nodes sample synchronously. Subordinate node transceivers support sample rates (f_S) of 1× (48 kHz), 2× (96 kHz) or 4× (192 kHz), individually configured per subordinate node. Subordinate node transceivers also support reduced rate sampling for 24 kHz, 12 kHz, 6 kHz, 4 kHz, 3 kHz, 2.4 kHz, 2 kHz, 1.71 kHz, or 1.5 kHz at a low latency 48 kHz superframe rate. See the *AD2437 A²B Transceiver Technical Reference* for more information.
Discovery Time	<50 ms per node and <<500 ms for total system startup in a system with 10 nodes (includes register initialization)
Maximum Current Supported During Discovery per Node (I_{SYS_DSCVRY})	250 mA
Maximum Capacitive Load per Bus Powered Subordinate Node C_{SUB}	1000 µF
Bit Error Detection and Correction	Robust error detection for control data and status data with 16-bit cyclic redundancy check (CRC) Parity and line code error detection on synchronous data slots with audio error correction (repeat of last known good data). For 24-bit and 32-bit data channels, single error correction and double error detection (SECDED) of synchronous data slots is possible.
Line Fault Diagnostics	Location and cause of fault can be detected for A²B wires shorted to a high voltage (for example, positive terminal of car battery), shorted to ground, wires shorted to each other, wires reversed, wires open, or wrong port connection. See the *AD2437 A²B Transceiver Technical Reference* for more information.
System EMI/EMC	Meets or exceeds industry specification for robustness

[1] Local power nodes are needed to maintain data sheet-specified supply voltages at each node.

RMS Time Interval Error (TIE) Jitter

Clocks in an A^{2}B system are passed from the main node to Subordinate Node 0, from Subordinate Node 0 to Subordinate Node 1, and so on. Each transceiver adds self jitter to the incoming jitter, which results in jitter growth from the main node to the nth subordinate node. Table 14 illustrates typical RMS TIE jitter growth.

Table 14. SYNC Output RMS TIE Jitter at Each Subordinate Node[1]

Subordinate Node	Typ	Max	Unit
1	1.25	2.28	ns
2	1.47	2.29	ns
3	1.59	2.41	ns
4	1.76	2.59	ns
5	1.88	2.95	ns
6	1.99	3.18	ns
7	2.14	3.57	ns
8	2.24	3.08	ns
9	2.31	4.01	ns
10	2.48	4.24	ns
11	2.60	4.31	ns
12	2.66	4.35	ns
13	2.70	4.55	ns
14	2.75	4.59	ns
15	2.80	4.70	ns
16	2.95	4.89	ns

[1] Measured at f_{SYNC} = 48 kHz.

Table 15. BCLK Output RMS TIE Jitter at Each Subordinate Node[1]

Subordinate Node	Typ	Max	Unit
1	1.19	2.09	ns
2	1.39	2.21	ns
3	1.59	2.33	ns
4	1.76	2.51	ns
5	1.86	2.86	ns
6	1.91	3.11	ns
7	2.06	3.31	ns
8	2.21	3.45	ns
9	2.28	3.84	ns
10	2.31	4.00	ns
11	2.47	4.03	ns
12	2.57	4.06	ns
13	2.74	4.28	ns
14	2.78	4.38	ns
15	2.83	4.50	ns
16	2.88	4.60	ns

[1] Measured at f_{BCLK} = 3.072 MHz.

POWER-UP SEQUENCING RESTRICTIONS

There are no power-up sequencing restrictions. The transceiver remains in the reset state until all of the supplies (VIN, IOVDD, DVDD, and TRXVDD) power up. Additionally, the hardware reset pin can be deasserted once all of the power domains are stable. To avoid damage to the input pins, V_{IOVDD} must be within specification before the external devices drive the input signals, except the SCL and SDA pins.

PDM TYPICAL PERFORMANCE CHARACTERISTICS

Figure 22 through Figure 26 and Table 16 describe typical PDM performance characteristics.

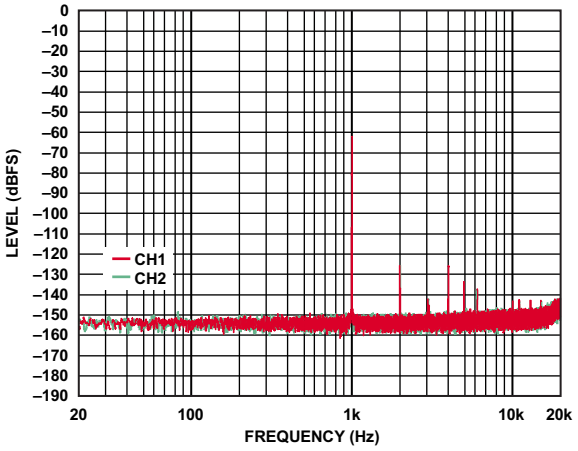


Figure 22. PDM FFT, f_{SYNCM} = 48 kHz, –60 dBFS Input

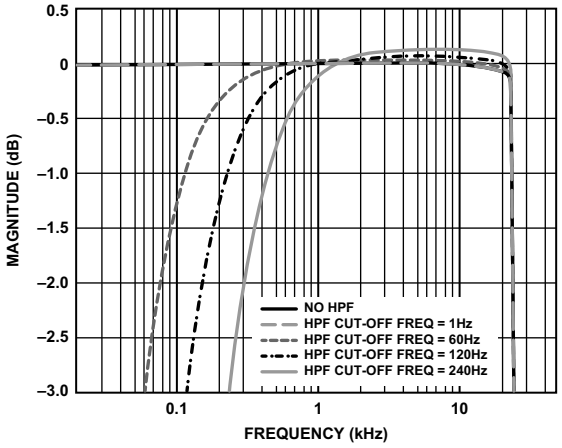


Figure 23. PDM Frequency Response (f_{SYNCM} = 48 kHz)

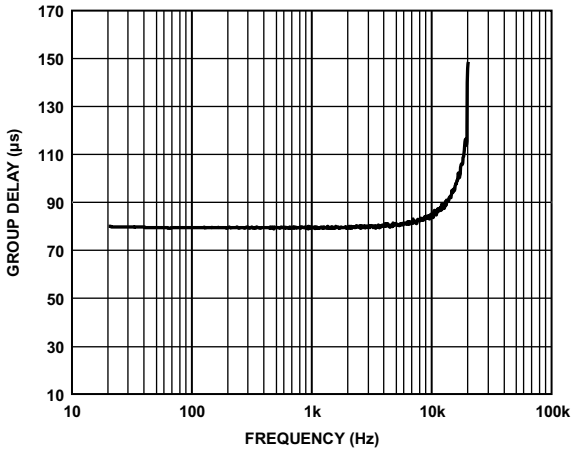


Figure 24. PDM Group Delay vs. Frequency, f_{SYNCM} = 48 kHz

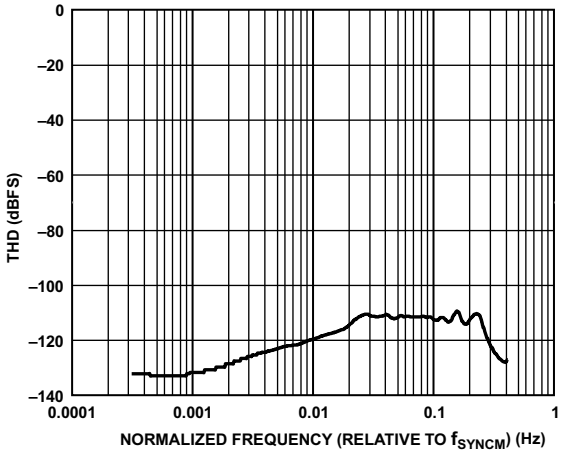


Figure 25. PDM Total Harmonic Distortion (THD) vs. Normalized Frequency (Relative to f_{SYNCM})

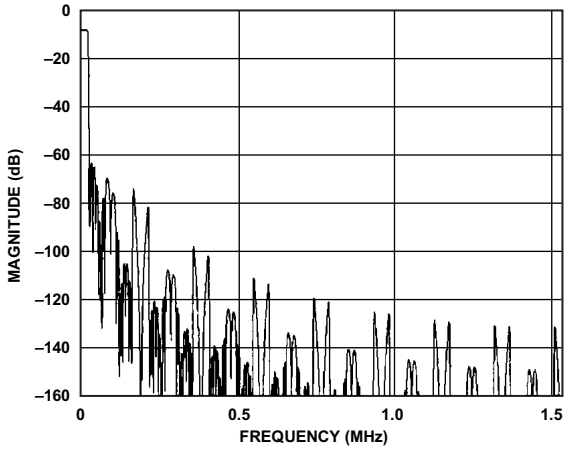


Figure 26. PDM Out of Band Frequency Response (f_{SYNCM} = 48 kHz)

Table 16. PDM Interface Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Dynamic Range with A-Weighted Filter	20 Hz to 20 kHz, –60 dBFS input		120		dB
SNR with A-Weighted Filter	20 Hz to 20 kHz		108		dB
Decimation Ratio[1]	Default is 64×	64×		256×	
Frequency Response[2]	DC to 0.45 f_{SYNCM}	–0.1		+0.01	dB
Stop Band			0.566		f_{SYNCM}
Attenuation		74			dB
Group Delay	0.02 f_{SYNCM} input signal		3.80		f_{SYNCM} cycles
Gain	PDM to PCM		0		dB
Start-Up Time[3]			48		f_{SYNCM} cycles
Bit Width	Internal and output		24		Bits

[1] The decimation ratio is controlled by the A2B_PDMCTL.PDMRATE field.
[2] Measured with the high pass filter (HPF) disabled. Refer to Figure 23 for the frequency response with the HPF enabled at different cut-off frequencies.
[3] The PDM start-up time is the time for the filters to settle after the PDM block is enabled. It is the time to wait before data is guaranteed to meet the specified performance.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 17 can cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 17. Absolute Maximum Ratings

Parameter	Rating
VIN to VSS	–0.3 V to +30 V
VBUS to VSS	–0.3 V to +30 V
Power Supply IOVDD to IOVSS	–0.3 V to +3.63 V
Power Supply DVDD to DVSS	–0.3 V to +1.98 V
Power Supply PLLVDD to PLLVSS	–0.3 V to +1.98 V
Power Supply TRXVDD to TRXVSS	–0.3 V to +3.63 V
Digital Pin Output Voltage Swing[1]	–0.3 V to V_{IOVDD} + 0.5 V
Pin Voltage While IOVDD is Unbiased	
I^2C Pins SCL and SDA	–0.3 V to +5.5 V
Other Digital Pins[1]	–0.3 V to +0.3 V
Pin Voltage While IOVDD is Biased	
I^2C Pins SCL and SDA	–0.3 V to +5.5 V
Other Digital Pins[2, 3]	–0.3 V to +2.10 V
Other Digital Pins[2, 4]	–0.3 V to +3.63 V
A^2B Bus Terminal Voltage (AP, AN, BP, and BN Pins)	–0.3 V to +4.1 V
Voltage to VSS	
ISENSEP, ISENSEN, VSENSEP, VSENSEN	–0.3 V to +30 V
SWN	–0.3 V to +7 V
ISENSEP	V_{VBUS} ±7 V
SWP to VSENSEP	–0.3 V to +8 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	–40°C to +125°C
Digital Pin Output Current per Pin Group[5]	15 mA

[1] Applies to BCLK, SYNC, ADR1, ADR2, SCK, MISO, MOSI, SIOn, IRQ, and GPIO7 pins.
[2] Applies to BCLK, SYNC, ADR1, ADR2, SCK, MISO, MOSI, SIOn, $\overline{RST}$, and GPIO7 pins.
[3] Applies when nominal V_{IOVDD} is 1.8 V.
[4] Applies when nominal V_{IOVDD} is 3.3 V.
[5] For more information, see the following description and Table 18.

Permanent damage can occur if the digital pin output current per pin group value is exceeded. For example, if three pins from Group 2 in the Total Current Pin Groups table are sourcing or sinking 2 mA each, the total current for those pins is 6 mA. Up to 9 mA can be sourced or sunk by the remaining pins in the group without damaging the device.

Table 18. Total Current Pin Groups

Group	Pins in Group
1	SIO0, SIO1, SIO2, SYNC, BCLK
2	SIO3, SIO4, GPIO7
3	SDA[1], SCL[1], MISO[2], MOSI[2], SCK[2]
4	ADR1, ADR2, IRQ

[1] Applicable when SCL and SDA are used as GPIO.
[2] PWM pins are multiplexed with SPI pins and cannot directly drive high power LEDs. An LED driver can be interfaced to drive high power LEDs.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THERMAL CHARACTERISTICS

The AD2437 A^{2}B transceiver is rated for performance over the temperature range specified in Operating Conditions.

The JESD51 package thermal characteristics in this section are provided for package comparison and estimation purposes only. They are not intended for accurate system temperature calculation. System thermal simulation is required for accurate temperature analysis that accounts for all specific 3D system design features, including, but not limited to other heat sources, use of heat-sinks, and the system enclosure. Contact Analog Devices for package thermal models that are intended for use with thermal simulation tools.

In Table 19, airflow measurements comply with JEDEC standards JESD51-13, and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 for leaded surface mount packages. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

To estimate the junction temperature of a single device while on a JEDEC 2S2P PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J is the junction temperature (°C).

T_{CASE} is the case temperature (°C) measured at the top center of the package.

Ψ_{JT} is the typical value (junction-to-top of package characterization parameter) from Table 19.

P_D is the power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + \theta_{JA} \times P_D$$

where T_A is the ambient temperature (°C).

Values of θ_{JB} are provided for package comparison and PCB design considerations when an external heat sink is required.

The 48-lead LFCSP package requires thermal trace squares and thermal vias to an embedded ground plane in the PCB. The exposed paddle must connect to ground for proper operation and to meet data sheet specifications. Refer to JEDEC standard JESD51-5 for more information.

Note that the thermal characteristics values provided in Table 19 are modeled values.

Table 19. Thermal Characteristics

Parameter	Conditions	Typical (°C/W)
θ_{JA}	Airflow = 0 m/s	23.256
θ_{JMA}	Airflow = 1 m/s	20.98
θ_{JMA}	Airflow = 2 m/s	20.19
θ_{JB}	Airflow = 0 m/s	5.8
Ψ_{JT}	Airflow = 0 m/s	0.16
Ψ_{JT}	Airflow = 1 m/s	0.28
Ψ_{JT}	Airflow = 2 m/s	0.36

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

Figure 27 shows a line driver voltage measurement circuit of the differential line driver and receiver AP/AN and BP/BN pins.

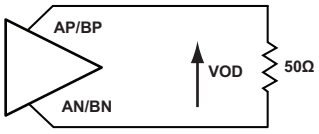


Figure 27. Differential Line Driver Voltage Measurement

OUTPUT DRIVE CURRENTS

Figure 28 through Figure 33 show typical current voltage characteristics for the output drivers of the transceiver. The curves represent the current drive capability of the output drivers as a function of output voltage. Drive strength 0 is DS0, and drive strength 1 is DS1.

Note the following:

- I^2C pins only support high drive strength (DS1).
- Digital I/Os include ADR1, ADR2, SCK, MISO, MOSI, SIOn, BCLK, SYNC, IRQ, and GPIO7 pins.

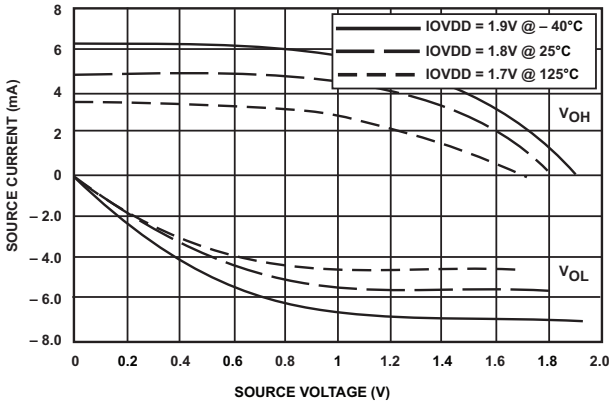


Figure 28. Digital I/O Drivers (DS0, 1.8 V IOVDD)

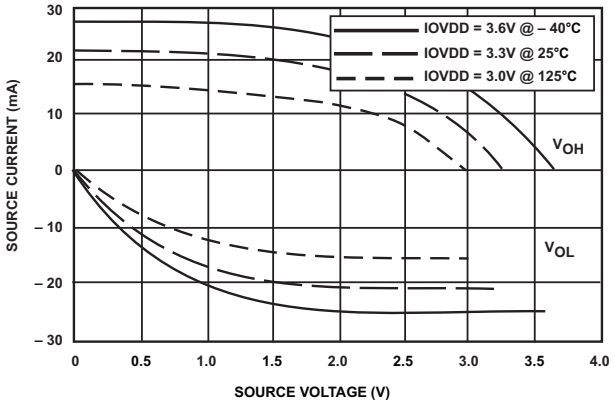


Figure 29. Digital I/O Drivers (DS0, 3.3 V IOVDD)

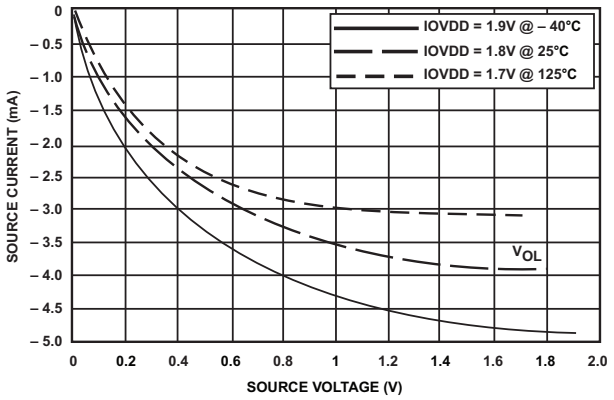


Figure 30. I^2C Drivers (1.8 V IOVDD)

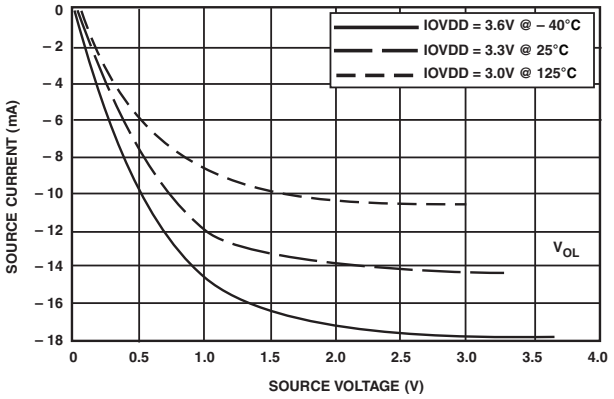


Figure 31. I^2C Drivers (3.3 V IOVDD)

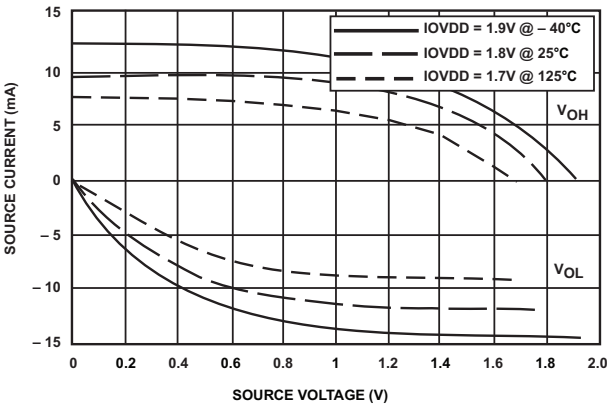


Figure 32. Digital I/O Drivers (DS1, 1.8 V IOVDD)

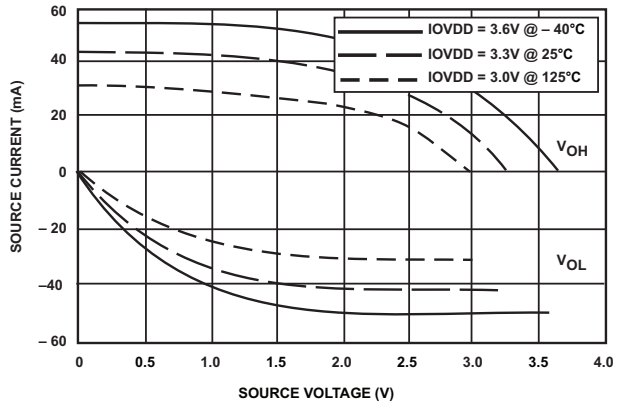


Figure 33. Digital I/O Drivers (DS1, 3.3 V IOVDD)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 34 shows the measurement point for ac measurements (except output enable/disable). The measurement point, V_{MEAS}, is $V_{IOVDD}/2$ for V_{IOVDD} (nominal) = 3.3 V.

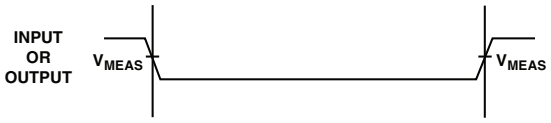


Figure 34. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 35. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

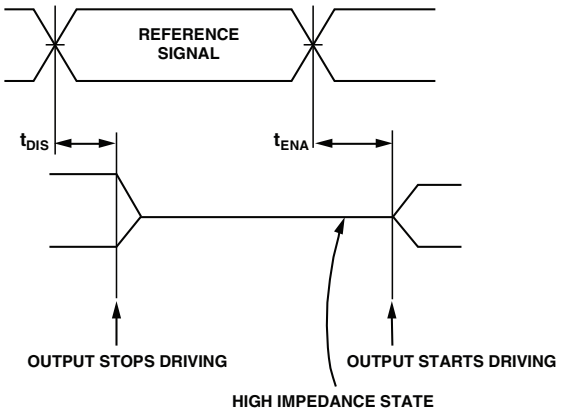


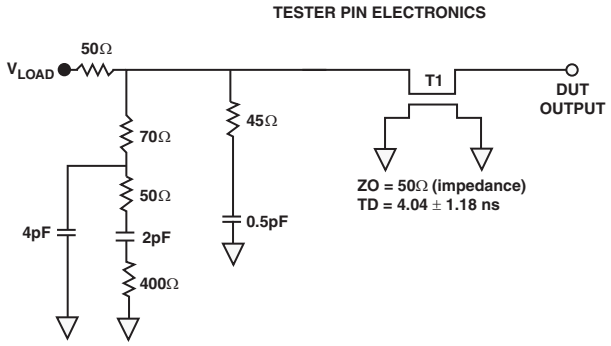
Figure 35. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 35.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 36). V_{LOAD} is equal to $V_{IOVDD}/2$. Figure 37 through Figure 40 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 37 through Figure 40 cannot be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, THE SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 36. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

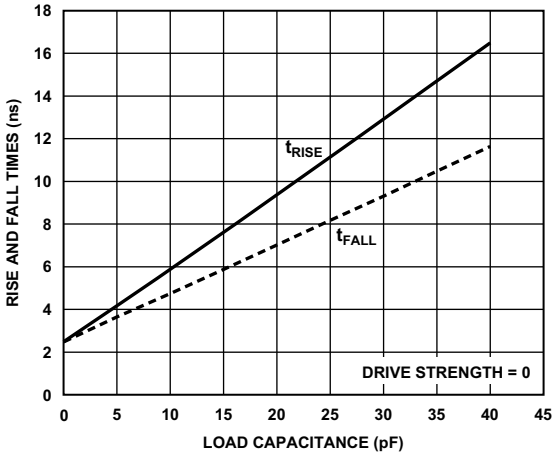


Figure 37. Digital I/O Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 1.8 V, T_J = 25°C)

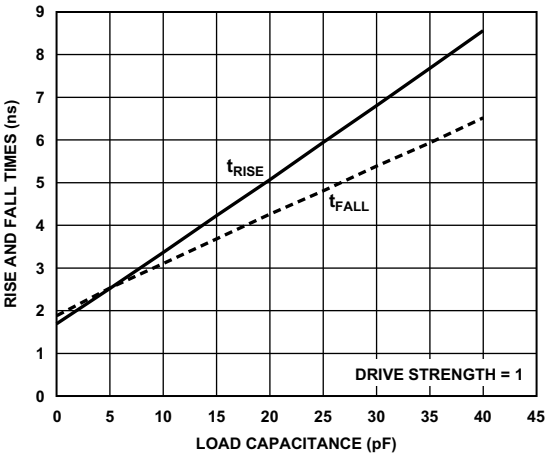


Figure 38. Digital I/O Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 1.8 V, T_J = 25°C)

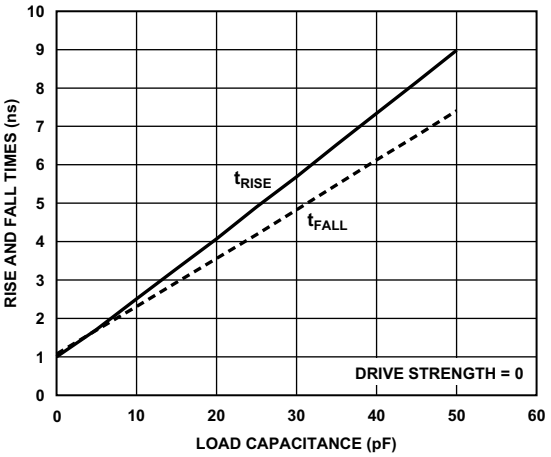


Figure 39. Digital I/O Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 3.3 V, T_J = 25°C)

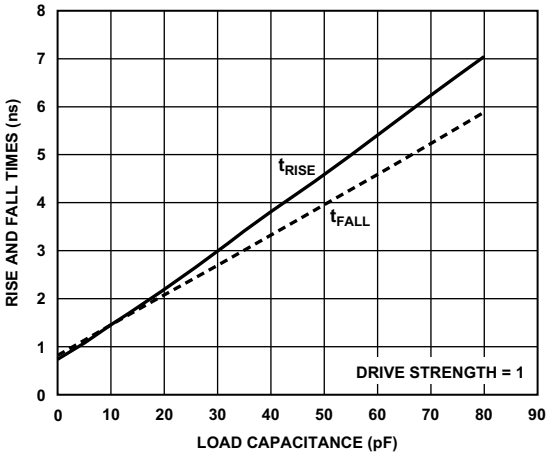


Figure 40. Digital I/O Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 3.3 V, T_J = 25°C)

In Figure 37 through Figure 40, digital I/Os include ADR1, ADR2, SCK, MISO, MOSI, SIOn, BCLK, SYNC, IRQ, and GPIO7 pins.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Package pin information is shown in Figure 41. The pin function descriptions are shown in Table 20.

All digital inputs and digital outputs are three-stated with inputs disabled during reset.

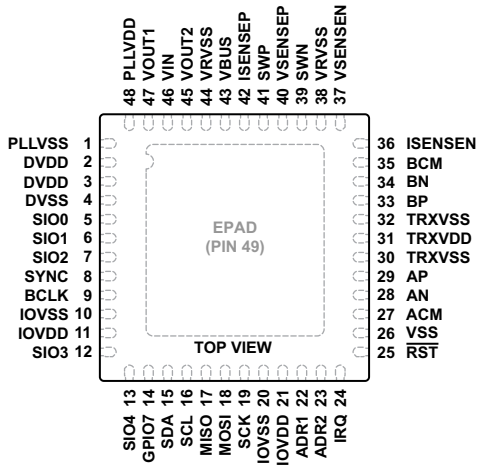


Figure 41. Package Pin Configuration

Table 20. AD2437 Pin Function Descriptions

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
1	PLLVSS	PWR	None	**Power supply pin for PLLVDD return currents.** This pin must be connected to a low impedance local ground plane.
2, 3	DVDD	PWR	None	**Power supply pin for digital core logic.** This pin must be connected to VOUT1.
4	DVSS	PWR	None	**Power supply pin for DVDD return currents.** This pin must be connected to a low impedance local ground plane.
5	SIO0[2, 3]	D_IO	PDM0 GPIO0	**Serial I/O pin 0.** This pin is a I²S/TDM receive data pin (DRX0). When PDM functions are enabled, this pin is a microphone input pin (PDM0). When not used for serial input, this pin can be configured as a general-purpose I/O pin (GPIO0).
6	SIO1[2, 3]	D_IO	PDM1 GPIO1	**Serial I/O pin 1.** This pin is a configurable I²S/TDM data pin (DRX1 or DTX3).When PDM functions are enabled, this pin is a microphone input pin (PDM1). When not used for serial I/O, this pin can be configured as a general-purpose I/O pin (GPIO1).
7	SIO2[2, 3]	D_IO	$\overline{\text{ASPISS}}$ $\overline{\text{SPISSEL1}}$ GPIO2	**Serial I/O pin 2.** This pin is a configurable I²S/TDM data pin (DRX2 or DTX2). When not used for serial I/O, this pin can be configured as the alternate SPI slave-select input pin ($\overline{\text{ASPISS}}$) or as an SPI slave-select output pin ($\overline{\text{SPISSEL1}}$). When not used for I²S/TDM or SPI purposes, this pin can be configured as a general-purpose I/O pin (GPIO2).

In this table, the type is defined as follows: PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, D_IO_OD = digital input/open-drain output, N/A = not applicable.

Table 20. AD2437 Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
8	SYNC[4]	D_IO	None	**Synchronization signal.** This signal frames the multichannel I²S/TDM data stream. For the main transceiver, this pin is a digital input driven by the host. In addition to I²S/TDM communication, this signal is also used as a PLL input by the main transceiver. This signal must be continuous and stable because the main transceiver derives all clocking information for itself and for the A²B bus from this signal. When this pin stops toggling, the A²B bus resets after a delay due to the PLL unlock operation. For more information, see Table 4. For subordinate transceivers, this pin is a digital output. It is driven based on the frame rate (normal, increased, or reduced). In parallel A²B bus mode, this pin is a digital input, wherein it accepts the SYNC signal from a paired subordinate transceiver.
9	BCLK[4]	D_IO	PDMCLK	**Bit clock.** This pin is the bit clock for the I²S/TDM interface. For the main transceiver, this pin is a digital input (driven by the host) based on the TDM mode and channel size. For subordinate transceivers, this pin is a digital output. It is driven based on the frame rate, TDM mode, and channel size configurations. It can also drive the clock for the PDM microphones. In parallel A²B bus mode, this pin is a digital input, wherein it accepts the bit clock from a paired subordinate transceiver.
10	IOVSS	PWR	None	**Power supply pin for IOVDD return current.** This pin must be connected to a low impedance local ground plane.
11	IOVDD	PWR	None	**Power supply pin for digital input and output pins.** The digital output pins are supplied from IOVDD, which also sets the highest input voltage that is allowed on the digital input pins. Two I/O voltage ranges are supported (see V_{IOVDD} specifications in the Operating Conditions section). The current draw of these pins is variable and depends on the loads of the digital outputs. IOVDD can be sourced by either the VOUT1 or VOUT2 pin. However, if the signals do not originate from logic supplied by the VOUT1 pin or VOUT2 pin, source IOVDD with an external supply.
12	SIO3[2, 3]	D_IO	GPIO3	**Serial I/O pin 3.** This pin is a configurable I²S/TDM data pin (DRX3 or DTX1). When not used for serial I/O, this pin can be configured as a general-purpose I/O pin (GPIO3).
13	SIO4[2,3]	D_IO	GPIO0	**Serial I/O pin 4.** This pin is an I²S/TDM transmit data pin (DTX0). When not used for serial I/O, this pin can be configured as a general-purpose I/O pin (GPIO0).
14	GPIO7[2]	D_IO	RRSTRB PDMCLK	**General-purpose I/O pin 7.** This pin is a dedicated general-purpose I/O pin (GPIO7). When not used for GPIO, this pin can be configured as a reduced rate strobe pin (RRSTRB) in slave mode or as the alternate PDM clock output pin (PDMCLK).
15	SDA	D_IO_OD	GPIO6	**I²C serial data.** This pin is a bidirectional open-drain input/output. Place a pull-up resistor on this pin. Consult version 2.1 of the I²C bus specification for the proper resistor value. When not used for I²C, this pin can be configured as a general-purpose I/O pin (GPIO6). Connect the pin to ground if not used.

In this table, the type is defined as follows: PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, D_IO_OD = digital input/open-drain output, N/A = not applicable.

Table 20. AD2437 Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
16	SCL	D_IO_OD	GPIO5	**Serial clock for I²C data transfers.** Clock input I²C target in A²B main node mode. Clock input (I²C target) or open-drain clock output (I²C controller) in A²B subordinate node mode. Place a pull-up resistor on this pin. Consult version 2.1 of the I²C bus specification for the proper resistor value. When not used for I²C, this pin can be configured as a general-purpose I/O pin (GPIO5). Connect the pin to ground if not used.
17	MISO[2]	D_IO	PWM1 GPIO5	**SPI Master In Slave Out pin.** This pin is a serial data pin when SPI is enabled. When not used for SPI purposes, this pin can be configured as a PWM output (PWM1) or as a general-purpose I/O (GPIO5).
18	MOSI[5]	D_IO	PWM2 GPIO6	**SPI Master Out Slave In pin.** This pin is a serial data pin when SPI is enabled. When not used for SPI purposes, this pin can be configured as a PWM output (PWM2) or as a general-purpose I/O pin (GPIO6).
19	SCK[5]	D_IO	PWM3 GPIO0	**SPI clock.** This pin is the SPI clock pin when SPI is enabled. When not used for SPI purposes, this pin can be configured as a PWM output (PWM3) or as a general-purpose I/O (GPIO0).
20	IOVSS	PWR	None	**Power supply pin for IOVDD return current.**This pin must be connected to a low impedance local ground plane.
21	IOVDD	PWR	None	**Power supply pin for digital input and output pins.** This pin is the second IOVDD pin along with Pin 11. Externally connect the two IOVDD pins together.
22	ADR1[5]	D_IO	$\overline{\text{SPISS}}$ $\overline{\text{SPISSEL0}}$ PWMOE CLKOUT GPIO4	**I²C address 1 pin.** This pin (along with the ADR2 pin) sets the I²C target device address immediately after reset deassertion. After power-on, this pin can be configured as the SPI slave-select input ($\overline{\text{SPISS}}$) pin or as an SPI slave-select output pin ($\overline{\text{SPISSEL0}}$) when SPI functions are enabled. When not used for SPI purposes, this pin can serve as the PWM output enable pin (PWMOE) when PWM functions are enabled. When not used for SPI or PWM purposes, this pin can be programmed as a clock output pin (CLKOUT1) or as a general-purpose I/O pin (GPIO4).
23	ADR2[5]	D_IO	$\overline{\text{ASPISS}}$ $\overline{\text{SPISSEL2}}$ CLKOUT GPIO4	**I²C address 2 pin.** This pin (along with the ADR1 pin) sets the I²C target device address immediately after reset deassertion. This pin can be configured as the alternate SPI slave-select input pin ($\overline{\text{ASPISS}}$) or as an SPI slave-select output pin ($\overline{\text{SPISSEL2}}$) when SPI functions are enabled. When not used for SPI purposes, this pin can be programmed as a clock output pin (CLKOUT2) or as a general-purpose I/O pin (GPIO4).
24	IRQ[6]	D_OUT	None	**Interrupt request digital output.** This pin indicates that the A²B transceiver is raising an event driven interrupt request towards the host controller. At the main transceiver, this pin indicates bit errors on the A²B bus, interrupts from GP inputs, SPI interrupts, VMTR interrupts, mailbox interrupts, and line faults detected by the main and the subordinate transceivers. At the subordinate transceiver, this pin indicates mailbox and SPI related interrupts. In bus monitor mode, this pin indicates that the A²B transceiver has a PLL lock. This pin cannot be used as a GPIO pin.
25	$\overline{\text{RST}}$	D_IN	None	**Hardware reset.** Resets the transceiver when driven low. When all the power domains are stable, this pin must be driven high externally. This pin must be pulled high with a 10 kΩ when not used.
26	VSS	PWR	None	**Power supply pin for return current.** This pin must be connected to a low impedance local ground plane.
27	ACM	A_IO	None	**Common-mode bias pin for bidirectional, differential A²B line transceiver for A port.**

In this table, the type is defined as follows: PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, D_IO_OD = digital input/open-drain output, N/A = not applicable.

Table 20. AD2437 Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
28	AN	A_IO	None	**Bidirectional inverted data pin for A port, differential A^{2}B line driver and receiver.** It is directed towards the upstream transceiver on the A^{2}B bus. This pin is self biased.
29	AP	A_IO	None	**Bidirectional noninverted data pin for A port, differential A^{2}B line driver and receiver.** It is directed towards the upstream transceiver on the A^{2}B bus. This pin is self biased.
30	TRXVSS	GND	None	**Power supply pin for TRXVDD return currents.** Connect this pin to a low impedance local ground plane.
31	TRXVDD	PWR	None	**Power supply pin for A^{2}B line driver and receiver circuit.** This pin must be connected to VOUT2.
32	TRXVSS	GND	None	**Power supply pin for TRXVDD return currents.** Connect this pin to a low impedance local ground plane.
33	BP	A_IO	None	**Noninverted pin of bidirectional, differential A^{2}B line driver and receiver B.** It is directed towards the next downstream subordinate transceiver on the A^{2}B bus. This pin is self biased.
34	BN	A_IO	None	**Inverted pin of bidirectional, differential A^{2}B line driver and receiver B.** It is directed towards the next downstream subordinate transceiver on the A^{2}B bus. This pin is self biased.
35	BCM	A_IO	None	**Common-mode input for bidirectional, differential A^{2}B line transceiver B.**
36	ISENSEN	A_IN	None	**Low side current sense input pin.** Analog input to sense the current returning from the downstream subordinate transceiver. A sense resistor, connected from ISENSEN to VSENSEN, is required to provide sensing of the return current when using a single-pair cable. This pin must be pulled low with a 100 kΩ when using XLR/DMX and CAT cables.
37	VSENSEN	A_IO	None	**Low side voltage sense input pin.** Analog input to sense the negative power supplied to the next subordinate device when using a single-pair cable. This pin must be pulled low with a 100 kΩ when using XLR/DMX and CAT cables.
38	VRVSS	PWR	None	**Power supply pin for internal voltage regulators (VOUT1 and VOUT2) return current.** Connect this pin to a low impedance local ground plane.
39	SWN	A_IO	None	**Low side MOSFET switch control pin.** This output pin drives the gate of an external low side NMOS when using a single-pair cable. This pin is driven high to turn on a switch to deliver power to the next subordinate device. The pin is driven low by default and when fault conditions occur. This pin requires an external pull-down resistor to keep the external NMOS off during bus initialization. This pin must be pulled low with a 100 kΩ when using XLR/DMX and CAT cables.
40	VSENSEP	A_IO	None	**High side voltage sense input pin.** Analog input to sense the bus bias voltage supplied to the next subordinate device.
41	SWP	A_OUT	None	**High side MOSFET switch control pin.** This output pin drives the gate of an external high side NMOS. When controlling the NMOS, a voltage above VBUS is maintained on this output pin to turn the external NMOS on and keep it powered during normal operation to deliver power to the next subordinate device. The pin is driven low when fault conditions occur. For the last subordinate node, connect this pin per the reference schematic.

In this table, the type is defined as follows: PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, D_IO_OD = digital input/open-drain output, N/A = not applicable.

Table 20. AD2437 Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
42	ISENSEP	A_IN	None	**High side current sense input pin.** Analog input to sense the current supplied to the next subordinate device. A sense resistor must be connected between VBUS and ISENSEP.
43	VBUS	A_IN	None	**Analog input pin for sensing bus bias voltage and high side current.**
44	VRVSS	PWR	None	**Power supply pin for internal voltage regulators (VOUT1 and VOUT2) return current.** Connect this pin to a low impedance local ground plane.
45	VOUT2	PWR	None	**Output of the on-chip low dropout voltage regulator 2.** This regulated voltage output pin must be connected to the TRXVDD power supply pin. External devices can also be powered by this supply. Refer to the VREG Safe Operating Area section. In LVI mode, connect this pin to VIN.
46	VIN	PWR	None	**Power supply input pin.**
47	VOUT1	PWR	None	**Output of the on-chip low dropout voltage regulator 1.** This regulated voltage output pin must be connected to the DVDD and PLLVDD power supply pins. External devices can also be powered by this supply. Refer to the VREG Safe Operating Area section.
48	PLLVDD	PWR	None	**Power supply for PLL.** This pin must be connected to VOUT1.
49	EPAD	PWR	None	**Power supply for return currents.** See other VSS description in this table. This pin is the exposed pad on the bottom of the package. This exposed pad must be connected to a low impedance local ground plane.

In this table, the type is defined as follows: PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, D_IO_OD = digital input/open-drain output, N/A = not applicable.

[1] See the *AD2437 A²B Transceiver Technical Reference* for more information about configuring pins for alternate functions.
[2] These pins are in the high impedance state until they are configured.
[3] Refer to Table 2 for the SIO pin mapped functions.
[4] In A²B main node mode, the BCLK and SYNC pins are in a high impedance state after reset and are configured as input pins once the PLL locks. In A²B subordinate node mode, the BCLK and SYNC pins are in a high impedance state until they are configured.
[5] This pin is a digital input after reset.
[6] The IRQ pin is in a high impedance state after reset. It is configured as an output after the PLL locks.

DESIGNER REFERENCE

Contact your local Analog Devices representative for the latest schematic circuit recommendations and bill of materials for node configurations. The recommended circuit and component selection must be followed to ensure interoperability between AD2437 systems.

PCB LAYOUT

The transceivers are highly integrated devices, comprising both digital sections for audio data, clocks, PLL, and analog A^2B transceiver sections. PCB layout plays an important role in ensuring system performance. For detailed layout guidelines, see the *A^2B System Specification*.

RECOMMENDED PCB FOOTPRINT

Figure 42 shows the transceiver footprint. Solder the exposed paddle underneath the transceiver effectively to the PCB where it is locally connected to the ground plane.

See "Soldering Considerations for Exposed-Pad Packages (EE-352)", on the Analog Devices web site. The exposed paddle is used for a thermal pathway as well as for electrical connection.

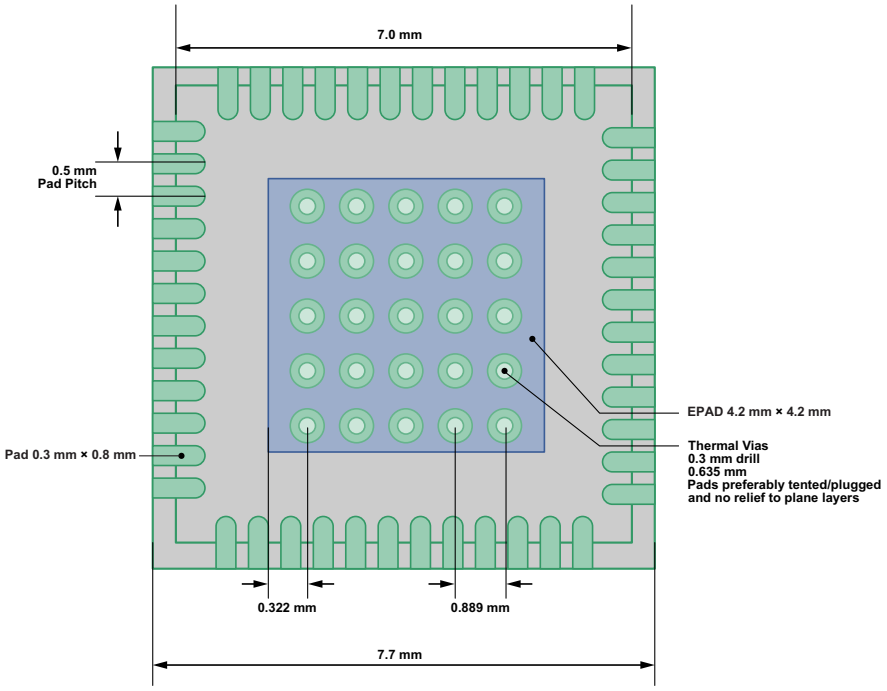


Figure 42. Transceiver Footprint

OUTLINE DIMENSIONS

Figure 43 shows the outline dimensions for the 48-Lead LFCSP (CP-48-26).

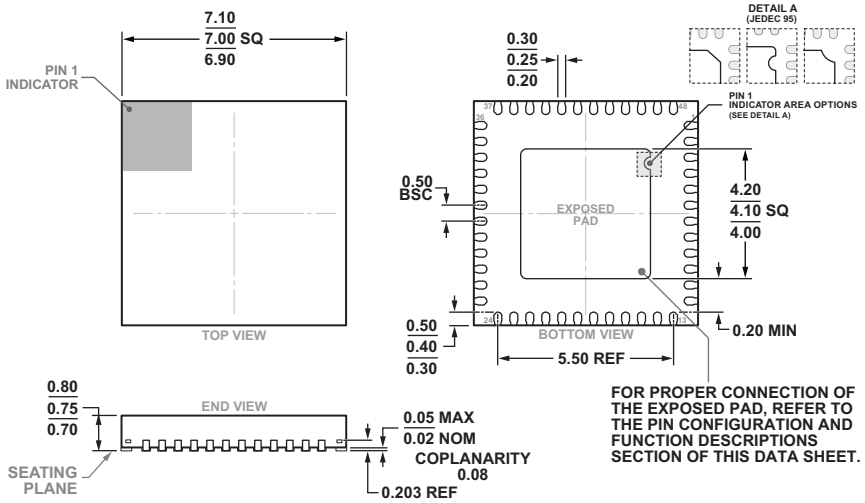


Figure 43. 48-Lead Frame Chip Scale Package [LFCSP]
7 mm x 7 mm Body and 0.75 mm Package Height
(CP-48-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range[3]	Package Description	Package Option
AD2437KCPZY	0°C to 105°C	48-Lead Frame Chip Scale Package [LFCSP]	CP-48-26
AD2437KCPZY-RL	0°C to 105°C	48-Lead Frame Chip Scale Package [LFCSP]	CP-48-26
AD2437BCPZY	–40°C to +105°C	48-Lead Frame Chip Scale Package [LFCSP]	CP-48-26
AD2437BCPZY-RL	–40°C to +105°C	48-Lead Frame Chip Scale Package [LFCSP]	CP-48-26

[1] Z = RoHS Compliant Part.
[2] RL = Supplied on Tape and Reel.
[3] Referenced temperature is junction temperature. See the Operating Conditions section for junction temperature (T_J) specification.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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