Evaluation of the ADRF5717 Silicon Digital Attenuator, 2-Bit, 1 MHz to 30 GHz

FEATURES

- Full featured evaluation board for the ADRF5717
- Easy connection to test equipment
- Additional through line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5717 is a 2-bit digital attenuator with 48 dB attenuation range manufactured in the silicon on insulator (SOI) process.

This user guide describes the ADRF5717-EVALZ evaluation board, which is designed to simply evaluate the features and performance of the ADRF5717. A photograph of the evaluation board is shown in Figure 1.

For full details on the ADRF5715, see the ADRF5715 data sheet, which should be consulted in conjunction with this user guide when using the ADRF5717-EVALZ.

ADRF5717-EVALZ EVALUATION BOARD PHOTOGRAPH

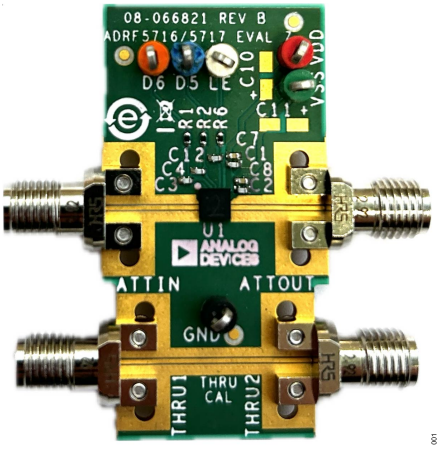

Figure 1. ADRF5717-EVALZ Evaluation Board Photograph

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REVISION HISTORY

12/2023—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5717-EVALZ is a connectorized board, assembled with the ADRF5717 and its application circuitry. All components are placed on the primary side of ADRF5717-EVALZ. An assembly drawing for the ADRF5717-EVALZ is shown in Figure 8, and an evaluation board schematic is shown in Figure 7.

BOARD LAYOUT

The ADRF5717-EVALZ is designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

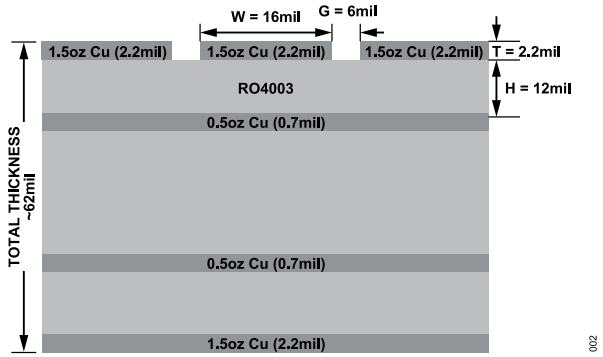

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1.5 oz (2.2 mil) thick and the inner layers are 0.5 oz (0.7 mil) thick.

The top dielectric material is 12 mil Rogers 4003, which provides 50 Ω controlled impedance and optimizes the high frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining two layers are also ground planes filled with FR4 material to manage the thermal rise during high power operations and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62 mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 16 mil and ground spacing of 6 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of the CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5717, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY AND CONTROL INPUTS

The ADRF5717-EVALZ has two power-supply inputs, three control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, D5, D6, LE, and GND. A +3.3 V supply is connected to the DC test points on VDD, and the −3.3 V supply is connected to the DC test points on VSS. Ground reference can be connected to GND. Connect D5, D6, and LE to 3.3 V or 0 V. The typical total current consumption for the ADRF5717 is 0.73 mA.

The VDD and VSS supply pins and control pins of the ADRF5717 are decoupled with 100 pF capacitor.

Table 1. Power Supply and Control Inputs

Test Point	Description
VDD	+3.3 V supply voltage
VSS	−3.3 V supply voltage
D5	Control Input 1
D6	Control Input 2
LE	Latch enable
GND	Ground

RF INPUTS AND OUTPUTS

The ADRF5717-EVALZ has four edge-mounted, 2.92 mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

SMA Connector	Description
ATTIN	Attenuator input
ATTOUT	Attenuator output
THRU1	Thru line input and output
THRU2	Thru line input and output

The ADRF5717-EVALZ is shipped together with a thru line that calibrates out the board loss effects from the measurements determining the device performance at the pins of the IC.

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5717-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the D5, D6, and LE test points.
5. Apply an RF input signal.

The ADRF5717-EVALZ is shipped fully assembled and tested. Figure 3 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and to verify the operation of the ADRF5717-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage output terminal of the 3.3 V supply.
3. Connect the VSS test point to the voltage output terminal of the −3.3 V supply. Note that the current from VDD test point is around 230 µA and from VSS test point is around 500 µA.
4. Connect the V1, V2, EN, and LS test points to the voltage output terminal of the 3.3 V supply. The ADRF5717 can be configured in different modes by connecting the control test points to 3.3 V or 0 V, as shown in Table 3.
5. Connect a calibrated network analyzer to the ATTIN and ATTOUT 2.92 mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50 Ω. Sweep the frequency from 1 MHz to 30 GHz and set the power to 10 dBm.
6. The ADRF5717-EVALZ is expected to have an insertion loss of 2.8 dB at 30 GHz. See the expected results in Figure 4.

Additional test equipment is needed to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.92 mm connectors of the ADRF5717-EVALZ include the losses of the 2.92 mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5717-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

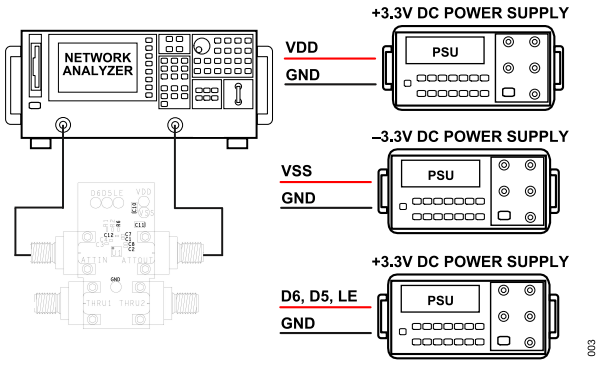

Figure 3. Test Setup Diagram

Table 3. Control Voltage Truth Table

D5	D6	Attenuation State (dB)
Low	Low	0
High	Low	16
Low	High	32
High	High	48

TEST PROCEDURE

EXPECTED RESULTS

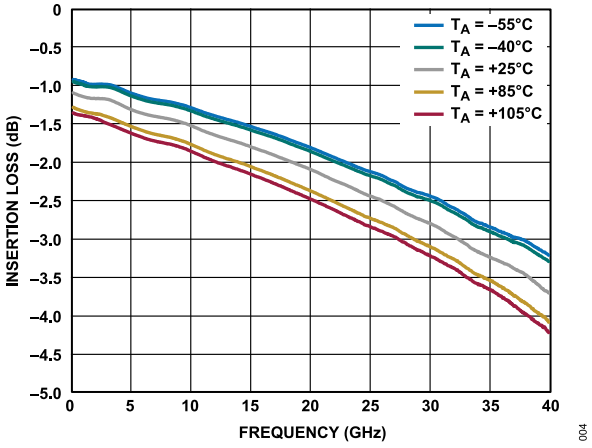

Figure 4. Insertion Loss for RFC to RFx On vs. Frequency

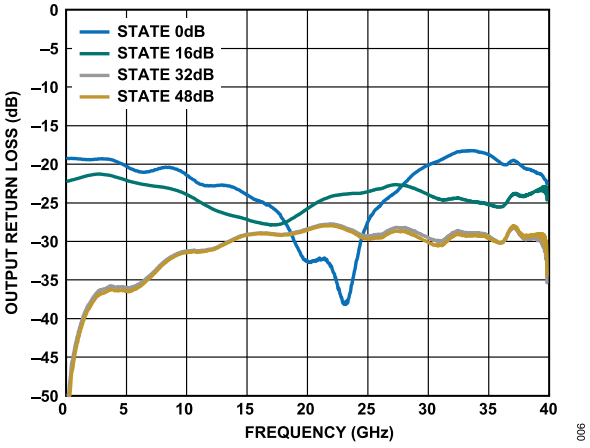

Figure 6. Output Return Loss vs. Frequency

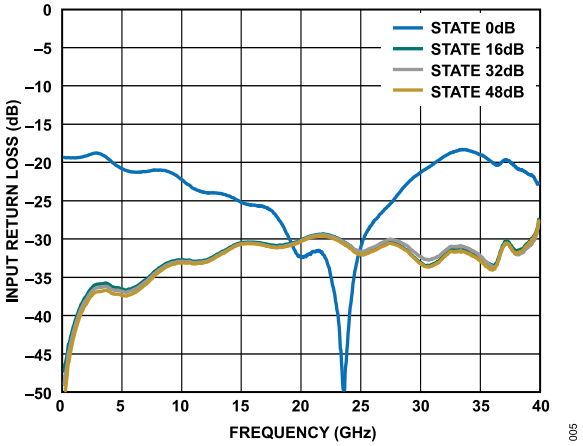

Figure 5. Input Return Loss vs. Frequency

EVALUATION BOARD SCHEMATIC AND ARTWORK

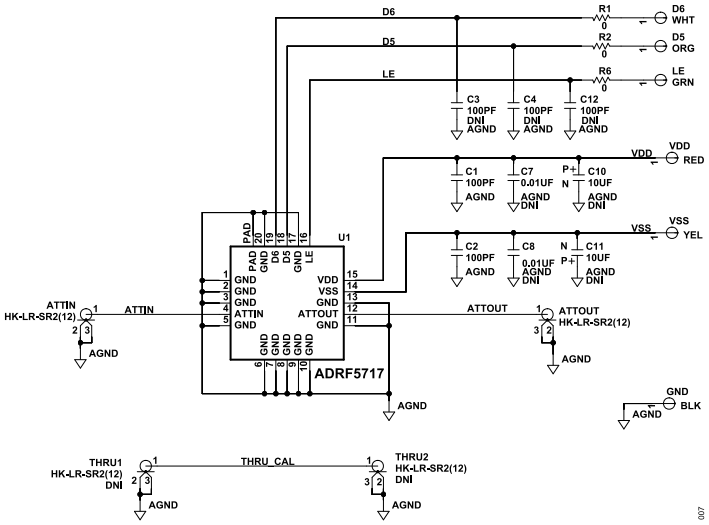

Figure 7. ADRF5717-EVALZ Evaluation Board Schematic

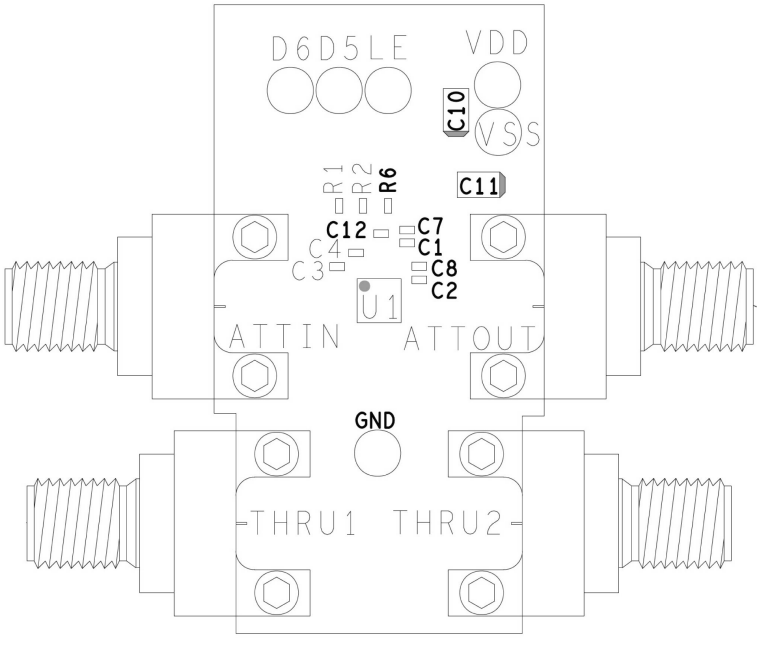

Figure 8. ADRF5717-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5717-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
2	C1 and C2	Capacitors, 100 pF, 50 V, C0402 package	Murata	GCM1555C1H101JA16D
3	R1, R2, and R6	Resistors, 0 Ω, 1/16 W, R0402 package	Hirose Electronic Co.	RC0402JR-070RL
2	ATTIN and ATTOUT	Edge-mount 2.92 mm connectors	Hirose Electronic Co.	HK-LR-SR2(12)
1	D5	Surface-mount test point	Components Corporation	TP-105-40-03
5	VDD, VSS, D6, GND, and LE	Surface-mount test points	Components Corporation	TP-104-01-0X
1	U1	Silicon digital attenuator, 2-bit, 1 MHz to 30 GHz	Analog Devices, Inc.	ADRF5717
1	PCB	ADRF5717 evaluation board	Analog Devices	ADRF5717-EVALZ